REV	DESCRIPTION	DATE	APPROVED
A	Initial schematic for layout	11/07/2012	RRP
B	Beta updates	02/12/2013	TNYC
C	PLC UPDATES	06/18/2013	TNYC

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APPLICATION

DWN	R.R.P.	DATE 02/21/3013
CHK	T.W.K.	DATE 02/21/3013
ENGR	R.R.P.	DATE 02/21/3013
ENGR-MGR	R.R.P.	DATE 02/21/3013
QA	C.M.D.	DATE 02/21/3013
MFG	R.R.P.	DATE 02/21/3013
RLSE	R.R.P.	DATE 02/21/3013

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[XDMA_EVENT_INTR0//TIMER4/CLKOUT1/SPI1_CS1/PR1_PRU1_PRU_R31_16/EMU2/GPIO0_19] XDMA_EVENT_INTR0
[XDMA_EVENT_INTR1//TCLKIN/CLKOUT2/TIMER7/PR1_PRU0_PRU_R31_16/EMU3/GPIO0_20] XDMA_EVENT_INTR1

AM335x

15mm x 15mm Package

[GPMC_CLK/LCD_MEMORY_CLK/GPMC_WAIT1/MMC2_CLK/PR1_MII1_CRS/PR1_MDIO_MDCLK/MCASP0_FSR/GPIO2_1] GPMC_CLK
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[GPMC_CSN1/GPMC_CLK/MMC1_CLK/PR1_EDIO_DATA_IN6/PR1_EDIO_DATA_OUT6/PR1_PRU1_PRU_R30_12/PR1_PRU1_PRU_R31_12/GPIO1_30] GPMC_CSn1
[GPMC_CSN2/GPMC_BE1N/MMC1_CMD/PR1_EDIO_DATA_IN7/PR1_EDIO_DATA_OUT7/PR1_PRU1_PRU_R30_13/PR1_PRU1_PRU_R31_13/GPIO1_31] GPMC_CSn2
[GPMC_CSN3///MMC2_CMD/PR1_MII0_CRS/PR1_MDIO_DATA/EMU4/GPIO2_0] GPMC_CSn3
[GPMC_WEN//TIMER6/////GPIO2_4] GPMC_WEn
[GPMC_OEN_REN//TIMER6/////GPIO2_4] GPMC_OEn_REn
[GPMC_ADVN_ALE//TIMER4/////GPIO2_2] GPMC_ADVn_ALE
[GPMC_BE0N_CLE//TIMER5/////GPIO2_5] GPMC_BEn0_CLE
[GPMC_BE1N/GMII2_COL/GPMC_CSN6/MMC2_DAT3/GPMC_DIR/PR1_MII1_RXLINK/MCASP0_ACLKR/GPIO1_28] GPMC_BEn1
[GPMC_WAIT0/GMII2_CRS/GPMC_CSN4/RMII2_CRS_DV/MMC1_SDCD/PR1_MII1_COL/UART4_RXD/GPIO0_30] GPMC_WAIT0
[GPMC_WPN/GMII2_RXERR/GPMC_CSN5/RMII2_RXERR/MMC2_SDCD/PR1_MII1_TXEN/UART4_TXD/GPIO0_31] GPMC_WPn

[GPMC_AD0/MMC1_DAT0/////GPIO1_0] GPMC_AD0
[GPMC_AD1/MMC1_DAT1/////GPIO1_1] GPMC_AD1
[GPMC_AD2/MMC1_DAT2/////GPIO1_2] GPMC_AD2
[GPMC_AD3/MMC1_DAT3/////GPIO1_3] GPMC_AD3
[GPMC_AD4/MMC1_DAT4/////GPIO1_4] GPMC_AD4
[GPMC_AD5/MMC1_DAT5/////GPIO1_5] GPMC_AD5
[GPMC_AD6/MMC1_DAT6/////GPIO1_6] GPMC_AD6
[GPMC_AD7/MMC1_DAT7/////GPIO1_7] GPMC_AD7
[GPMC_AD8/LCD_DATA23/MMC1_DAT0/MMC2_DAT4/EHRPWM2A/PR1_MII_MT0_CLK//GPIO0_22] GPMC_AD8
[GPMC_AD9/LCD_DATA22/MMC1_DAT1/MMC2_DAT5/EHRPWM2B/PR1_MII0_COL//GPIO0_23] GPMC_AD9
[GPMC_AD10/LCD_DATA21/MMC1_DAT2/MMC2_DAT6/EHRPWM2_TRIPZONE_INPUT/PR1_MII0_TXEN//GPIO0_26] GPMC_AD10
[GPMC_AD11/LCD_DATA20/MMC1_DAT3/MMC2_DAT7/EHRPWM2_SYNCO/PR1_MII0_TXD3//GPIO0_27] GPMC_AD11
[GPMC_AD12/LCD_DATA19/MMC1_DAT4/MMC2_DAT0/EQEP2A_IN/PR1_MII0_TXD2/PR1_PRU0_PRU_R30_14/GPIO1_12] GPMC_AD12
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AM335X_15x15

Clockout Measurement Testpoints

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D14 — TP1mm TP45

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SCKT1

AM335x
15x15
Socket

AM335X 15x15 Socket

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[MCASP0_AHCLKX/EQEP0_STROBE/MCASP0_AXR3/MCASP1_AXR1/EMU4/PR1_PRU0_PRU_R30_7/PR1_PRU0_PRU_R31_7/GPIO3_21]
[MCASP0_ACLKX/EHRPWM0A//SPI1_SCLK/MMC0_SDCD/PR1_PRU0_PRU_R30_0/PR1_PRU0_PRU_R31_0/GPIO3_14]
[MCASP0_FSX/EHRPWM0B//SPI1_D0/MMC1_SDCD/PR1_PRU0_PRU_R30_1/PR1_PRU0_PRU_R31_1/GPIO3_15]
[MCASP0_AXR0/EHRPWM0_TRIPZONE_INPUT//SPI1_D1/MMC2_SDCD/PR1_PRU0_PRU_R30_2/PR1_PRU0_PRU_R31_2/GPIO3_16]
[MCASP0_AHCLKR/EHRPWM0_SYNCI_O/MCASP0_AXR2/SPI1_CS0/ECAP2_IN_PWM2_OUT/PR1_PRU0_PRU_R30_3/PR1_PRU0_PRU_R31_3/GPIO3_17]
[MCASP0_ACLKR/EQEP0A_IN/MCASP0_AXR2/MCASP1_ACLKX/MMC0_SDWP/PR1_PRU0_PRU_R30_4/PR1_PRU0_PRU_R31_4/GPIO3_18]
[MCASP0_FSR/EQEP0B_IN/MCASP0_AXR3/MCASP1_FSX/EMU2/PR1_PRU0_PRU_R30_5/PR1_PRU0_PRU_R31_5/GPIO3_19]
[MCASP0_AXR1/EQEP0_INDEX//MCASP1_AXR0/EMU3/PR1_PRU0_PRU_R30_6/PR1_PRU0_PRU_R31_6/GPIO3_20]

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MCASP0_ACLKX	A13	AM335X_EHRPWM0A_ESAM_PARITY	33	
MCASP0_FSX	B13	ESAM_RESET	33	
MCASP0_AXR0	D12	AM335X_MCASP0_AXR0_RS485_TXD	30	
MCASP0_AHCLKR	C12	AM335X_MCASP0_AXR2_RS485_RXD	30	
MCASP0_ACLKR	B12	EXP_ETH1_RSTn	38	
MCASP0_FSR	C13	EXP_ETH0_RSTn	37	
MCASP0_AXR1	D13	AM335X_MCASP1_AXR0_ESAM_RXD	33	

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[MMC0_CMD/GPMC_A25/UART3_RTSN/UART2_TXD/DCAN1_RX/PR1_PRU0_PRU_R30_13/PR1_PRU0_PRU_R31_13/GPIO2_31]
[MMC0_DAT0/GPMC_A23/UART5_RTSN/UART3_TXD/UART1_RIN/PR1_PRU0_PRU_R30_11/PR1_PRU0_PRU_R31_11/GPIO2_29]
[MMC0_DAT1/GPMC_A22/UART5_CTSN/UART3_RXD/UART1_DTRN/PR1_PRU0_PRU_R30_10/PR1_PRU0_PRU_R31_10/GPIO2_28]
[MMC0_DAT2/GPMC_A21/UART4_RTSN/TIMER6/UART1_DSRN/PR1_PRU0_PRU_R30_9/PR1_PRU0_PRU_R31_9/GPIO2_27]
[MMC0_DAT3/GPMC_A20/UART4_CTSN/TIMER5/UART1_DCDN/PR1_PRU0_PRU_R30_8/PR1_PRU0_PRU_R31_8/GPIO2_26]

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MMC0_CMD	G18	AM335X_UART2_TXD	6	
MMC0_DAT0	G16	UART3_TXD	27	
MMC0_DAT1	G15	UART3_RXD	27	
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3V3_EVM

3V3_EVM 3V3_EVM 5,6,9,11,18,19,21,23,25,26,27,28,29,30,31,32,33,37,38,40,41,42

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[LCD_DATA0/GPMC_A0/PR1_MII_MT0_CLK/EHRPWM2A//PR1_PRU1_PRU_R30_0/PR1_PRU1_PRU_R31_0/GPIO2_6]
[LCD_DATA1/GPMC_A1/PR1_MII0_TXEN/EHRPWM2B//PR1_PRU1_PRU_R30_1/PR1_PRU1_PRU_R31_1/GPIO2_7]
[LCD_DATA2/GPMC_A2/PR1_MII0_TXD3/EHRPWM2_TRIPZONE_INPUT//PR1_PRU1_PRU_R30_2/PR1_PRU1_PRU_R31_2/GPIO2_8]
[LCD_DATA3/GPMC_A3/PR1_MII0_TXD2/EHRPWM2_SYNCI_O//PR1_PRU1_PRU_R30_3/PR1_PRU1_PRU_R31_3/GPIO2_9]
[LCD_DATA4/GPMC_A4/PR1_MII0_TXD1/EQEP2A_IN//PR1_PRU1_PRU_R30_4/PR1_PRU1_PRU_R31_4/GPIO2_10]
[LCD_DATA5/GPMC_A5/PR1_MII0_TXD0/EQEP2B_IN//PR1_PRU1_PRU_R30_5/PR1_PRU1_PRU_R31_5/GPIO2_11]
[LCD_DATA6/GPMC_A6/PR1_EDIO_DATA_IN6/EQEP2_INDEX/PR1_EDIO_DATA_OUT6/PR1_PRU1_PRU_R30_6/PR1_PRU1_PRU_R31_6/GPIO2_12]
[LCD_DATA7/GPMC_A7/PR1_EDIO_DATA_IN7/EQEP2_STROBE/PR1_EDIO_DATA_OUT7/PR1_PRU1_PRU_R30_7/PR1_PRU1_PRU_R31_7/GPIO2_13]

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LCD_DATA1 R2 AM335X_LCD_DATA1 — AM335X_LCD_DATA1 19
LCD_DATA2 R3 AM335X_LCD_DATA2 — AM335X_LCD_DATA2 19
LCD_DATA3 R4 AM335X_LCD_DATA3 — AM335X_LCD_DATA3 19
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LCD_DATA5 T2 AM335X_LCD_DATA5 — AM335X_LCD_DATA5 19
LCD_DATA6 T3 AM335X_LCD_DATA6 — AM335X_LCD_DATA6 19
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[LCD_DATA8/GPMC_A12/EHRPWM1_TRIPZONE_INPUT/MCASP0_ACLKX/UART5_TXD/PR1_MII0_RXD3/UART2_CTSN/GPIO2_14]
[LCD_DATA9/GPMC_A13/EHRPWM1_SYNCO/MCASP0_FSX/UART5_RXD/PR1_MII0_RXD2/UART2_RTSN/GPIO2_15]
[LCD_DATA10/GPMC_A14/EHRPWM1A/MCASP0_AXR0//PR1_MII0_RXD1/UART3_CTSN/GPIO2_16]
[LCD_DATA11/GPMC_A15/EHRPWM1B/MCASP0_AHCLKR/MCASP0_AXR2/PR1_MII0_RXD0/UART3_RTSN/GPIO2_17]
[LCD_DATA12/GPMC_A16/EQEP1A_IN/MCASP0_ACLKR/MCASP0_AXR2/PR1_MII0_RXLINK/UART4_CTSN/GPIO0_8]
[LCD_DATA13/GPMC_A17/EQEP1B_IN/MCASP0_FSR/MCASP0_AXR3/PR1_MII0_RXER/UART4_RTSN/GPIO0_9]
[LCD_DATA14/GPMC_A18/EQEP1_INDEX/MCASP0_AXR1/UART5_RXD/PR1_MII_MR0_CLK/UART5_CTSN/GPIO0_10]
[LCD_DATA15/GPMC_A19/EQEP1_STROBE/MCASP0_AHCLKX/MCASP0_AXR3/PR1_MII0_RXDV/UART5_RTSN/GPIO0_11]

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[LCD_VSYNC/GPMC_A8//PR1_EDIO_DATA_IN2/PR1_EDIO_DATA_OUT2/PR1_PRU1_PRU_R30_8/PR1_PRU1_PRU_R31_8/GPIO2_22]
[LCD_HSYNC/GPMC_A9//PR1_EDIO_DATA_IN3/PR1_EDIO_DATA_OUT3/PR1_PRU1_PRU_R30_9/PR1_PRU1_PRU_R31_9/GPIO2_23]
[LCD_AC_BIAS_EN/GPMC_A11/PR1_MII1_CRS/PR1_EDIO_DATA_IN5/PR1_EDIO_DATA_OUT5/PR1_PRU1_PRU_R30_11/PR1_PRU1_PRU_R31_11/GPIO2_25]

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LEDS

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AM335X_LCD_DATA6 0 R98 — CC_GPIO2 40
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AM335X

15mm x 15mm Package

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[SPI0_D1/MMC1_SDWP/I2C1_SDA/EHRPWM0_TRIPZONE_INPUT/PR1_UART0_RXD/PR1_EDIO_DATA_IN0/PR1_EDIO_DATA_OUT0/GPIO0_4]	SPI0_D1	B16		AM335X_SPI0_D1 23
[SPI0_CS0/MMC2_SDWP/I2C1_SCL/EHRPWM0_SYNCI/PR1_UART0_TXD/PR1_EDIO_DATA_IN1/PR1_EDIO_DATA_OUT1/GPIO0_5]	SPI0_CS0	A16		AM335X_SPI0_CS0 23
[SPI0_CS1/UART3_RXD/ECAP1_IN_PWM1_OUT/MMC0_POW/XDMA_EVENT_INTR2/MMC0_SDCD/EMU4/GPIO0_6]	SPI0_CS1	C15	0 R320	ECAP1_IN_PWM1_OUT 28
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[UART0_RXD/SPI1_CS0/DCAN0_TX/I2C2_SDA/ECAP2_IN_PWM2_OUT/PR1_PRU1_PRU_R30_14/PR1_PRU1_PRU_R31_14/GPIO1_10]	UART0_RXD	E15		AM335X_UART0_RXD 27
[UART0_CTSN/UART4_RXD/DCAN1_TX/I2C1_SDA/SPI1_D0/TIMER7/PR1_EDC_SYNC0_OUT/GPIO1_8]	UART0_CTSn	E18		AM335X_UART4_RXD 27,31
[UART0_RTSN/UART4_TXD/DCAN1_RX/I2C1_SCL/SPI1_D1/SPI1_CS0/PR1_EDC_SYNC1_OUT/GPIO1_9]	UART0_RTSn	E17		AM335X_UART4_TXD 27,31
[UART1_TXD/MMC2_SDWP/DCAN1_RX/I2C1_SCL//PR1_UART0_TXD/PR1_PRU0_PRU_R31_16/GPIO0_15]	UART1_TXD	D15		AM335X_UART1_TXD 6
[UART1_RXD/MMC1_SDWP/DCAN1_TX/I2C1_SDA//PR1_UART0_RXD/PR1_PRU1_PRU_R31_16/GPIO0_14]	UART1_RXD	D16		AM335X_UART1_RXD 6
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3V3_EVM

R306 4.7K

R294 4.7K

AM335X_I2C0_SCL

AM335X_I2C0_SDA

3V3_EVM

R466 4.7K

R438 4.7K

AM335X_SPI0_CS0

AM335X_SPI0_D1

3V3_EVM

3V3_EVM 3V3_EVM 6,9,11,18,19,21,23,25,26,27,28,29,30,31,32,33,37,38,40,41,42

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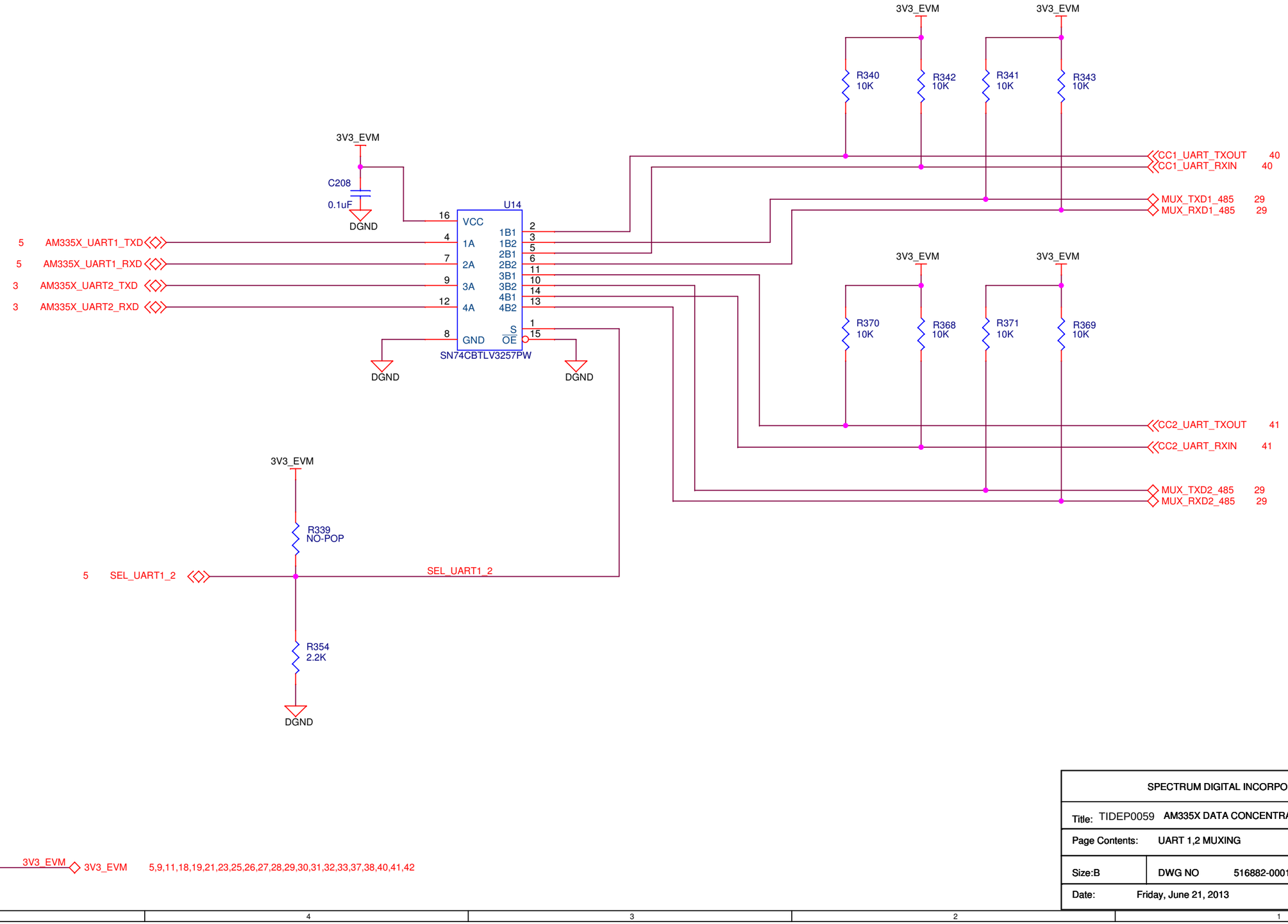

SPECTRUM DIGITAL INCORPORATED		
Title: TIDEP0059 AM335X DATA CONCENTRATOR		
Page Contents: UART 1,2 MUXING		
Size:B	DWG NO 516882-0001	Revision: B
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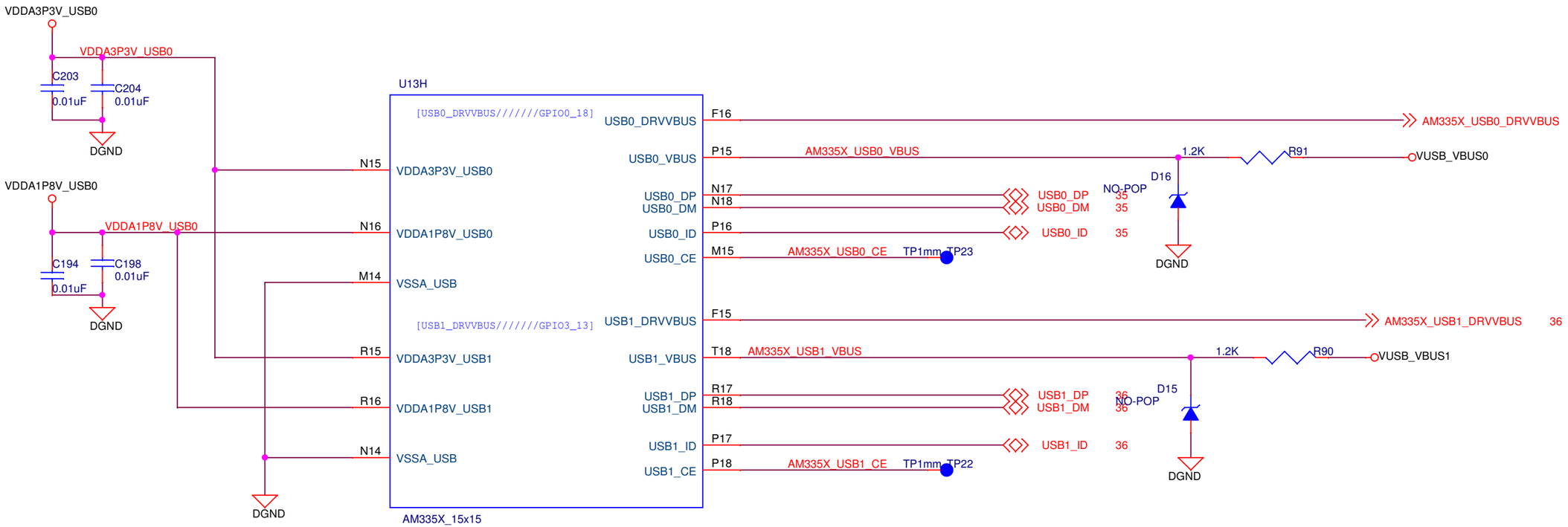

SPECTRUM DIGITAL INCORPORATED		
Title: TIDEP0059 AM335X DATA CONCENTRATOR		
Page Contents: AM335X USB INTERFACES		
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U13G

[GMII1_TXCLK/UART2_RXD/RGMII1_TCLK/MMC0_DAT7/MMC1_DAT0/UART1_DCDN/MCASP0_ACLKX/GPIO3_9]	MII1_TXCLK	K18	AM335X_RGMII1_TXC	22	R344	ETH_TXCLK	ETH_TXCLK	37
[GMII1_TXEN/RMII1_TXEN/RGMII1_TCTL/TIMER4/MCASP1_AXR0/EQEP0_INDEX/MMC2_CMD/GPIO3_3]	MII1_TXEN	J16	AM335X_RGMII1_TXCTL	22	R332	ETH_TXEN	ETH_TXEN	37
[GMII1_TXD0/RMII1_TXD0/RGMII1_TD0/MCASP1_AXR2/MCASP1_ACLKR/EQEP0B_IN/MMC1_CLK/GPIO0_28]	MII1_TXD0	K17	AM335X_RGMII1_TXD0	22	R337	ETH_TXD0	ETH_TXD0	37
[GMII1_TXD1/RMII1_TXD1/RGMII1_TD1/MCASP1_FSR/MCASP1_AXR1/EQEP0A_IN/MMC1_CMD/GPIO0_21]	MII1_TXD1	K16	AM335X_RGMII1_TXD1	22	R347	ETH_TXD1	ETH_TXD1	37
[GMII1_TXD2/DCAN0_RX/RGMII1_TD2/UART4_TXD/MCASP1_AXR0/MMC2_DAT2/MCASP0_AHCLKX/GPIO0_17]	MII1_TXD2	K15	AM335X_RGMII1_TXD2	22	R353	ETH_TXD2	ETH_TXD2	37
[GMII1_TXD3/DCAN0_TX/RGMII1_TD3/UART4_RXD/MCASP1_FSX/MMC2_DAT1/MCASP0_FSR/GPIO0_16]	MII1_TXD3	J18	AM335X_RGMII1_TXD3	22	R334	ETH_TXD3	ETH_TXD3	37
[GMII1_RXCLK/UART2_TXD/RGMII1_RCLK/MMC0_DAT6/MMC1_DAT1/UART1_DSRN/MCASP0_FSX/GPIO3_10]	MII1_RXCLK	L18	AM335X_RGMII1_RXC	37				
[GMII1_RXDV/LCD_MEMORY_CLK/RGMII1_RCTL/UART5_TXD/MCASP1_ACLKX/MMC2_DAT0/MCASP0_ACLKR/GPIO3_4]	MII1_RXDV	J17	AM335X_RGMII1_RXCTL	37				
[GMII1_RXD0/RMII1_RXD0/RGMII1_RD0/MCASP1_AHCLKX/MCASP1_AHCLKR/MCASP1_ACLKR/MCASP0_AXR3/GPIO2_21]	MII1_RXD0	M16	AM335X_RGMII1_RXD0	37				
[GMII1_RXD1/RMII1_RXD1/RGMII1_RD1/MCASP1_AXR3/MCASP1_FSR/EQEP0_STROBE/MMC2_CLK/GPIO2_20]	MII1_RXD1	L15	AM335X_RGMII1_RXD1	37				
[GMII1_RXD2/UART3_TXD/RGMII1_RD2/MMC0_DAT4/MMC1_DAT3/UART1_RIN/MCASP0_AXR1/GPIO2_19]	MII1_RXD2	L16	AM335X_RGMII1_RXD2	37				
[GMII1_RXD3/UART3_RXD/RGMII1_RD3/MMC0_DAT5/MMC1_DAT2/UART1_DTRN/MCASP0_AXR0/GPIO2_18]	MII1_RXD3	L17	AM335X_RGMII1_RXD3	37				
[GMII1_COL/RMII2_REFCLK/SPI1_SCLK/UART5_RXD/MCASP1_AXR2/MMC2_DAT3/MCASP0_AXR2/GPIO3_0]	MII1_COL	H16	AM335X_SPI1_SCLK	9				
[GMII1_CRS/RMII1_CRS_DV/SPI1_D0/I2C1_SDA/MCASP1_ACLKX/UART5_CTSN/UART2_RXD/GPIO3_1]	MII1_CRS	H17	AM335X_SPI1_D0	9				
[RMII1_REFCLK/XDMA_EVENT_INTR2/SPI1_CS0/UART5_TXD/MCASP1_AXR3/MMC0_POW/MCASP1_AHCLKX/GPIO0_29]	MII1_REFCLK	H18	AM335X_SPI1_CS0	9				
[GMII1_RXERR/RMII1_RXERR/SPI1_D1/I2C1_SCL/MCASP1_FSX/UART5_RTSN/UART2_TXD/GPIO3_2]	MII1_RXERR	J15	AM335X_SPI1_D1	9				
[GPMC_A6/GMII2_TXCLK/RGMII2_TCLK/MMC2_DAT4/GPMC_A22/PR1_MII1_RXD2/EQEP1_INDEX/GPIO1_22]	GPMC_A6	U15	AM335X_RGMII2_TXC	22	R392	ETH1_TXCLK	ETH1_TXCLK	38
[GPMC_A0/GMII2_TXEN/RGMII2_TCTL/RMII2_TXEN/GPMC_A16/PR1_MII_MT1_CLK/EHRPWM1_TRIPZONE_INPUT/GPIO1_16]	GPMC_A0	R13	AM335X_RGMII2_TXCTL	22	R396	ETH1_TXEN	ETH1_TXEN	38
[GPMC_A5/GMII2_TXD0/RGMII2_TD0/RMII2_TXD0/GPMC_A21/PR1_MII1_RXD3/EQEP1B_IN/GPIO1_21]	GPMC_A5	V15	AM335X_RGMII2_TXD0	22	R393	ETH1_TXD0	ETH1_TXD0	38
[GPMC_A4/GMII2_TXD1/RGMII2_TD1/RMII2_TXD1/GPMC_A20/PR1_MII1_TXD0/EQEP1A_IN/GPIO1_20]	GPMC_A4	R14	AM335X_RGMII2_TXD1	22	R391	ETH1_TXD1	ETH1_TXD1	38
[GPMC_A3/GMII2_TXD2/RGMII2_TD2/MMC2_DAT2/GPMC_A19/PR1_MII1_TXD1/EHRPWM1B/GPIO1_19]	GPMC_A3	T14	AM335X_RGMII2_TXD2	22	R394	ETH1_TXD2	ETH1_TXD2	38
[GPMC_A2/GMII2_TXD3/RGMII2_TD3/MMC2_DAT1/GPMC_A18/PR1_MII1_TXD2/EHRPWM1A/GPIO1_18]	GPMC_A2	U14	AM335X_RGMII2_TXD3	22	R395	ETH1_TXD3	ETH1_TXD3	38
[GPMC_A7/GMII2_RXCLK/RGMII2_RCLK/MMC2_DAT5/GPMC_A23/PR1_MII1_RXD1/EQEP1_STROBE/GPIO1_23]	GPMC_A7	T15	AM335X_RGMII2_RXC	38				
[GPMC_A1/GMII2_RXDV/RGMII2_RCTL/MMC2_DAT0/GPMC_A17/PR1_MII1_TXD3/EHRPWM0_SYNCO/GPIO1_17]	GPMC_A1	V14	AM335X_RGMII2_RXCTL	38				
[GPMC_A8/GMII2_RXD3/RGMII2_RD3/MMC2_DAT6/GPMC_A24/PR1_MII1_RXD0/MCASP0_ACLKX/GPIO1_24]	GPMC_A8	V16	AM335X_RGMII2_RXD3	38				
[GPMC_A9/GMII2_RXD2/RGMII2_RD2/MMC2_DAT7/GPMC_A25/PR1_MII_MR1_CLK/MCASP0_FSX/GPIO1_25]	GPMC_A9	U16	AM335X_RGMII2_RXD2	38				
[GPMC_A10/GMII2_RXD1/RGMII2_RD1/RMII2_RXD1/GPMC_A26/PR1_MII1_RXDV/MCASP0_AXR0/GPIO1_26]	GPMC_A10	T16	AM335X_RGMII2_RXD1	38				
[GPMC_A11/GMII2_RXD0/RGMII2_RD0/RMII2_RXD0/GPMC_A27/PR1_MII1_RXER/MCASP0_AXR1/GPIO1_27]	GPMC_A11	V17	AM335X_RGMII2_RXD0	38				
[MDIO_CLK/TIMER5/UART5_TXD/UART3_RTSN/MMC0_SDWP/MMC1_CLK/MMC2_CLK/GPIO0_1]	MDIO_CLK	M18	AM335X_GMII1_MDIO_CLK	37,38				
[MDIO_DATA/TIMER6/UART5_RXD/UART3_CTSN/MMC0_SDCD/MMC1_CMD/MMC2_CMD/GPIO0_0]	MDIO_DATA	M17	AM335X_GMII1_MDIO_DATA	37,38				

AM335X_15x15

SPECTRUM DIGITAL INCORPORATED			
Title: TIDEP0059 AM335X DATA CONCENTRATOR			
Page Contents: AM335X ETHERNET INTERFACES			
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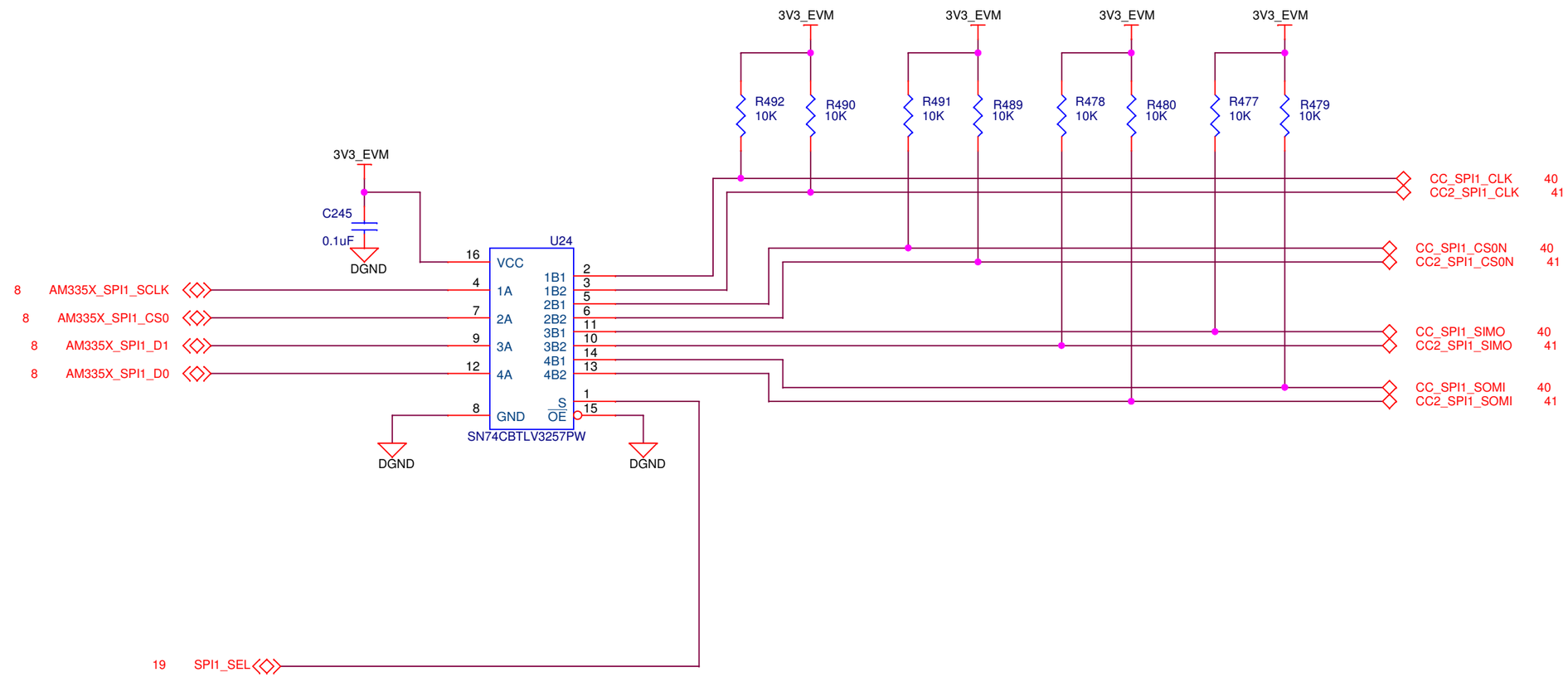
Date: Friday, June 21, 2013		Sheet 8 of 51	



3V3_EVM

3V3_EVM 3V3_EVM 5,6,11,18,19,21,23,25,26,27,28,29,30,31,32,33,37,38,40,41,42

SPECTRUM DIGITAL INCORPORATED		
Title: TIDEP0059 AM335X DATA CONCENTRATOR		
Page Contents: SPI 1 MUXING		
Size:B	DWG NO 516882-0001	Revision: B
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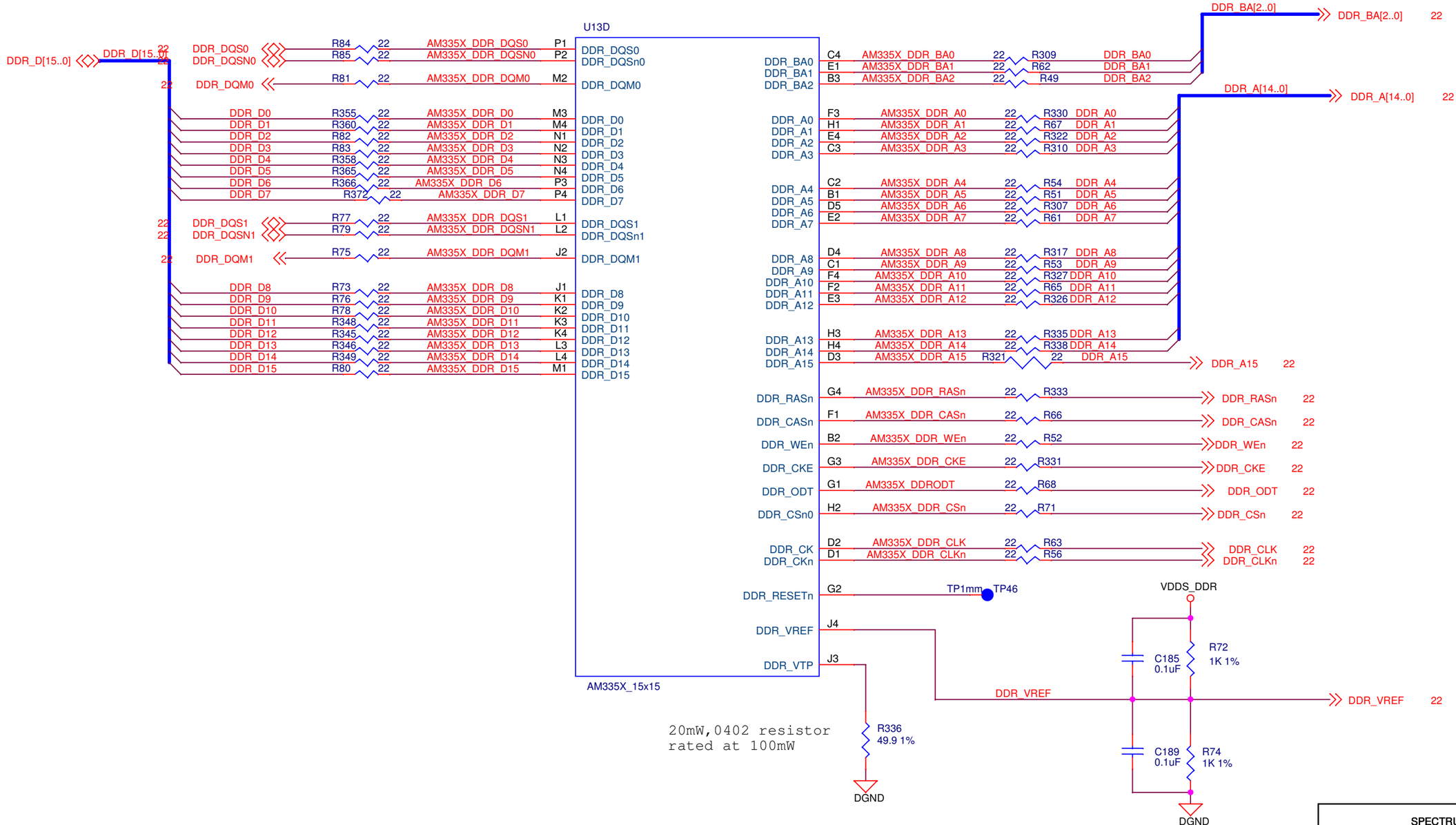

SPECTRUM DIGITAL INCORPORATED		
Title: TIDEP0059 AM335X DATA CONCENTRATOR		
Page Contents: AM335X DDR INTERFACE		
Size:B	DWG NO 516882-0001	Revision: B
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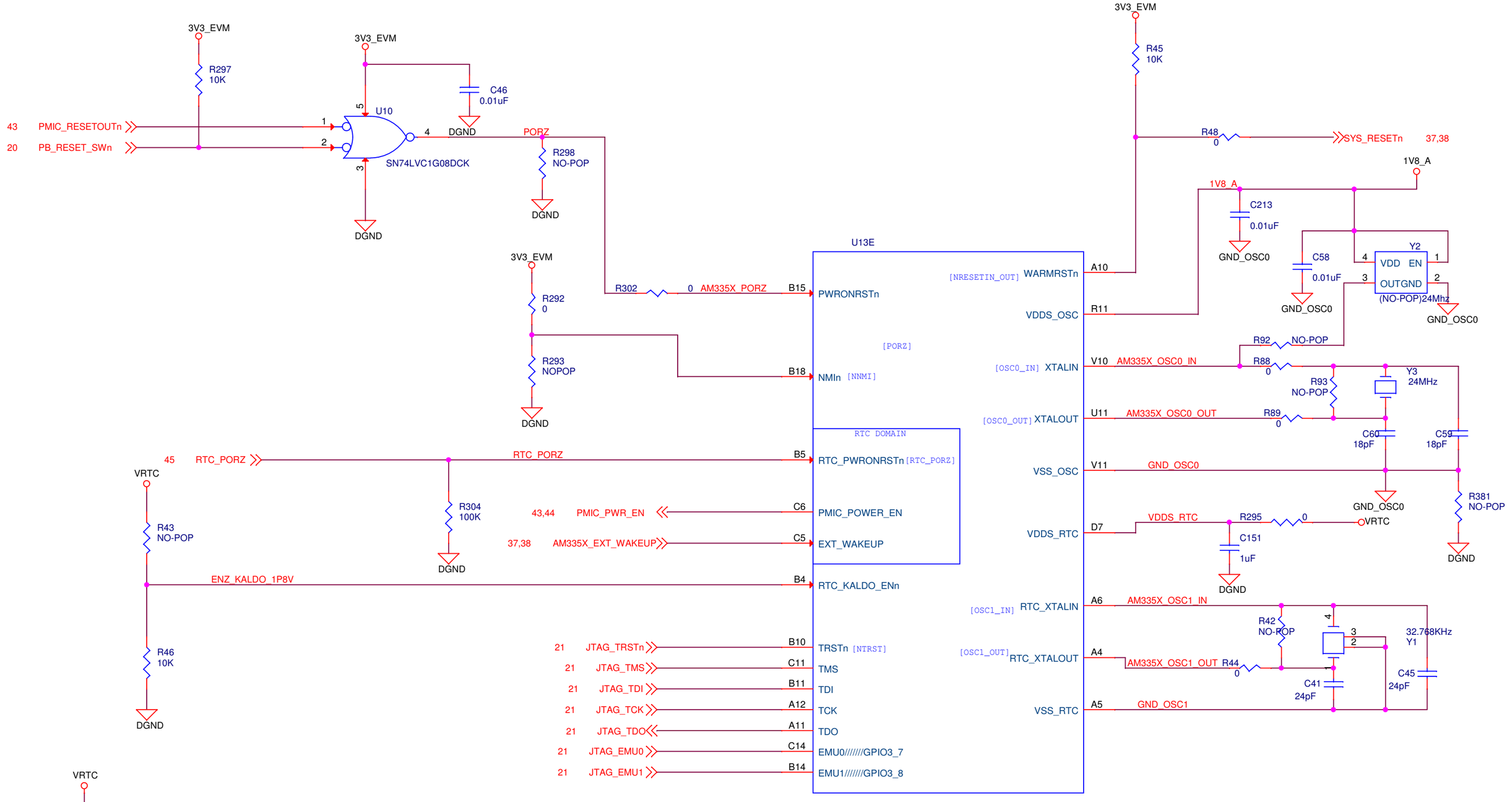

SPECTRUM DIGITAL INCORPORATED		
Title: TIDEP0059 AM335X DATA CONCENTRATOR		
Page Contents: AM335X JTAG, RESET, CLOCKS		
Size:B	DWG NO 516882-0001	Revision: B
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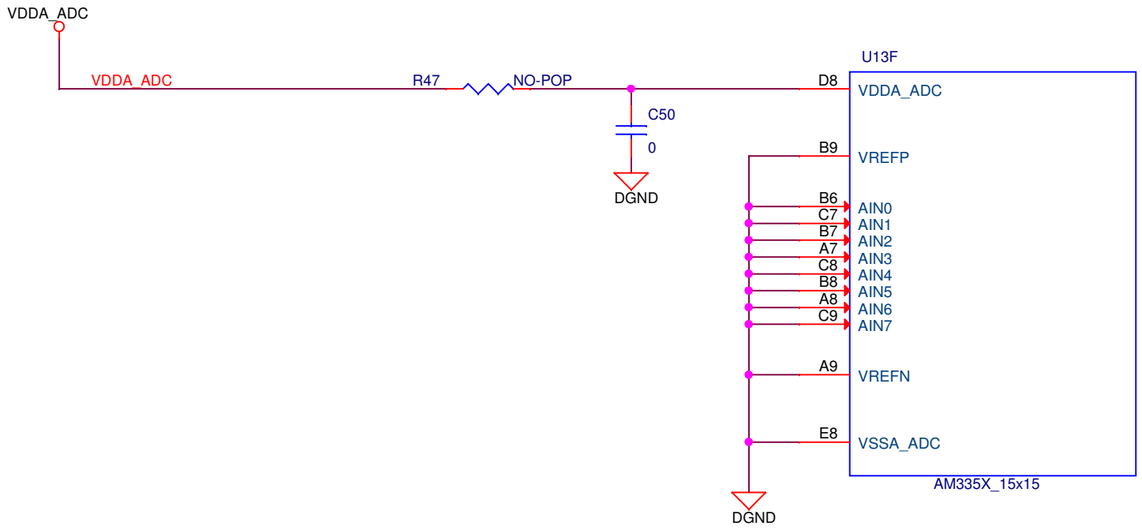
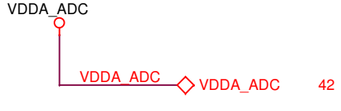
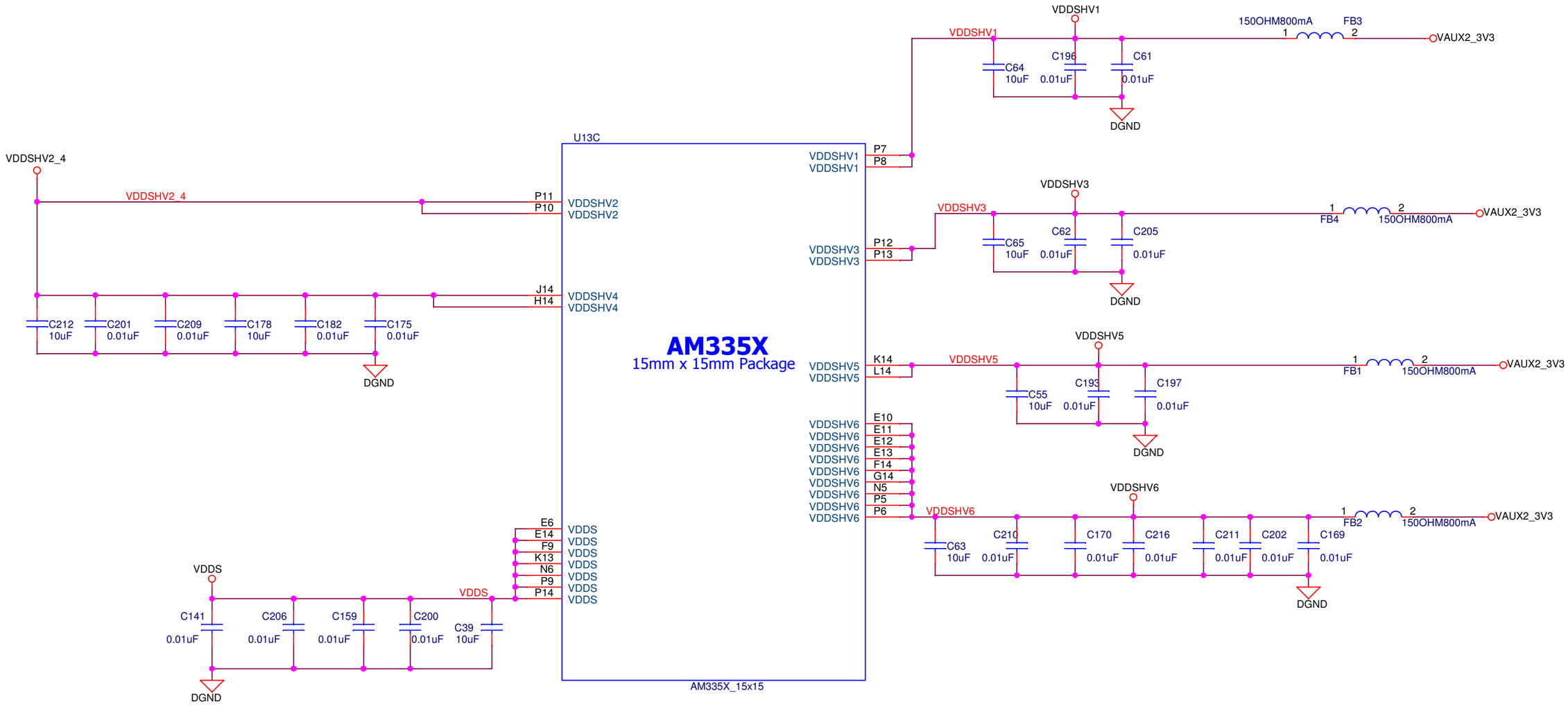




SPECTRUM DIGITAL INCORPORATED		
Title: TIDEP0059 AM335X DATA CONCENTRATOR		
Page Contents: AM335X ADC INTERFACE		
Size:B	DWG NO 516882-0001	Revision: B
Date: Friday, June 21, 2013	Sheet 12 of 51	



VAUX2_3V3
VAUX2_3V3 VAUX2_3V3 42

VDDSHV2_4
VDDSHV2_4 VDDSHV2_4 42

VDDS
VDDS VDDS 42

SPECTRUM DIGITAL INCORPORATED		
Title: TIDEP0059 AM335X DATA CONCENTRATOR		
Page Contents: AM335X I/O POWER		
Size:B	DWG NO 516882-0001	Revision: B
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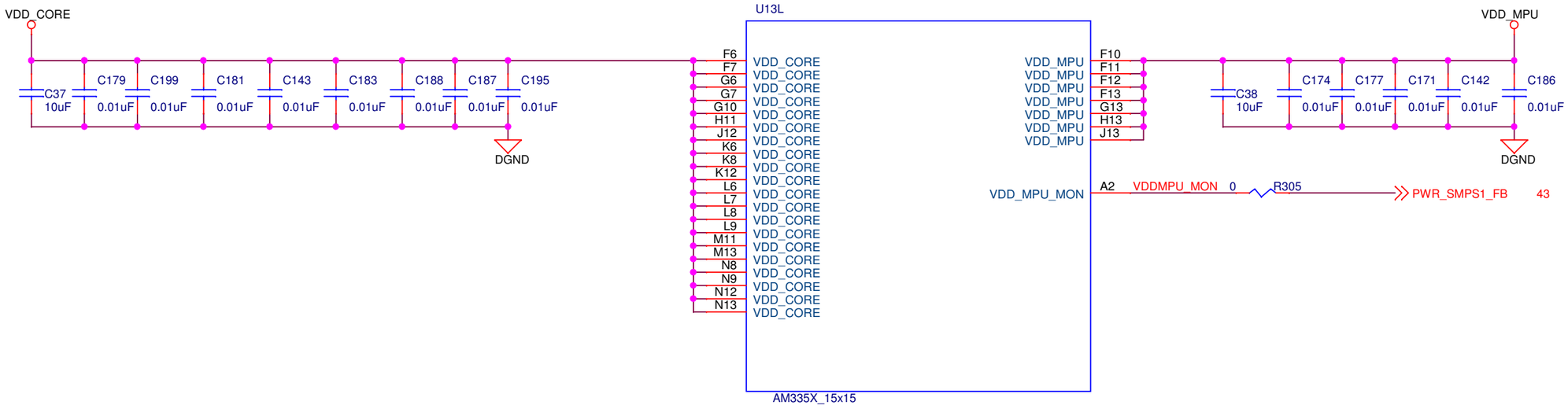

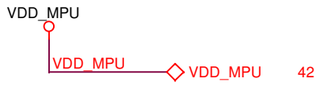

SPECTRUM DIGITAL INCORPORATED		
Title: TIDEP0059 AM335X DATA CONCENTRATOR		
Page Contents: AM335X CORE POWER		
Size:B	DWG NO 516882-0001	Revision: B
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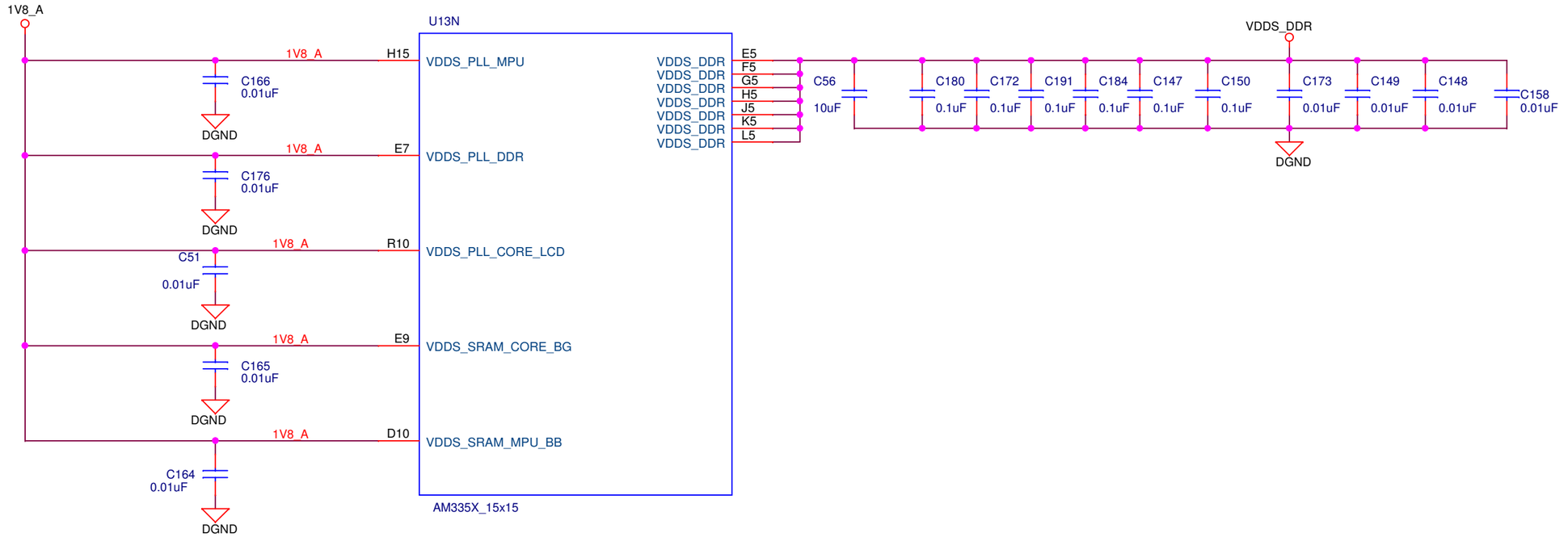

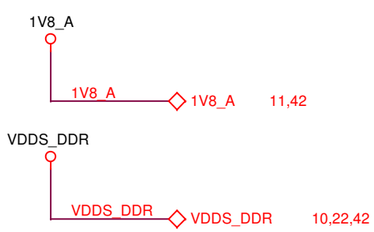

SPECTRUM DIGITAL INCORPORATED		
Title: TIDEP0059 AM335X DATA CONCENTRATOR		
Page Contents: AM335X DDR / PLL POWER		
Size:B	DWG NO 516882-0001	Revision: B
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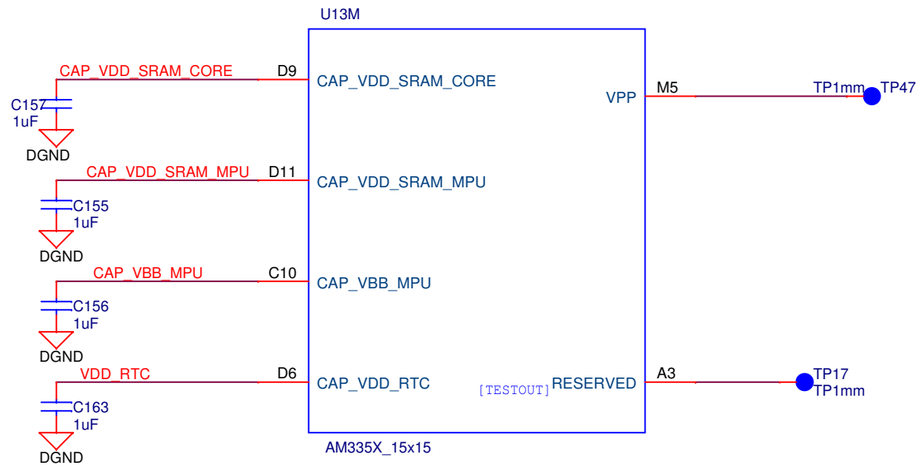

SPECTRUM DIGITAL INCORPORATED		
Title: TIDEP0059 AM335X DATA CONCENTRATOR		
Page Contents: AM335X LDO'S		
Size:B	DWG NO 516882-0001	Revision: B
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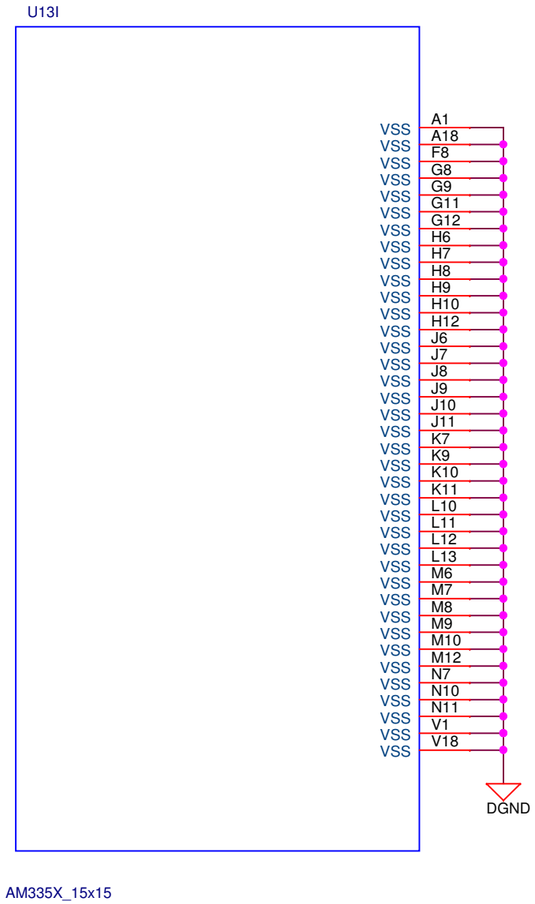

SPECTRUM DIGITAL INCORPORATED		
Title: TIDEP0059 AM335X DATA CONCENTRATOR		
Page Contents: AM335X GROUND PINS		
Size:B	DWG NO 516882-0001	Revision: B
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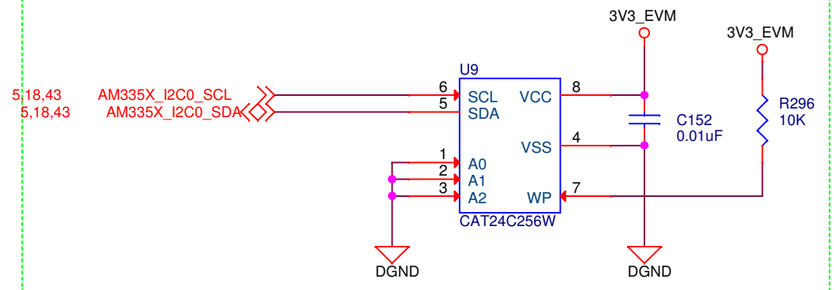
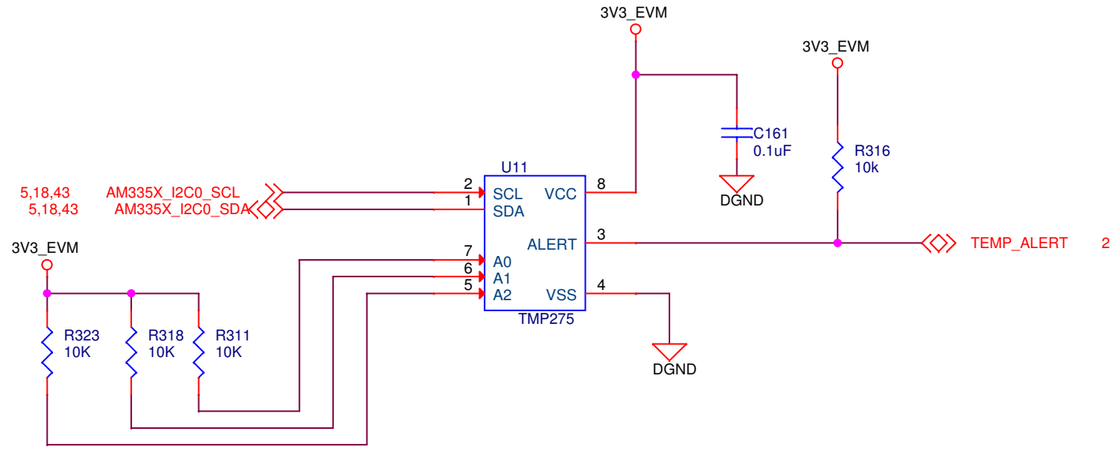
ID Memory





SPECTRUM DIGITAL INCORPORATED		
Title: TIDEP0059 AM335X DATA CONCENTRATOR		
Page Contents: AM335X I2C PERIPHERALS		
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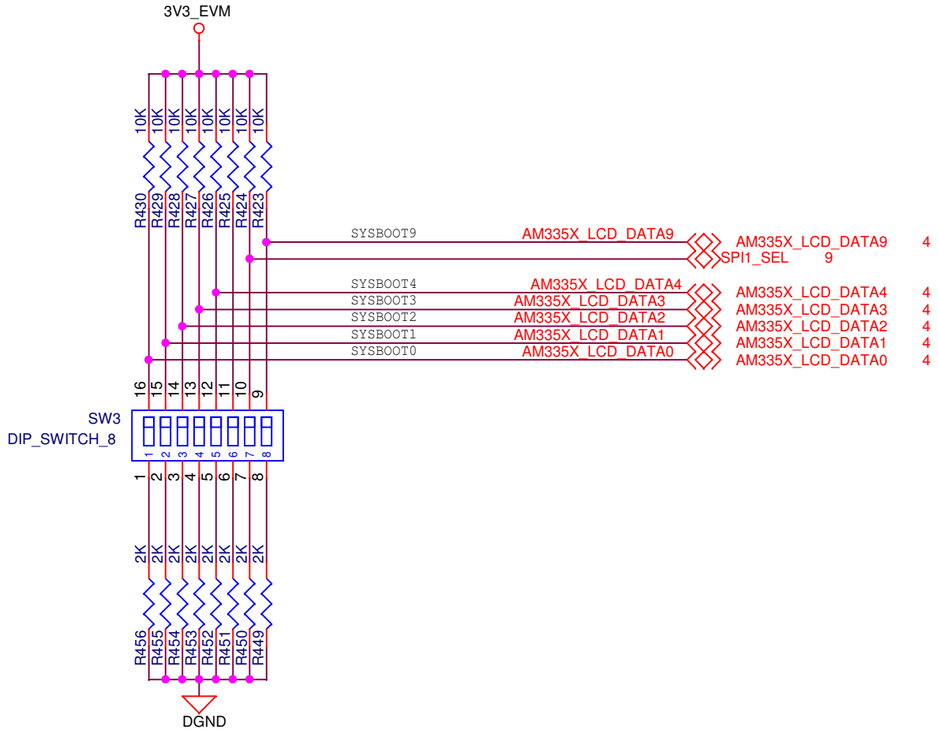
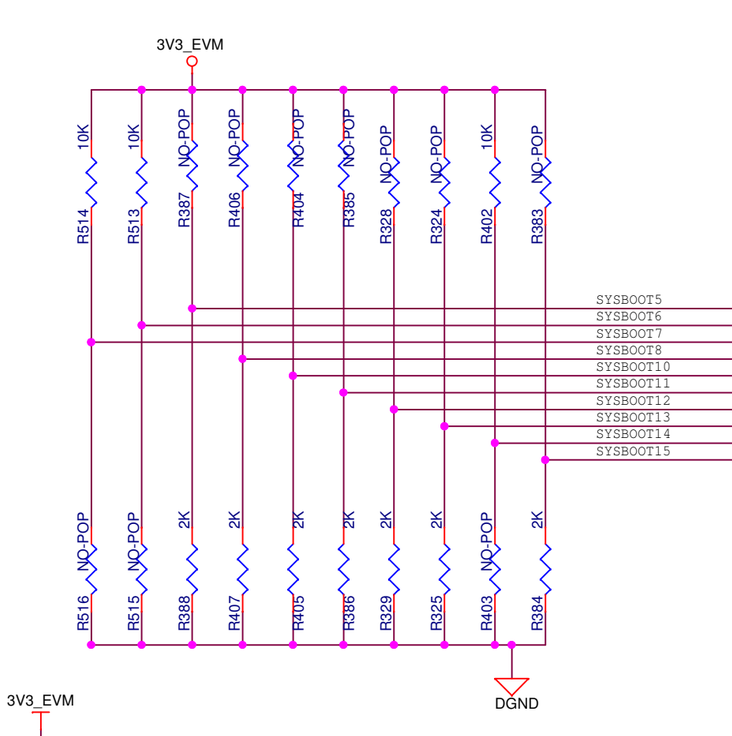
Boot Configuration





SYSBOOT[15:14] - can be fixed to 01b (24MHz)

SYSBOOT[13:12] - can be fixed to 00b (must be set to 00b per documentation)

SYSBOOT[11:10] - can be fixed to 00b (don't support XIP boot on this board and for NAND boot these pins must be set to 00b)

SYSBOOT[9] - keep configurable (controls use of ECC in ROM)

SYSBOOT[8] - can be fixed to 0b (8-bit NAND)

SYSBOOT[7:6] - SYSBOOT[7:6] can be fixed since we only support RGMII)

SYSBOOT[5] - fix to 0 (want CLKOUT1 disabled to avoid conflict with JTAG)

SYSBOOT[4:0] - keep configurable

SPECTRUM DIGITAL INCORPORATED		
Title: TIDEP0059 AM335X DATA CONCENTRATOR		
Page Contents: AM335X BOOT SWITCHES		
Size:B	DWG NO 516882-0001	Revision: B
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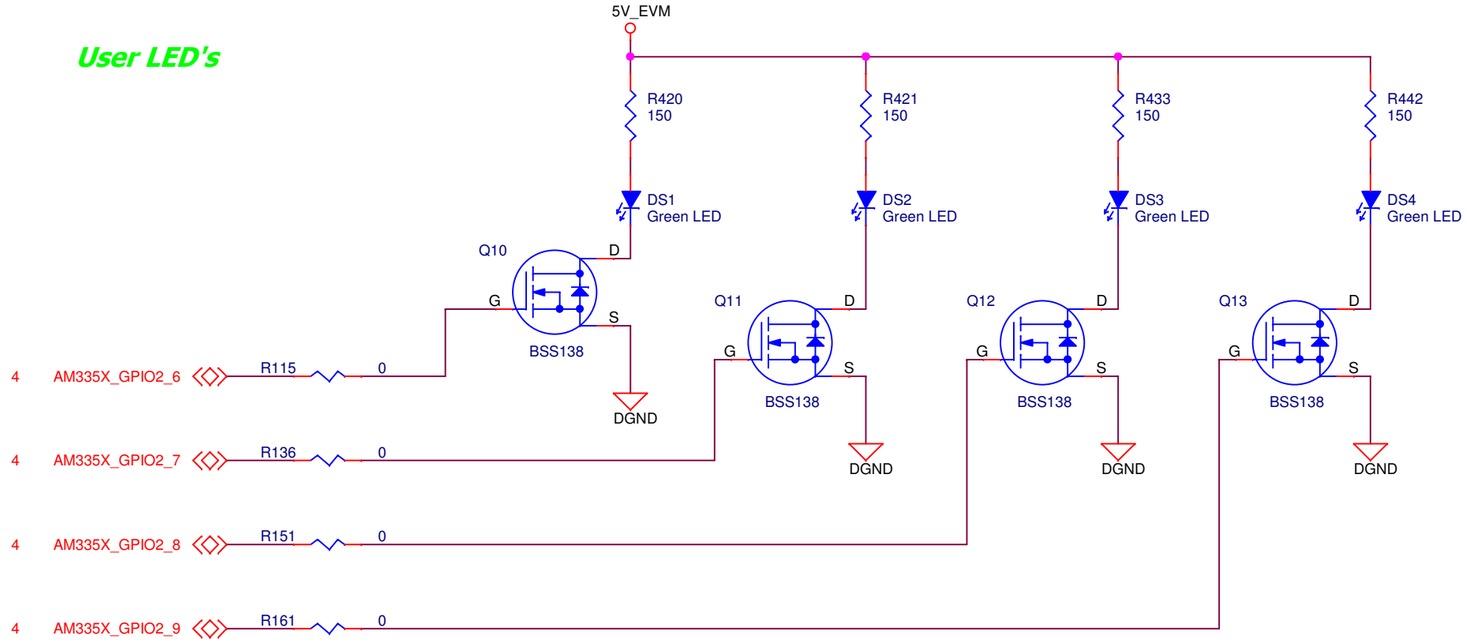
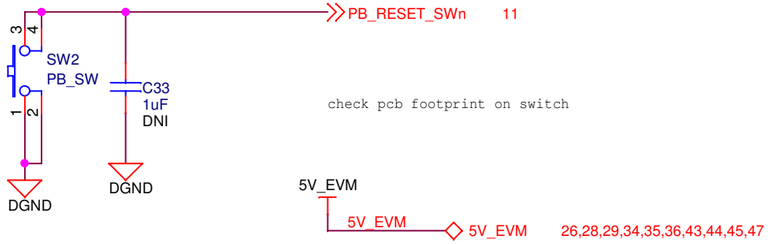
User LED's



User Reset Switches



SPECTRUM DIGITAL INCORPORATED		
Title: TIDEP0059 AM335X DATA CONCENTRATOR		
Page Contents: AM335X LEDS, USER SWITCHES		
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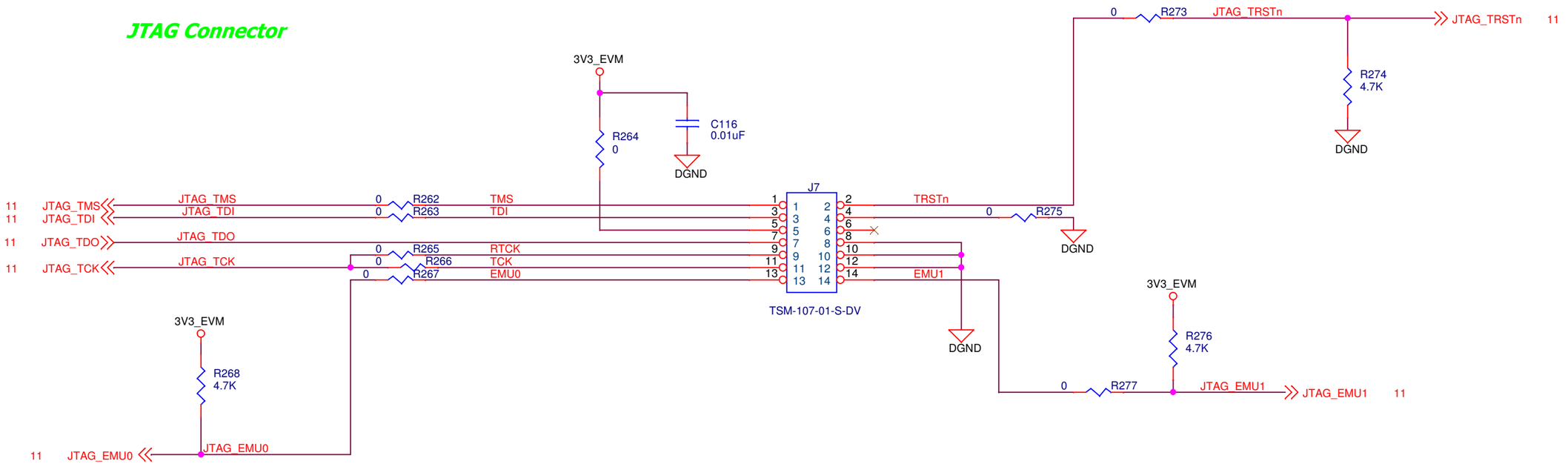
JTAG Connector



SPECTRUM DIGITAL INCORPORATED		
Title: TIDEP0059 AM335X DATA CONCENTRATOR		
Page Contents: JTAG CONNECTOR		
Size:B	DWG NO 516882-0001	Revision: B
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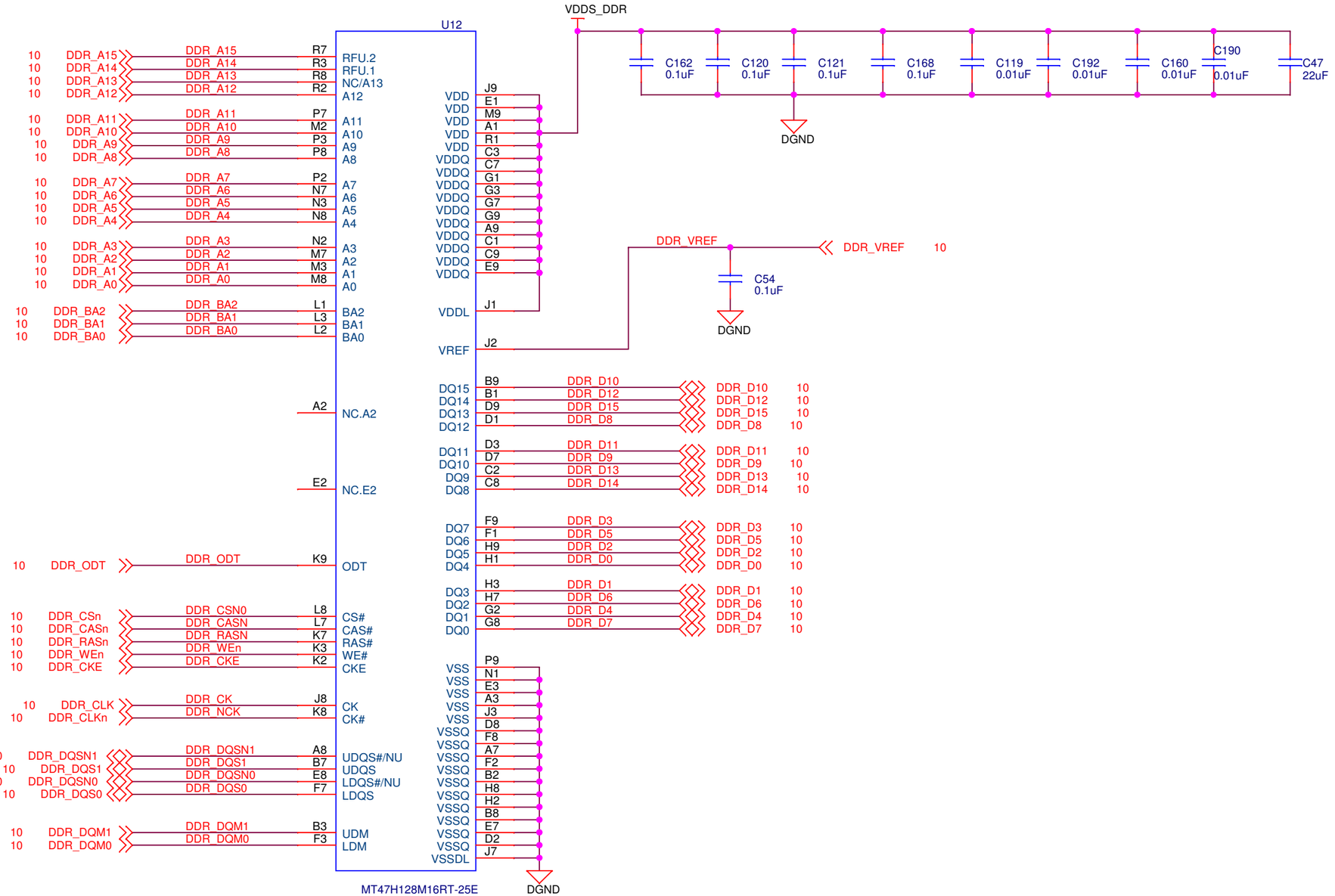

DDR2 SDRAM

VDDS_DDR → VDDS_DDR → VDDS_DDR 10,15,42

SPECTRUM DIGITAL INCORPORATED		
Title: TIDEP0059 AM335X DATA CONCENTRATOR		
Page Contents: DDR2 MEMORY		
Size:B	DWG NO 516882-0001	Revision: B
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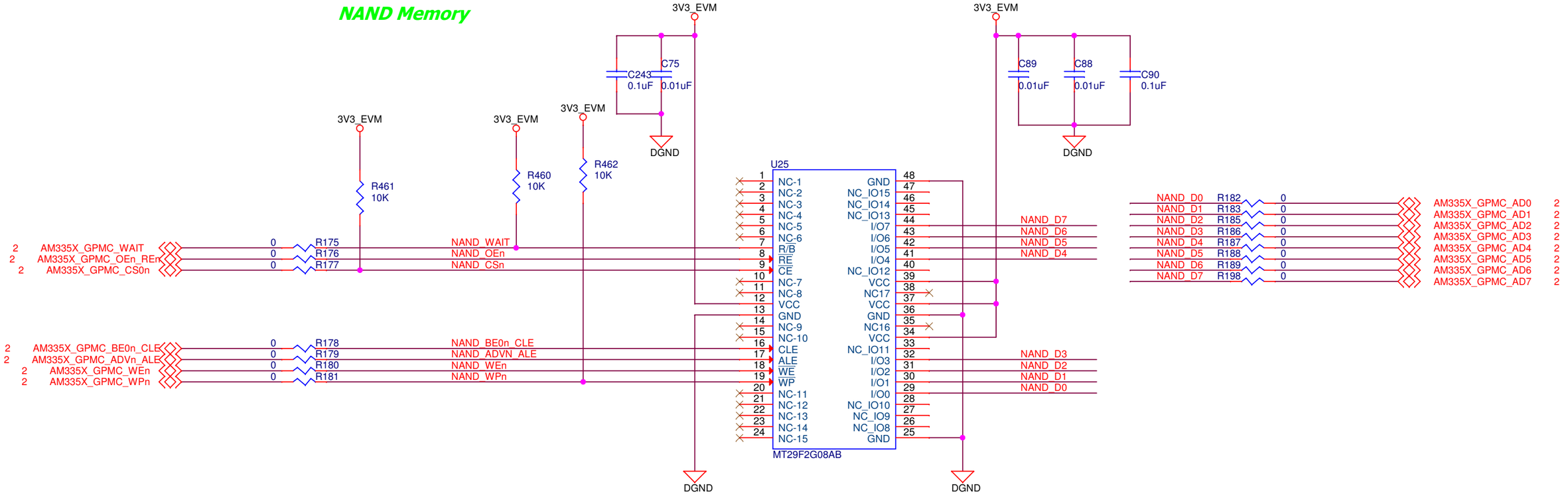
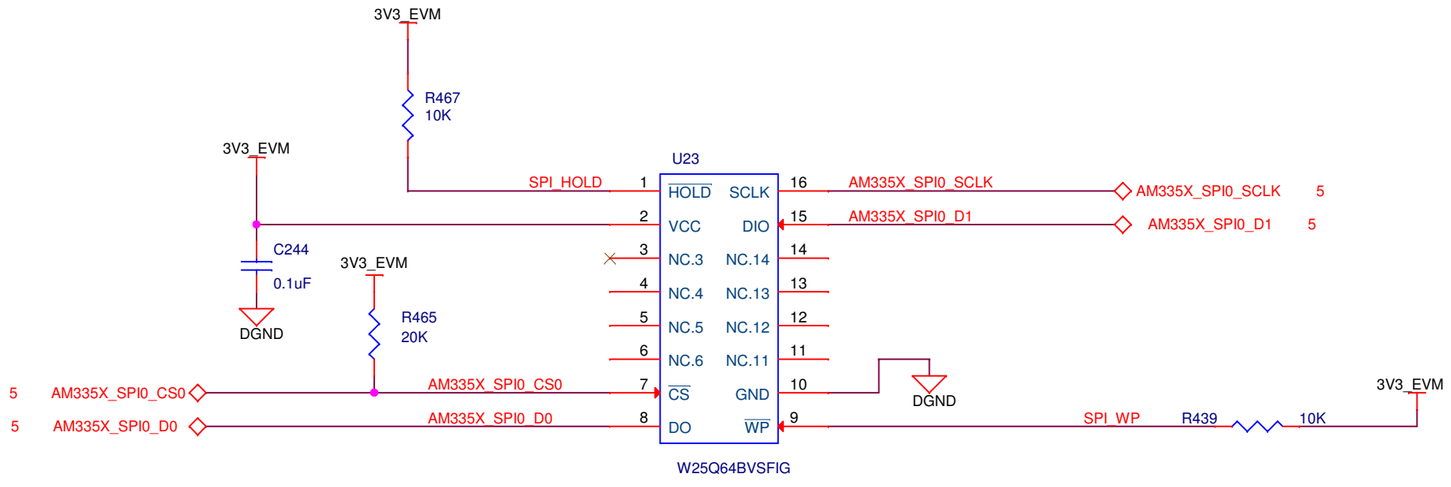
NAND Memory





3V3_EVM 3V3_EVM 5,6,9,11,18,19,21,25,26,27,28,29,30,31,32,33,37,38,40,41,42

SPECTRUM DIGITAL INCORPORATED		
Title: TIDEP0059 AM335X DATA CONCENTRATOR		
Page Contents: NAND/SPI FLASH		
Size:B	DWG NO 516882-0001	Revision: B
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25,48 LINE_AC_N

JP4
HDR_2_P1_INCH

LINE_N_F

25,48 LINE_AC_A

JP3
HDR_2_P1_INCH

C5
.47uF 400v(ECQ-E4474KF

JP20
HEADER 3

L16 15uH
L17 600nH

LINE_AC_A_CON

P1
1777574

JP5
HDR_2_P1_INCH

T1
WURTH_750510476

GND_AC_PWR

LINE_COMB

LINE_N_F

25 LINE_AC_B

JP1
HDR_2_P1_INCH

C1
.47uF 400v(ECQ-E4474KF

JP21
HEADER 3

L14 15uH
L15 600nH

LINE_AC_B_CON

Note Board Markings required

HAZZARD MARKING

CURRENT AND VOLTAGE MARKINGS

25 LINE_AC_C

JP2
HDR_2_P1_INCH

C2
.47uF 400v(ECQ-E4474KF

JP22
HEADER 3

L12 15uH
L13 600nH

LINE_AC_C_CON

SD PART# 103531-0001R

PL_TXRX PL_TXRX 26

D10
SM6T7V5CA

GND_AC_PWR

R17
4.7

C25
2200PF 250V

GND_AC_PWR

TP7
Test Point_0

GND_AC_PWR

TP10
Test Point_0

GND_AC_PWR

SPECTRUM DIGITAL INCORPORATED		
Title: TIDEP0059 AM335X DATA CONCENTRATOR		
Page Contents: PLC SOM INTERFACE		
Size:B	DWG NO 516882-0001	Revision: C
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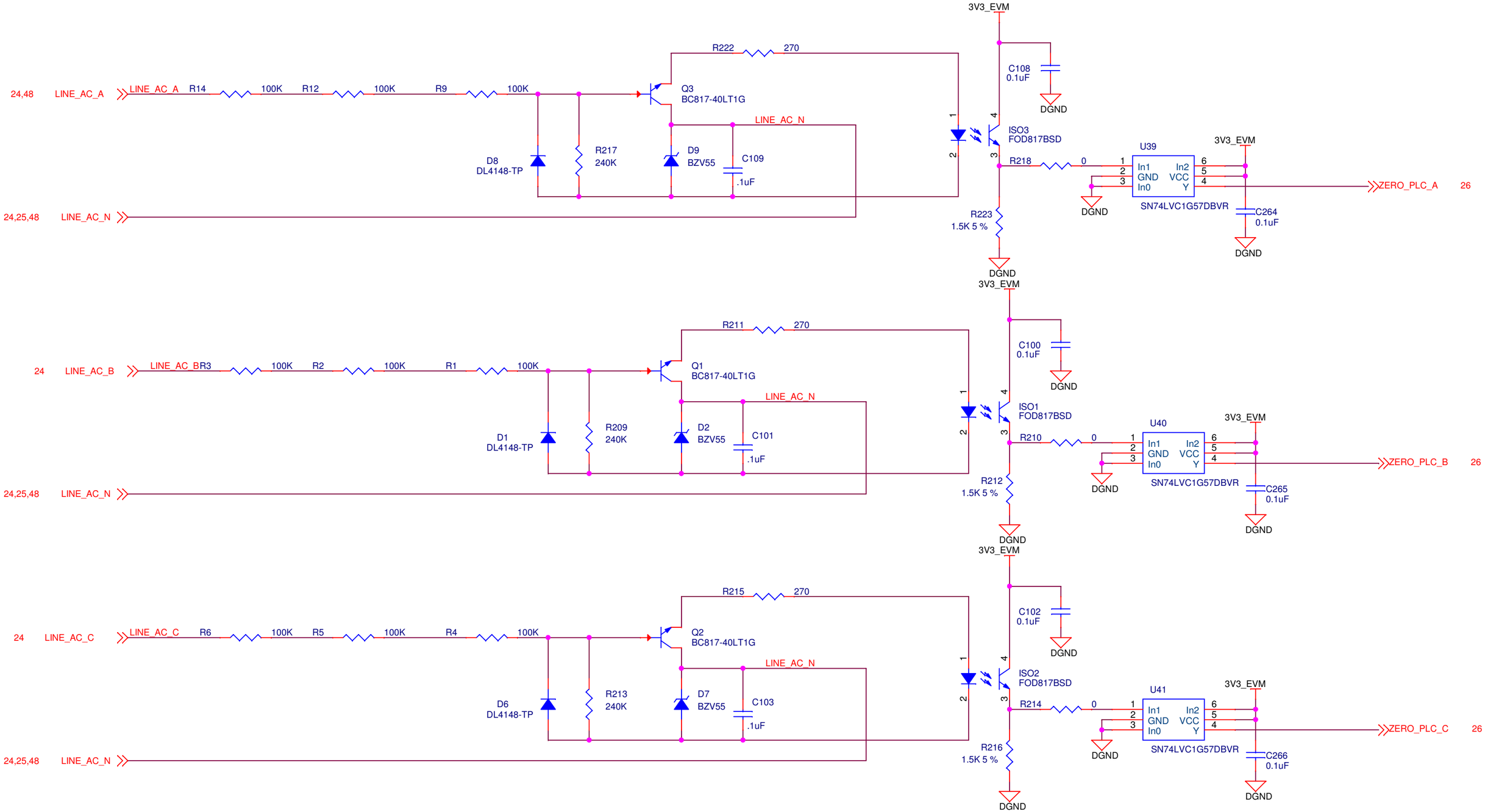
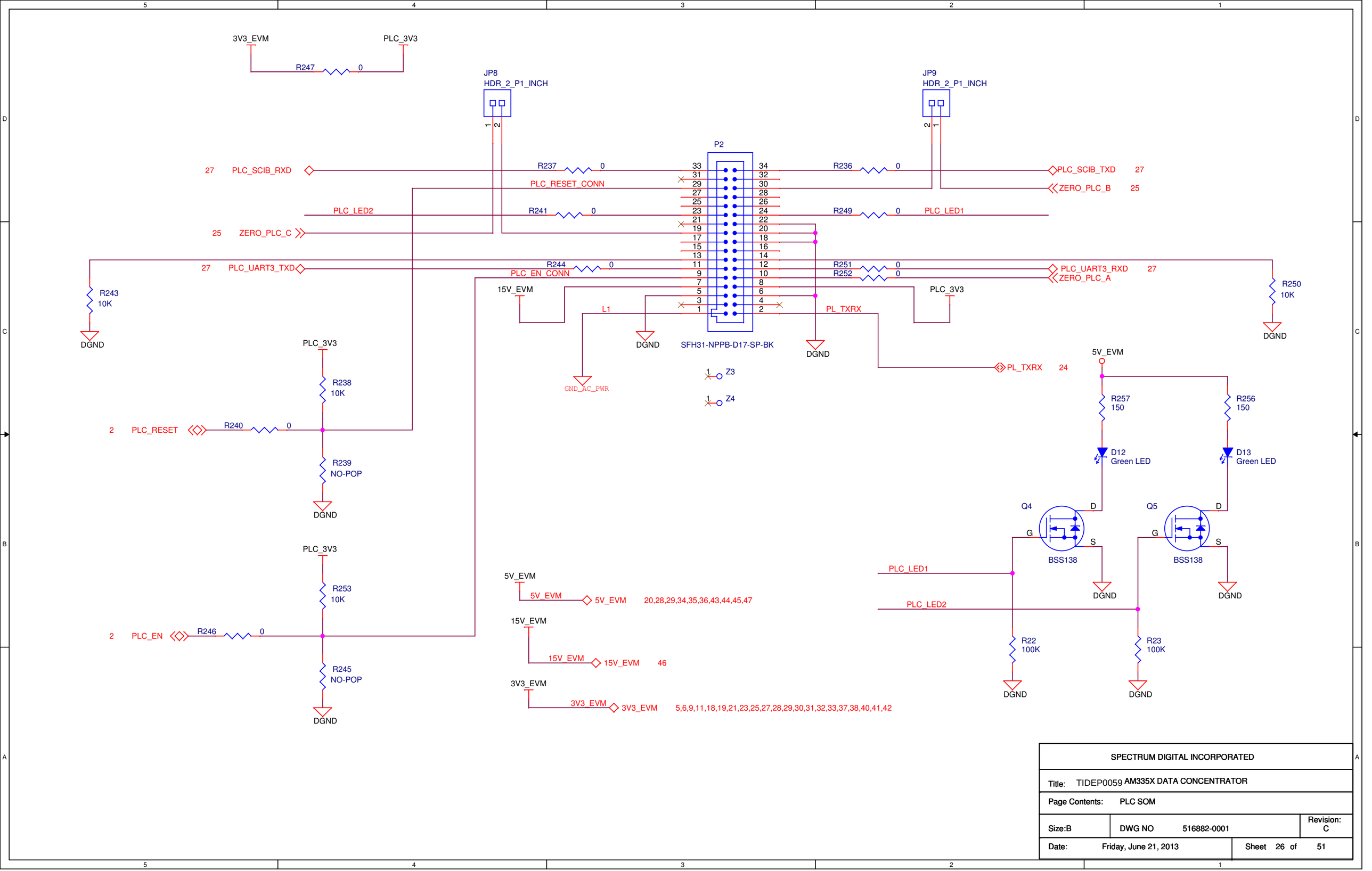


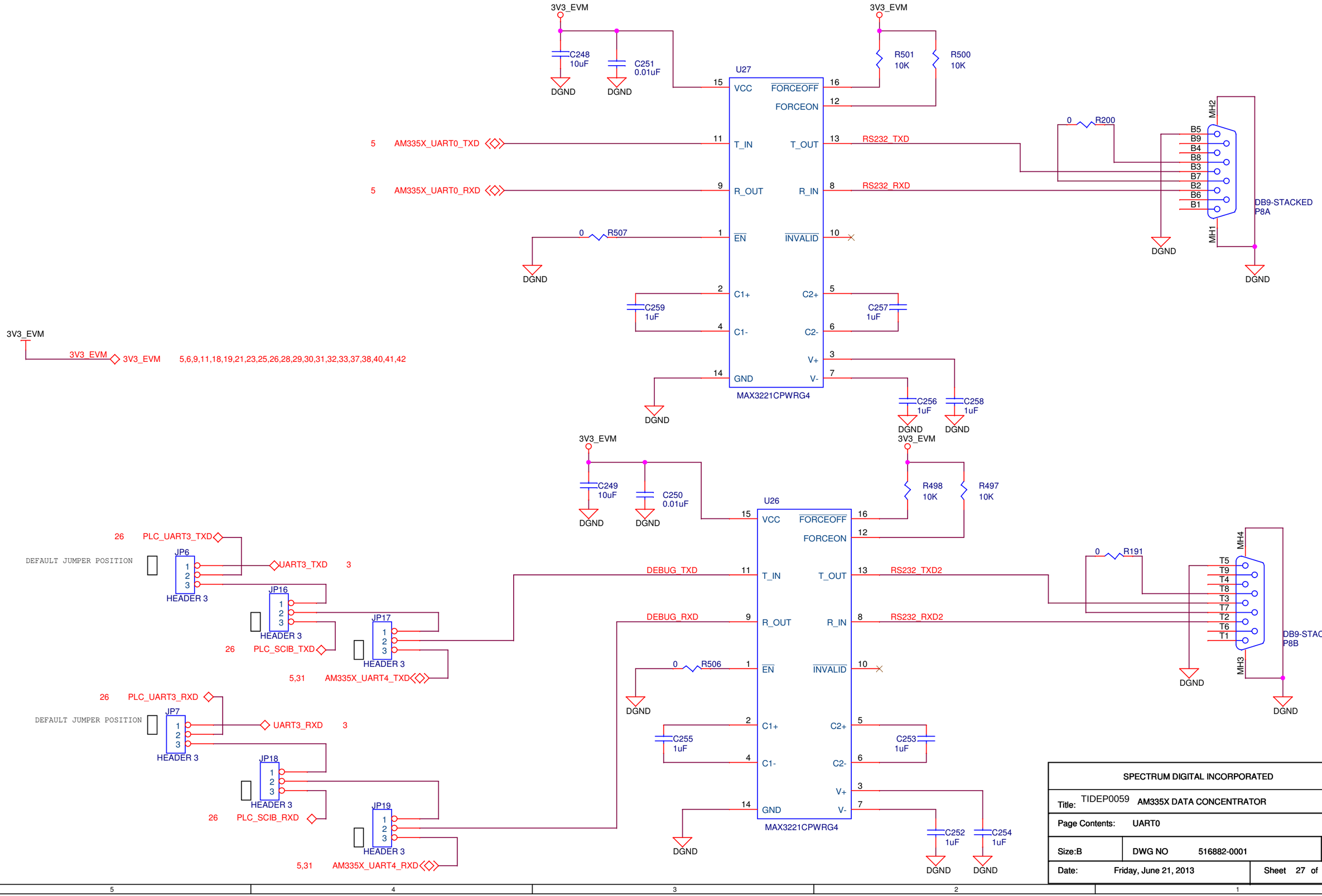
3V3_EVM

3V3_EVM ◇ 3V3_EVM 5,6,9,11,18,19,21,23,26,27,28,29,30,31,32,33,37,38,40,41,42

SPECTRUM DIGITAL INCORPORATED		
Title: TIDEP0059 AM335X DATA CONCENTRATOR		
Page Contents: ZERO CROSSING DETECTOR		
Size:B	DWG NO 516882-0001	Revision: C
Date: Friday, June 21, 2013	Sheet 25 of 51	



SPECTRUM DIGITAL INCORPORATED		
Title: TIDEP0059 AM335X DATA CONCENTRATOR		
Page Contents: PLC SOM		
Size:B	DWG NO 516882-0001	Revision: C
Date: Friday, June 21, 2013	Sheet 26 of 51	


3V3_EVM
C248
10uF
DGND
C251
0.01uF
DGND
U27
15
VCC
16
FORCEOFF
12
FORCEON
3V3_EVM
R501
10K
R500
10K
5
AM335X_UART0_TXD
11
T_IN
13
T_OUT
RS232_TXD
0
R200
MH2
B5
B9
B4
B8
B3
B7
B2
B6
B1
MH1
DB9-STACKED
P8A
DGND
5
AM335X_UART0_RXD
9
R_OUT
8
R_IN
RS232_RXD
0
R507
1
EN
10
INVALID
DGND
DGND
2
C1+
5
C2+
C259
1uF
C257
1uF
4
C1-
6
C2-
3V3_EVM
3V3_EVM
3V3_EVM
5,6,9,11,18,19,21,23,25,26,28,29,30,31,32,33,37,38,40,41,42
V+
3
14
GND
7
V-
MAX3221CPWRG4
C256
1uF
C258
1uF
DGND
DGND
DGND
DGND
3V3_EVM
C249
10uF
DGND
C250
0.01uF
DGND
U26
15
VCC
16
FORCEOFF
12
FORCEON
R498
10K
R497
10K
26
PLC_UART3_TXD
DEFAULT JUMPER POSITION
JP6
1
2
3
HEADER 3
UART3_TXD
3
JP16
HEADER 3
JP17
HEADER 3
26
PLC_SCIB_TXD
5,31
AM335X_UART4_TXD
DEBUG_TXD
11
T_IN
13
T_OUT
RS232_TXD2
0
R191
MH4
T5
T9
T4
T8
T3
T7
T2
T6
T1
MH3
DB9-STACKED
P8B
DGND
DGND
DEBUG_RXD
9
R_OUT
8
R_IN
RS232_RXD2
0
R506
1
EN
10
INVALID
DGND
DGND
2
C1+
5
C2+
C255
1uF
C253
1uF
4
C1-
6
C2-
V+
3
14
GND
7
V-
MAX3221CPWRG4
C252
1uF
C254
1uF
DGND
DGND
DGND
26
PLC_UART3_RXD
DEFAULT JUMPER POSITION
JP7
HEADER 3
UART3_RXD
3
JP18
HEADER 3
26
PLC_SCIB_RXD
JP19
HEADER 3
5,31
AM335X_UART4_RXD
SPECTRUM DIGITAL INCORPORATED
Title: TIDEP0059 AM335X DATA CONCENTRATOR
Page Contents: UART0
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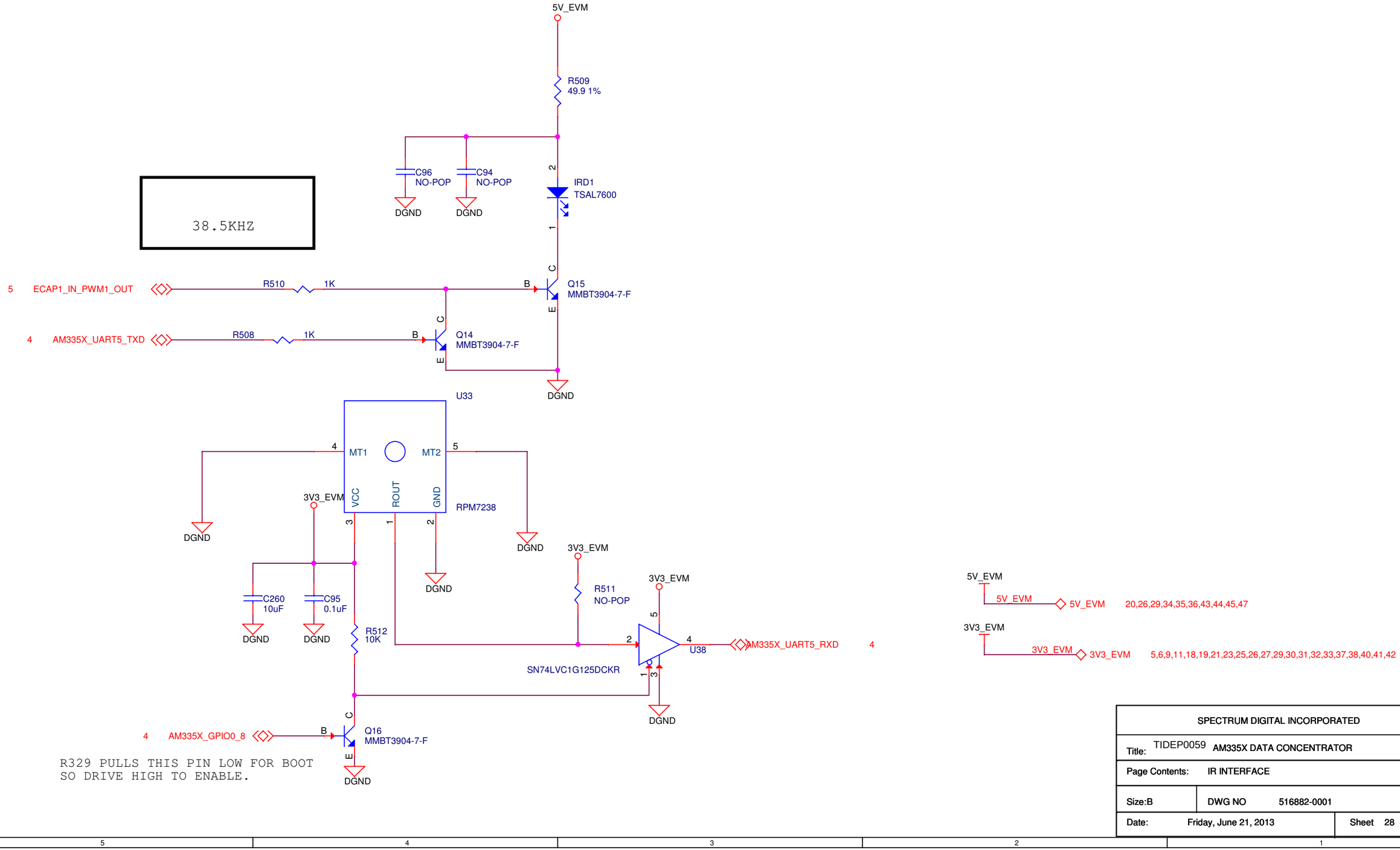
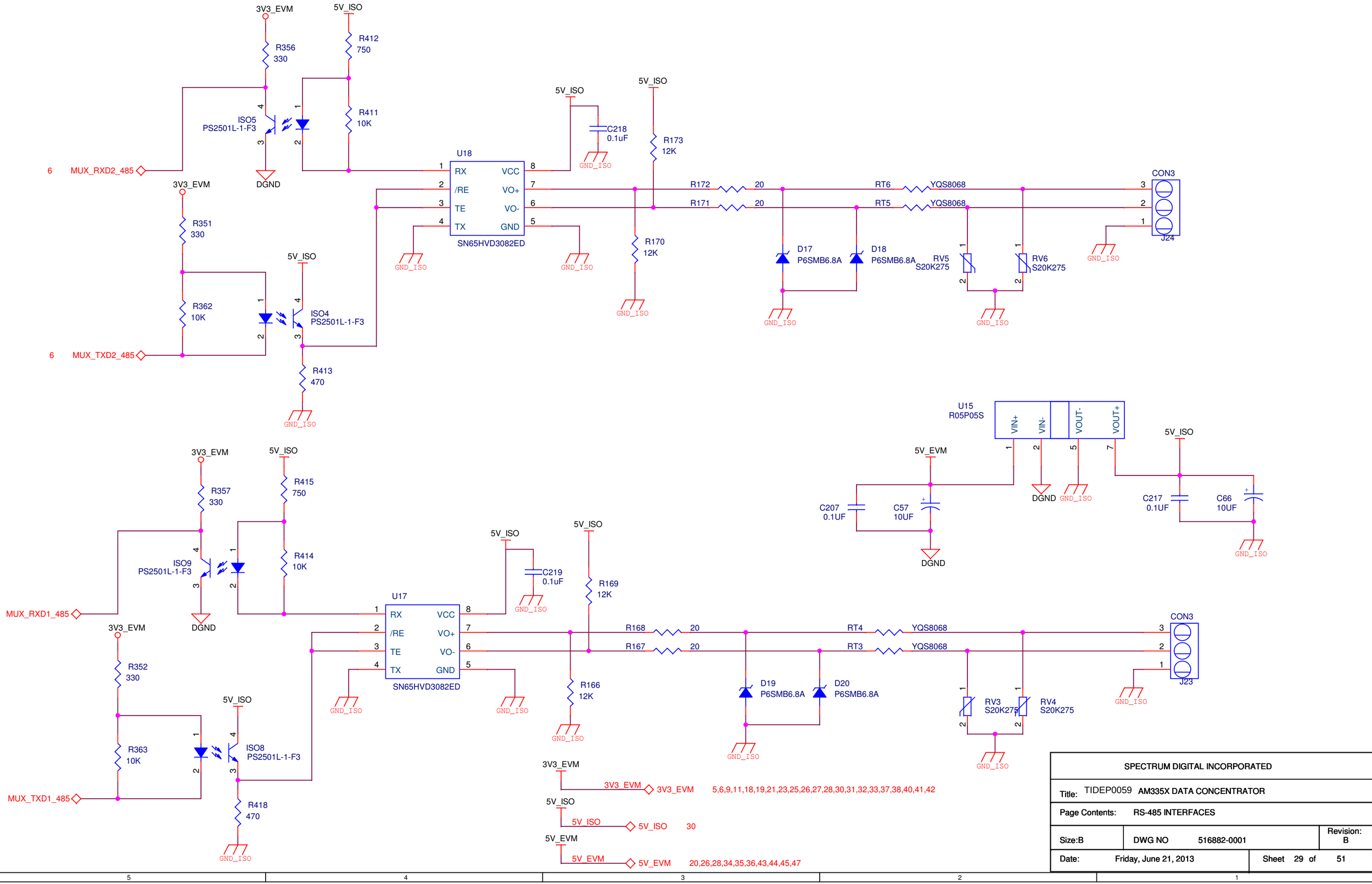
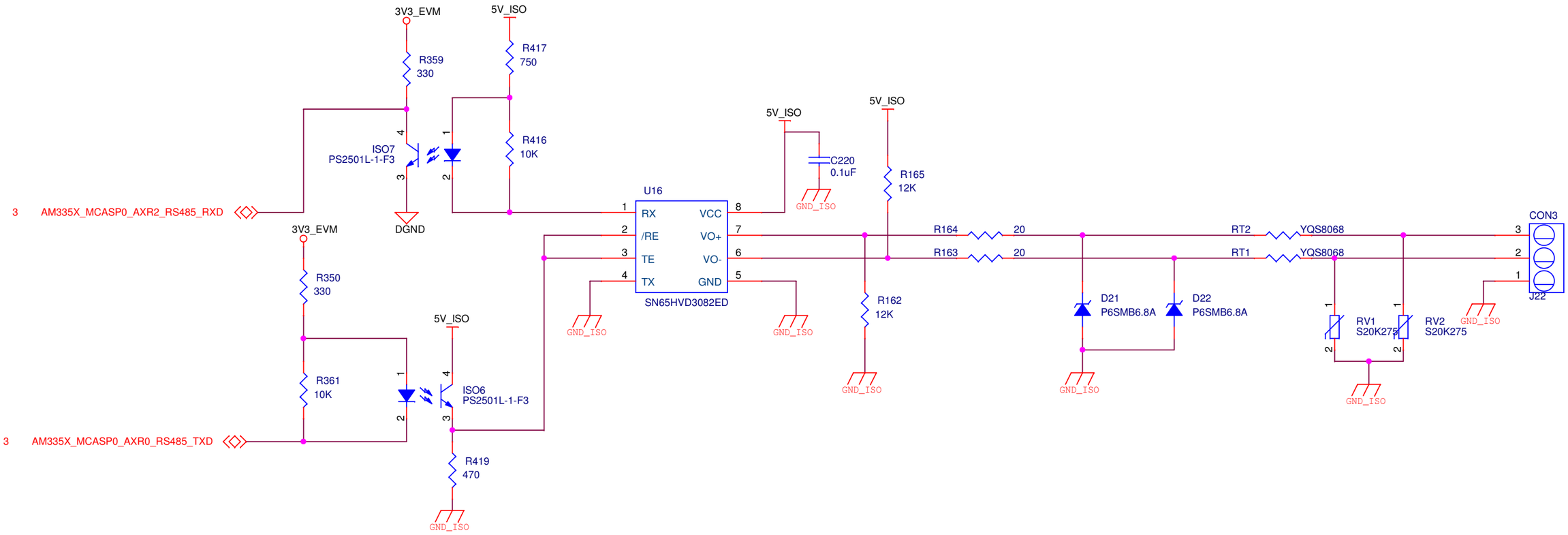


SPECTRUM DIGITAL INCORPORATED		
Title: TIDEP0059 AM335X DATA CONCENTRATOR		
Page Contents: IR INTERFACE		
Size:B	DWG NO 516882-0001	Revision: C
Date: Friday, June 21, 2013	Sheet 28 of 51	



SPECTRUM DIGITAL INCORPORATED		
Title: TIDEP0059 AM335X DATA CONCENTRATOR		
Page Contents: RS-485 INTERFACES		
Size:B	DWG NO 516882-0001	Revision: B
Date: Friday, June 21, 2013	Sheet 29 of 51	



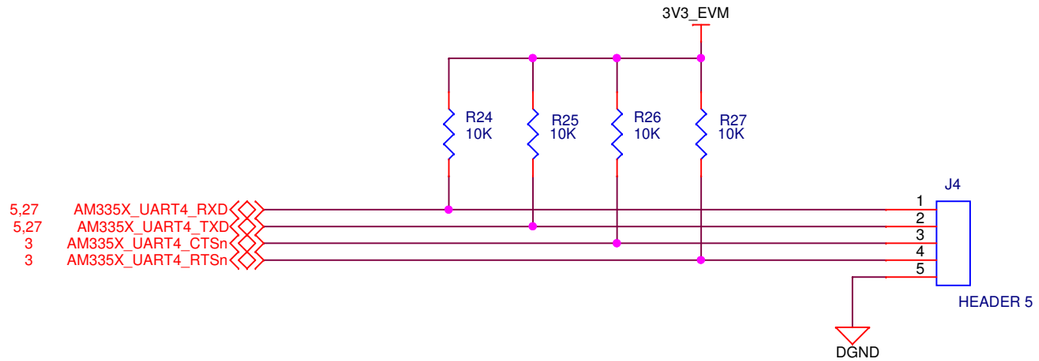
3V3_EVM

3V3_EVM 3V3_EVM 5,6,9,11,18,19,21,23,25,26,27,28,29,31,32,33,37,38,40,41,42

5V_ISO

5V_ISO 5V_ISO 29

SPECTRUM DIGITAL INCORPORATED		
Title: TIDEP0059 AM335X DATA CONCENTRATOR		
Page Contents: RS-485 INTERFACES		
Size:B	DWG NO 516882-0001	Revision: B
Date: Friday, June 21, 2013	Sheet 30 of 51	



SPECTRUM DIGITAL INCORPORATED		
Title: TIDEP0059 AM335X DATA CONCENTRATOR		
Page Contents: UART4 GPRS HEADER		
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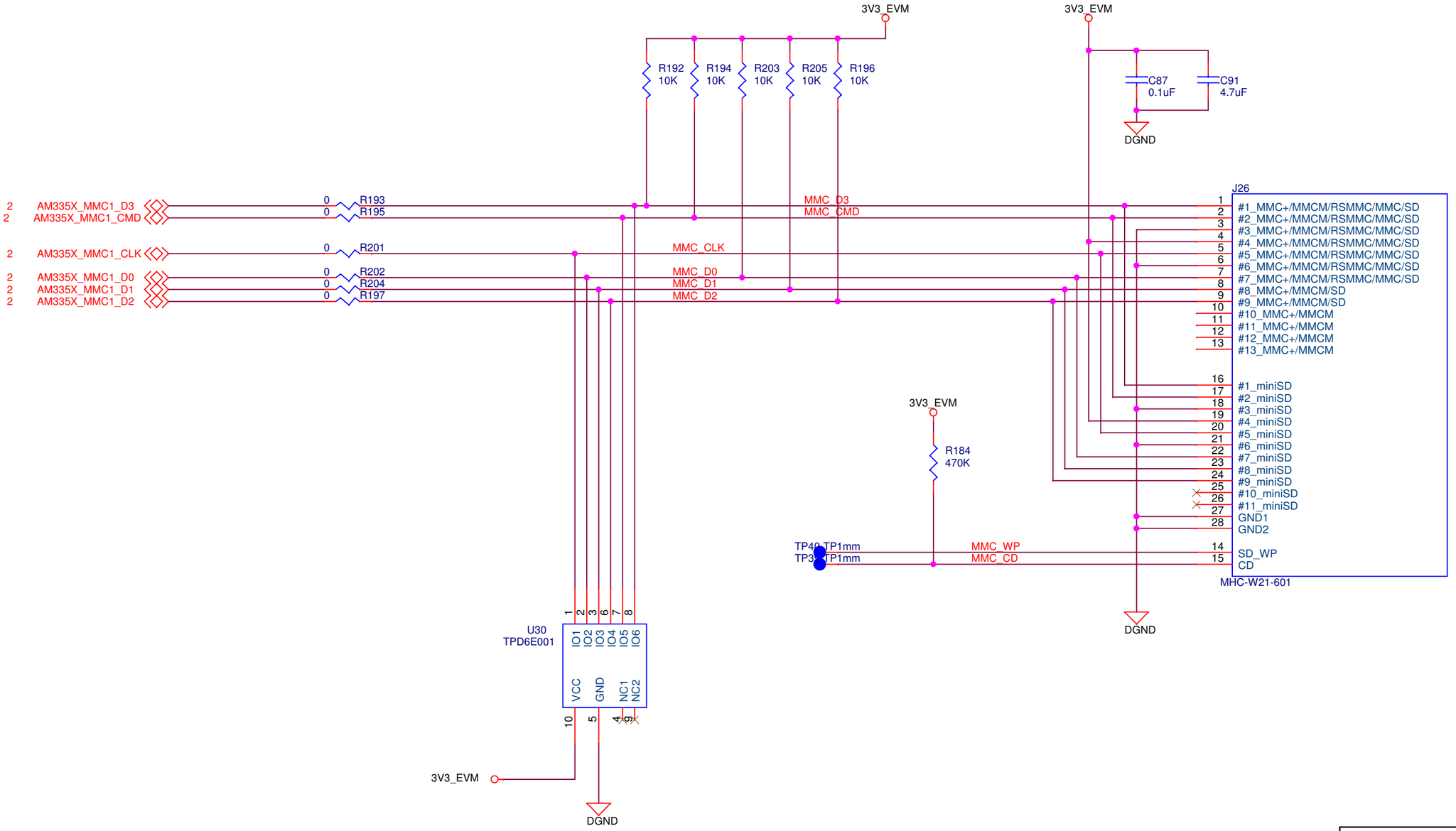
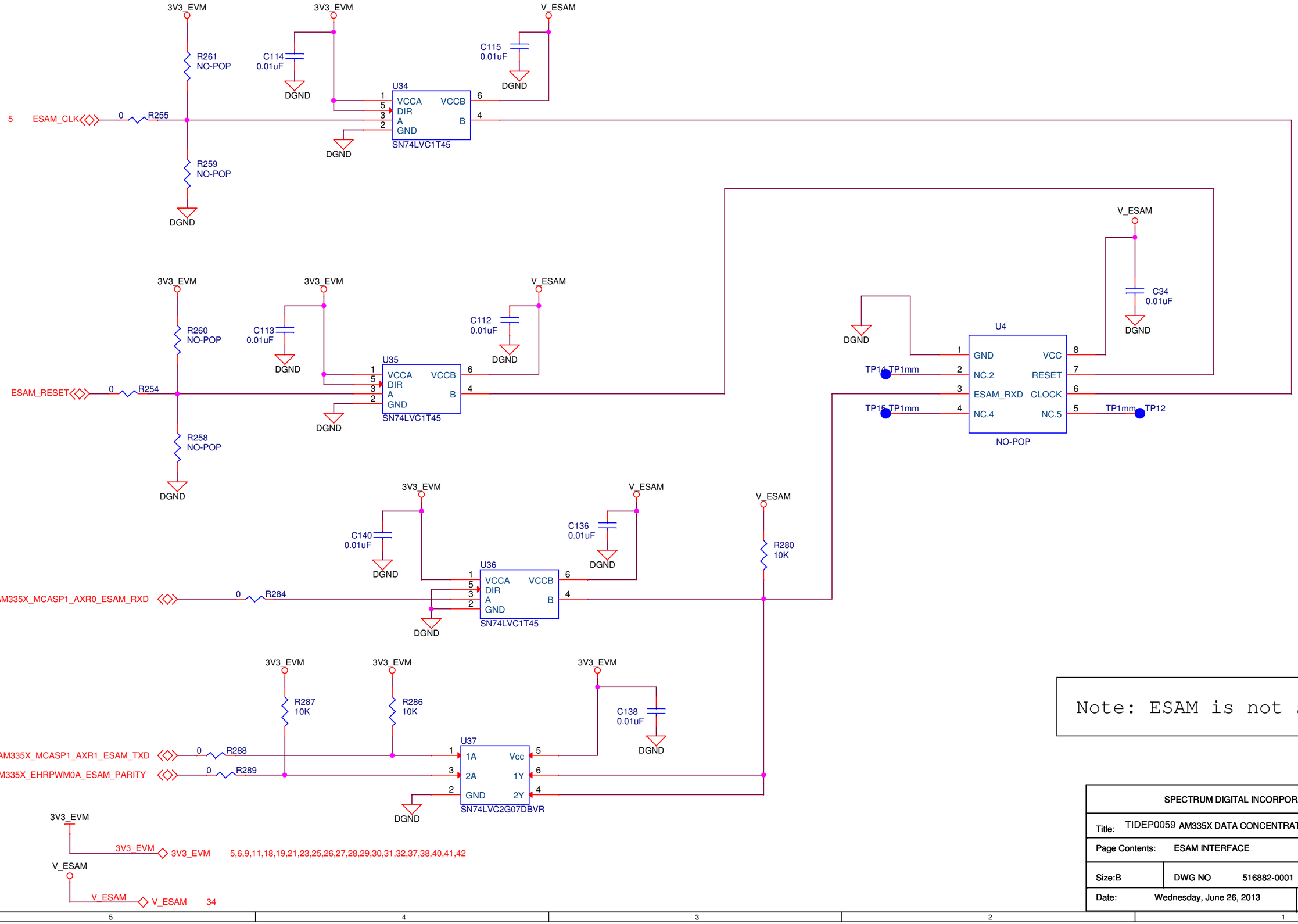
SD/MMC Connector

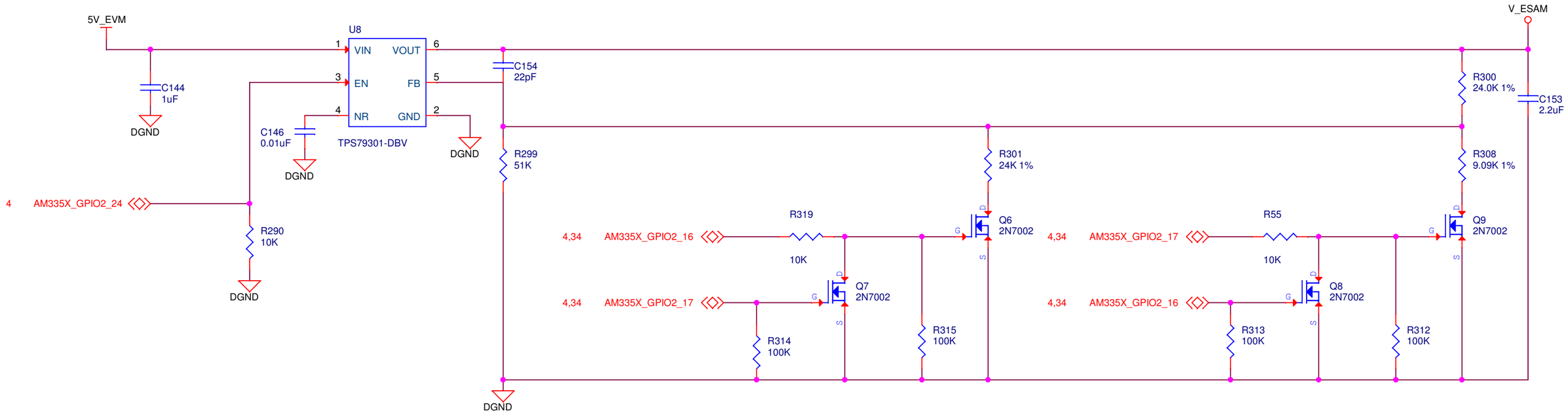


SPECTRUM DIGITAL INCORPORATED		
Title: TIDEP0059 AM335X DATA CONCENTRATOR		
Page Contents: SD CARD INTERFACE		
Size:B	DWG NO 516882-0001	Revision: B
Date: Friday, June 21, 2013	Sheet 32 of 51	



Note: ESAM is not supported

SPECTRUM DIGITAL INCORPORATED		
Title: TIDEP0059 AM335X DATA CONCENTRATOR		
Page Contents: ESAM INTERFACE		
Size:B	DWG NO 516882-0001	Revision: C
Date: Wednesday, June 26, 2013	Sheet 33 of 51	



V_ESAM

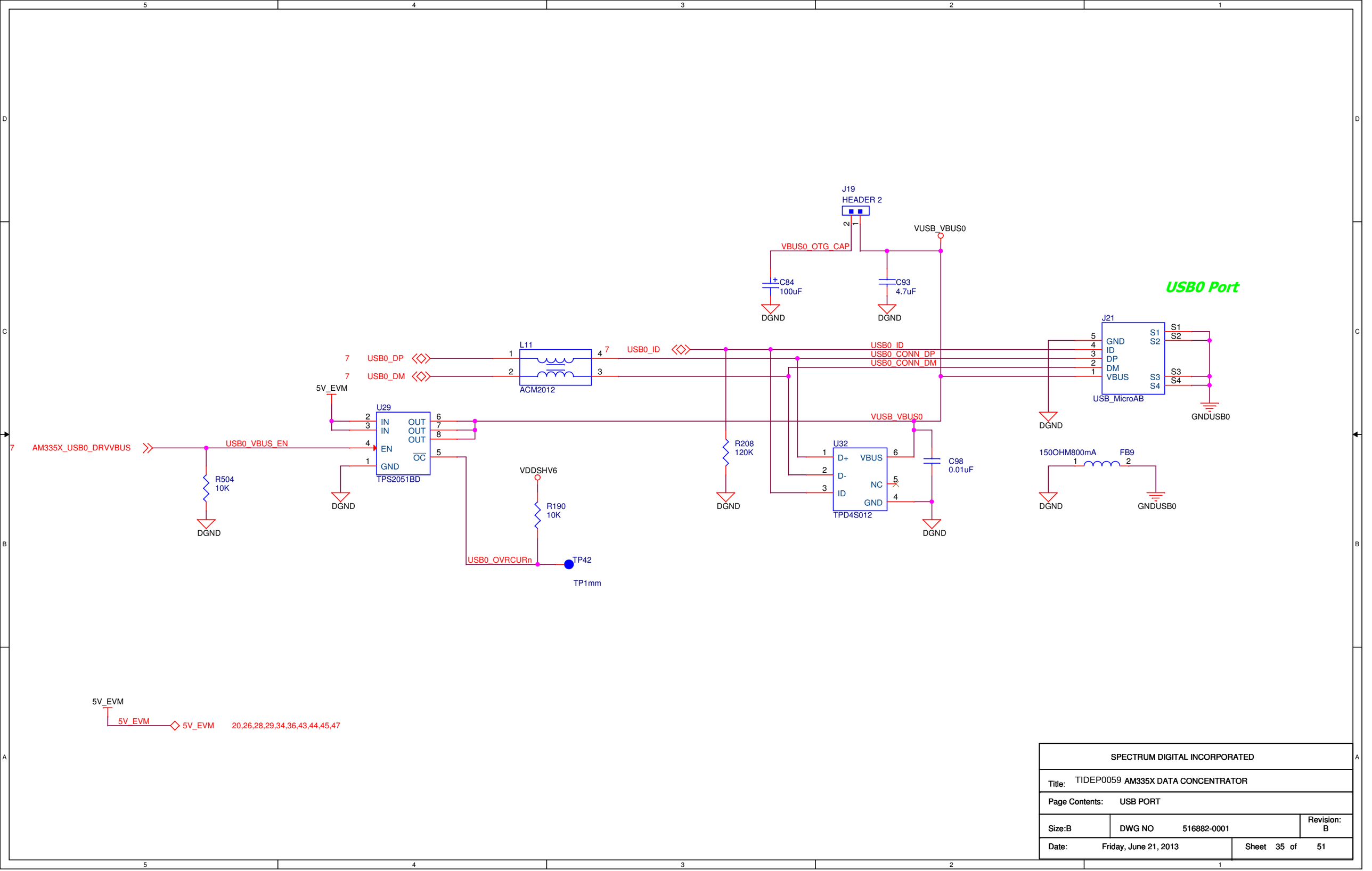
V_ESAM → V_ESAM 33

5V_EVM

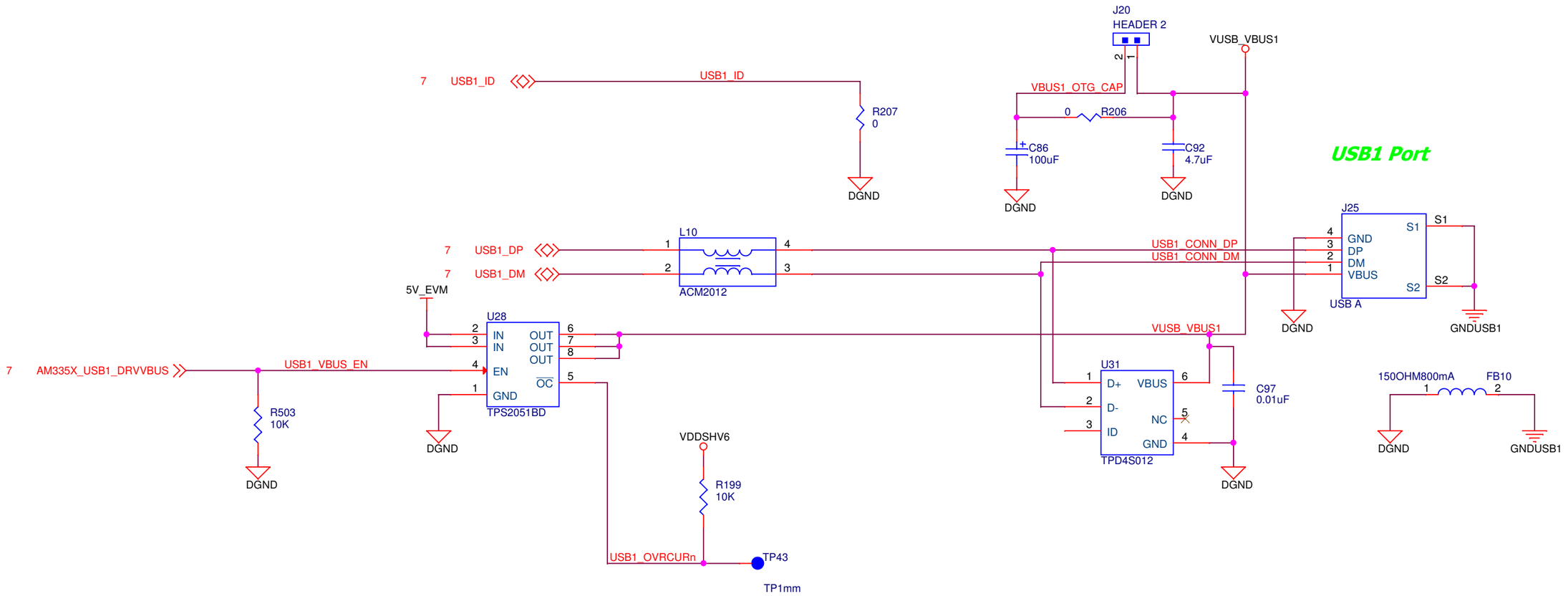
5V_EVM → 5V_EVM 20,26,28,29,35,36,43,44,45,47

Note: ESAM is not supported

SPECTRUM DIGITAL INCORPORATED		
Title: TIDEP0059 AM335X DATA CONCENTRATOR		
Page Contents: ESAM POWER		
Size:B	DWG NO 516882-0001	Revision: B
Date: Wednesday, June 26, 2013	Sheet 34 of 51	



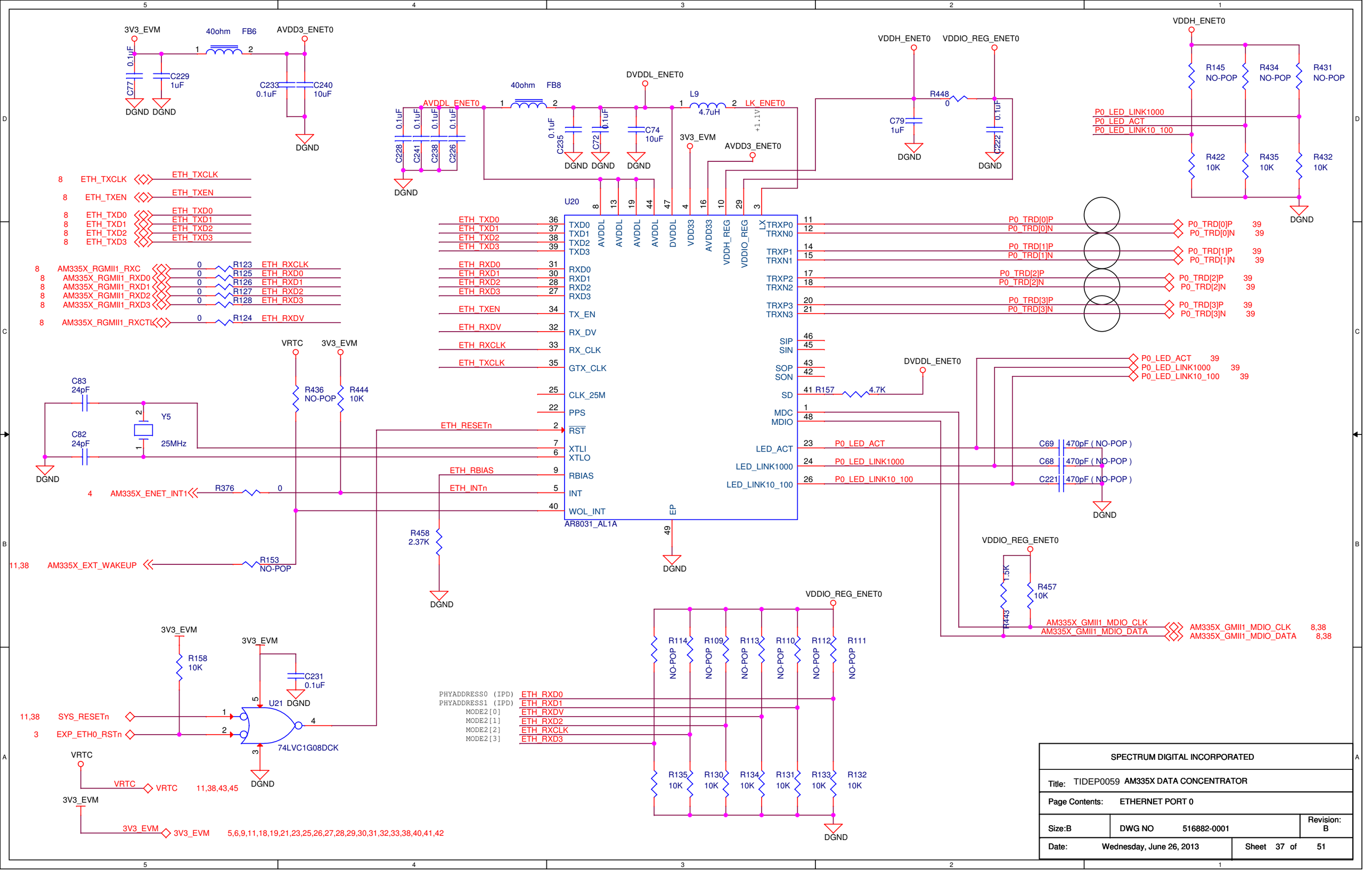
SPECTRUM DIGITAL INCORPORATED		
Title: TIDEP0059 AM335X DATA CONCENTRATOR		
Page Contents: USB PORT		
Size:B	DWG NO 516882-0001	Revision: B
Date: Friday, June 21, 2013	Sheet 35 of 51	



5V_EVM

5V_EVM 5V_EVM 20,26,28,29,34,35,43,44,45,47

SPECTRUM DIGITAL INCORPORATED		
Title: TIDEP0059 AM335X DATA CONCENTRATOR		
Page Contents: USB PORT 1		
Size:B	DWG NO 516882-0001	Revision: B
Date: Friday, June 21, 2013	Sheet 36 of 51	



SPECTRUM DIGITAL INCORPORATED		
Title: TIDEP0059 AM335X DATA CONCENTRATOR		
Page Contents: ETHERNET PORT 0		
Size:B	DWG NO 516882-0001	Revision: B
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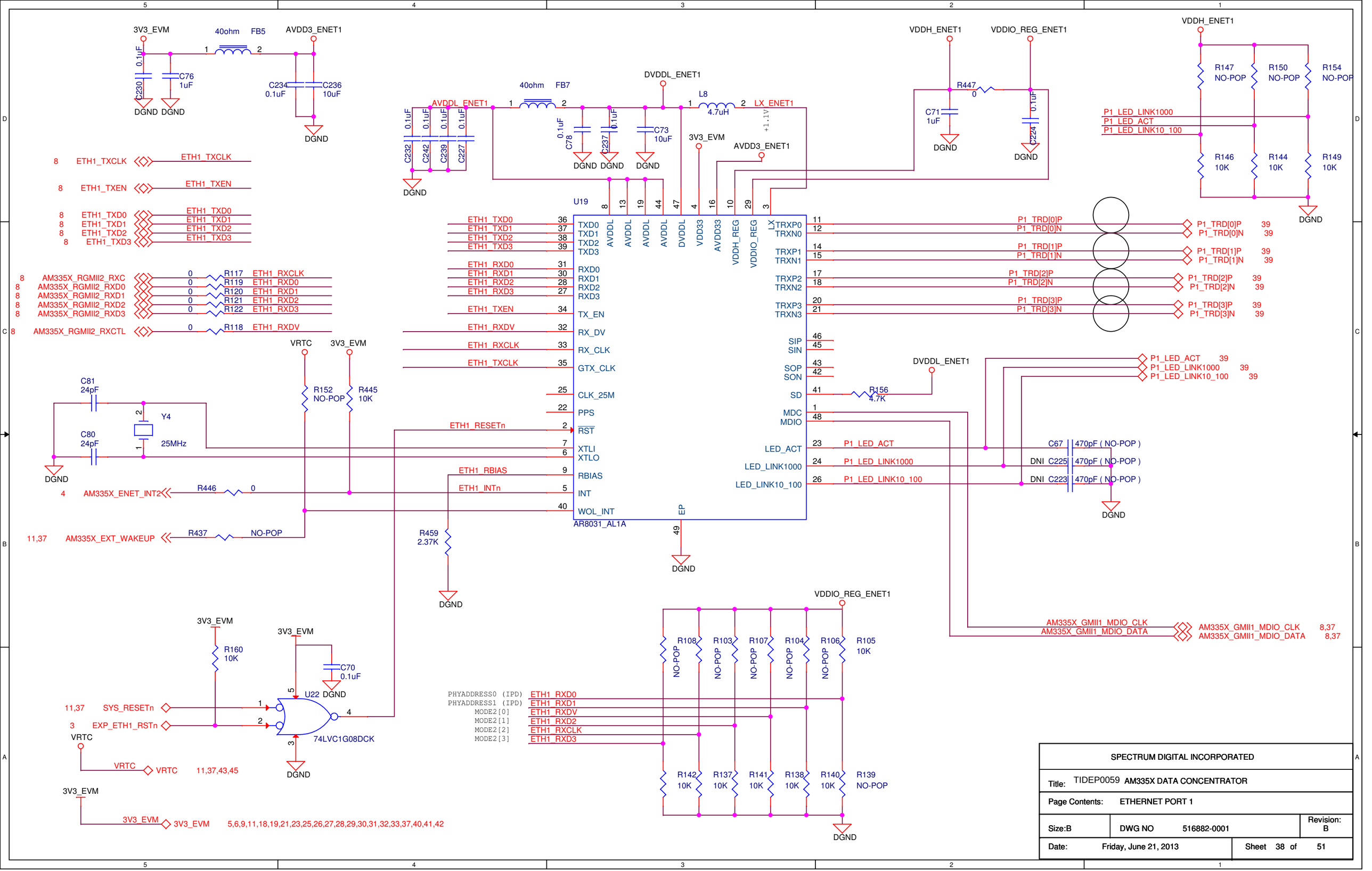
3V3_EVM
40ohm FB5
AVDD3_ENET1
0.1uF C230
C76 1uF
C234 0.1uF
C236 10uF
DGND DGND DGND
DVDDL_ENET1
AVDDL_ENET1
40ohm FB7
L8 4.7uH
LX_ENET1
+1.1V
C232 C242 C239 C227 0.1uF
C78 0.1uF
C237 0.1uF
C73 10uF
DGND DGND DGND DGND
3V3_EVM
AVDD3_ENET1
VDDH_ENET1
VDDIO_REG_ENET1
R447 0
C71 1uF
C224 0.1uF
DGND DGND
VDDH_ENET1
R147 NO-POP
R150 NO-POP
R154 NO-POP
P1_LED_LINK1000
P1_LED_ACT
P1_LED_LINK10_100
R146 10K
R144 10K
R149 10K
DGND
8 ETH1_TXCLK ETH1_TXCLK
8 ETH1_TXEN ETH1_TXEN
8 ETH1_TXD0 ETH1_TXD0
8 ETH1_TXD1 ETH1_TXD1
8 ETH1_TXD2 ETH1_TXD2
8 ETH1_TXD3 ETH1_TXD3
U19
TXD0 TXD1 TXD2 TXD3
TX_EN
GTX_CLK
RXD0 RXD1 RXD2 RXD3
RX_DV
RX_CLK
CLK_25M
PPS
RST
XTLI XTLO
RBIAS
INT
WOL_INT
AR8031_AL1A
EP
AVDDL AVDDL AVDDL AVDDL DVDDL VDD33 AVDD33 VDDH_REG VDDIO_REG
LX
TRXP0 TRXN0
TRXP1 TRXN1
TRXP2 TRXN2
TRXP3 TRXN3
SIP SIN
SOP SON
SD
MDC MDIO
LED_ACT
LED_LINK1000
LED_LINK10_100
8 AM335X_RGMII2_RXC 0 R117 ETH1_RXCLK
8 AM335X_RGMII2_RXD0 0 R119 ETH1_RXD0
8 AM335X_RGMII2_RXD1 0 R120 ETH1_RXD1
8 AM335X_RGMII2_RXD2 0 R121 ETH1_RXD2
8 AM335X_RGMII2_RXD3 0 R122 ETH1_RXD3
8 AM335X_RGMII2_RXCTL 0 R118 ETH1_RXDV
ETH1_TXD0 36
ETH1_TXD1 37
ETH1_TXD2 38
ETH1_TXD3 39
ETH1_RXD0 31
ETH1_RXD1 30
ETH1_RXD2 28
ETH1_RXD3 27
ETH1_TXEN 34
ETH1_RXDV 32
ETH1_RXCLK 33
ETH1_TXCLK 35
ETH1_RESETn 2
7
6
ETH1_RBIAS 9
ETH1_INTn 5
40
49
P1_TRD[0]P 11
P1_TRD[0]N 12
P1_TRD[1]P 14
P1_TRD[1]N 15
P1_TRD[2]P 17
P1_TRD[2]N 18
P1_TRD[3]P 20
P1_TRD[3]N 21
46
45
43
42
41
R156 4.7K
1
48
23 P1_LED_ACT
24 P1_LED_LINK1000
26 P1_LED_LINK10_100
P1_TRD[0]P 39
P1_TRD[0]N 39
P1_TRD[1]P 39
P1_TRD[1]N 39
P1_TRD[2]P 39
P1_TRD[2]N 39
P1_TRD[3]P 39
P1_TRD[3]N 39
P1_LED_ACT 39
P1_LED_LINK1000 39
P1_LED_LINK10_100 39
C67 470pF (NO-POP)
DNI C225 470pF (NO-POP)
DNI C223 470pF (NO-POP)
DGND
AM335X_GMII1_MDIO_CLK
AM335X_GMII1_MDIO_DATA
AM335X_GMII1_MDIO_CLK 8,37
AM335X_GMII1_MDIO_DATA 8,37
C81 24pF
C80 24pF
Y4
25MHz
DGND
VRTC 3V3_EVM
R152 NO-POP
R445 10K
4 AM335X_ENET_INT2
R446 0
11,37 AM335X_EXT_WAKEUP
R437 NO-POP
R459 2.37K
DGND
VDDIO_REG_ENET1
R108 NO-POP
R103 NO-POP
R107 NO-POP
R104 NO-POP
R106 NO-POP
R105 10K
PHYADDRESS0 (IPD) ETH1_RXD0
PHYADDRESS1 (IPD) ETH1_RXD1
MODE2[0] ETH1_RXDV
MODE2[1] ETH1_RXD2
MODE2[2] ETH1_RXCLK
MODE2[3] ETH1_RXD3
R142 10K
R137 10K
R141 10K
R138 10K
R140 10K
R139 NO-POP
DGND
3V3_EVM
R160 10K
C70 0.1uF
U22
74LVC1G08DCK
11,37 SYS_RESETn
3 EXP_ETH1_RSTn
VRTC
VRTC VRTC 11,37,43,45
3V3_EVM
3V3_EVM 3V3_EVM 5,6,9,11,18,19,21,23,25,26,27,28,29,30,31,32,33,37,40,41,42
SPECTRUM DIGITAL INCORPORATED
Title: TIDEP0059 AM335X DATA CONCENTRATOR
Page Contents: ETHERNET PORT 1
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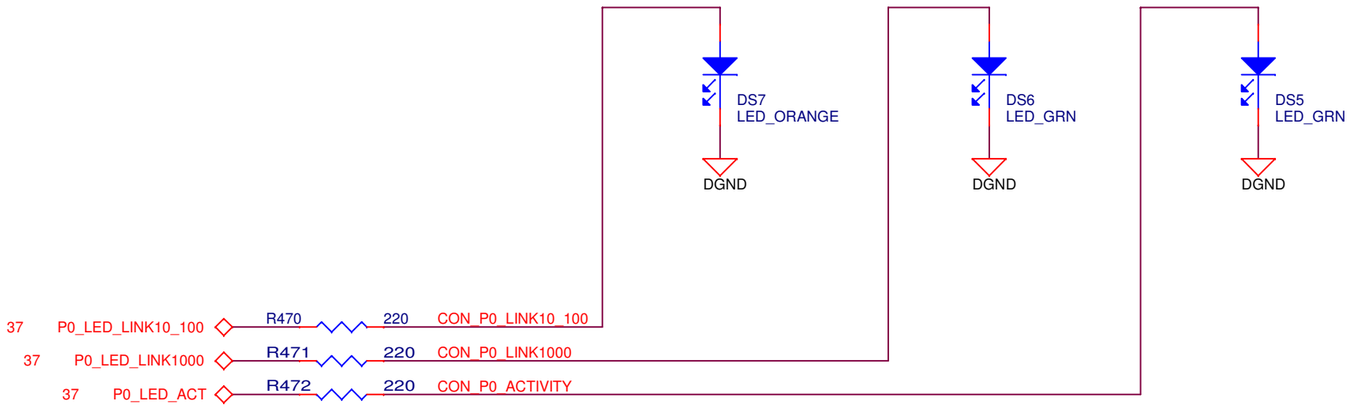
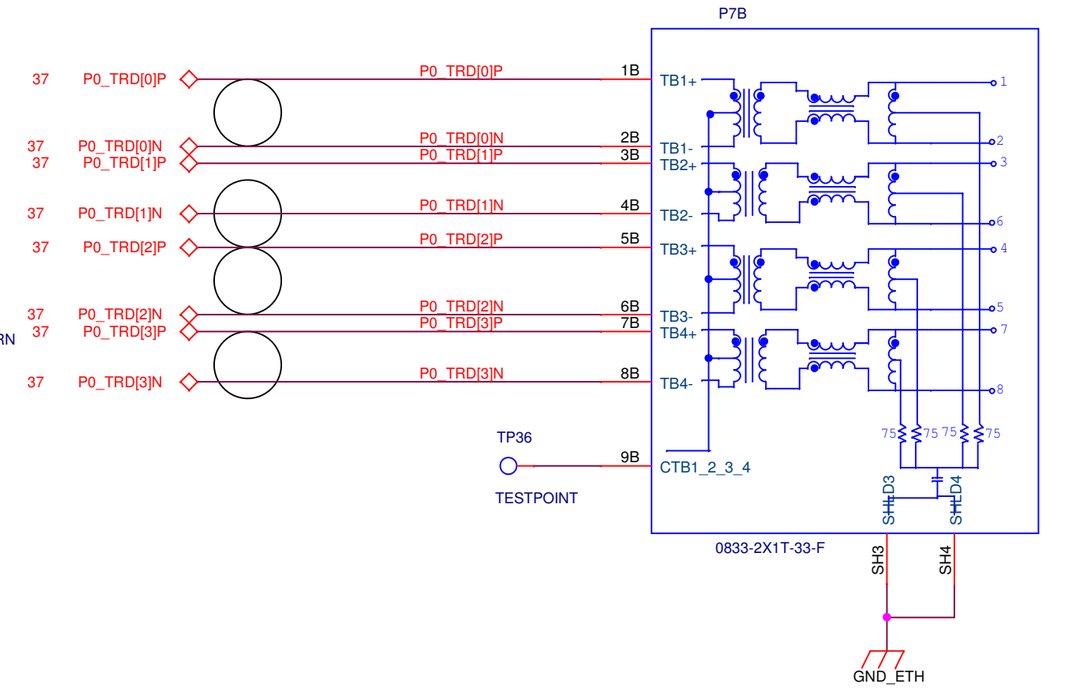
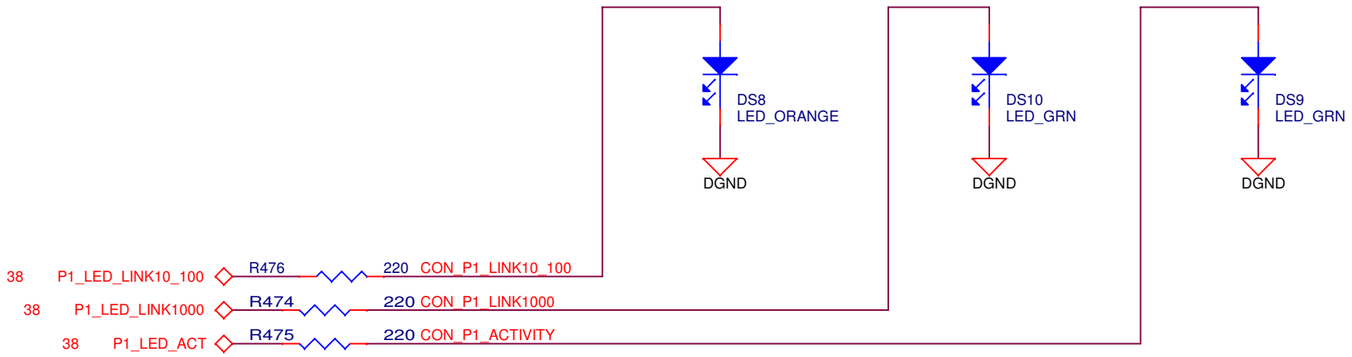
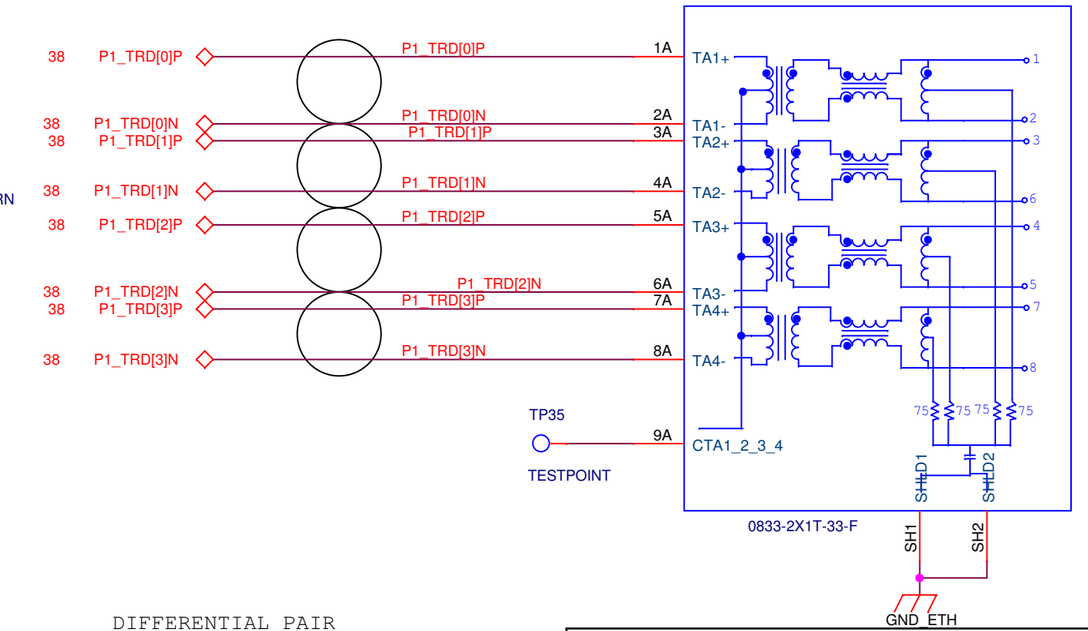
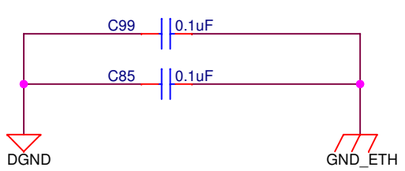






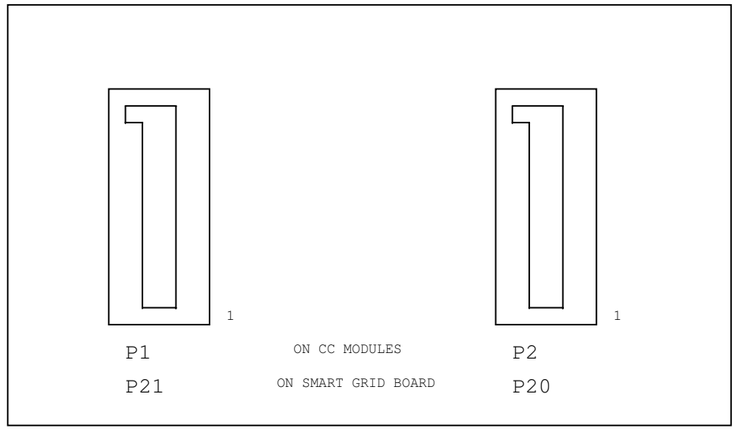


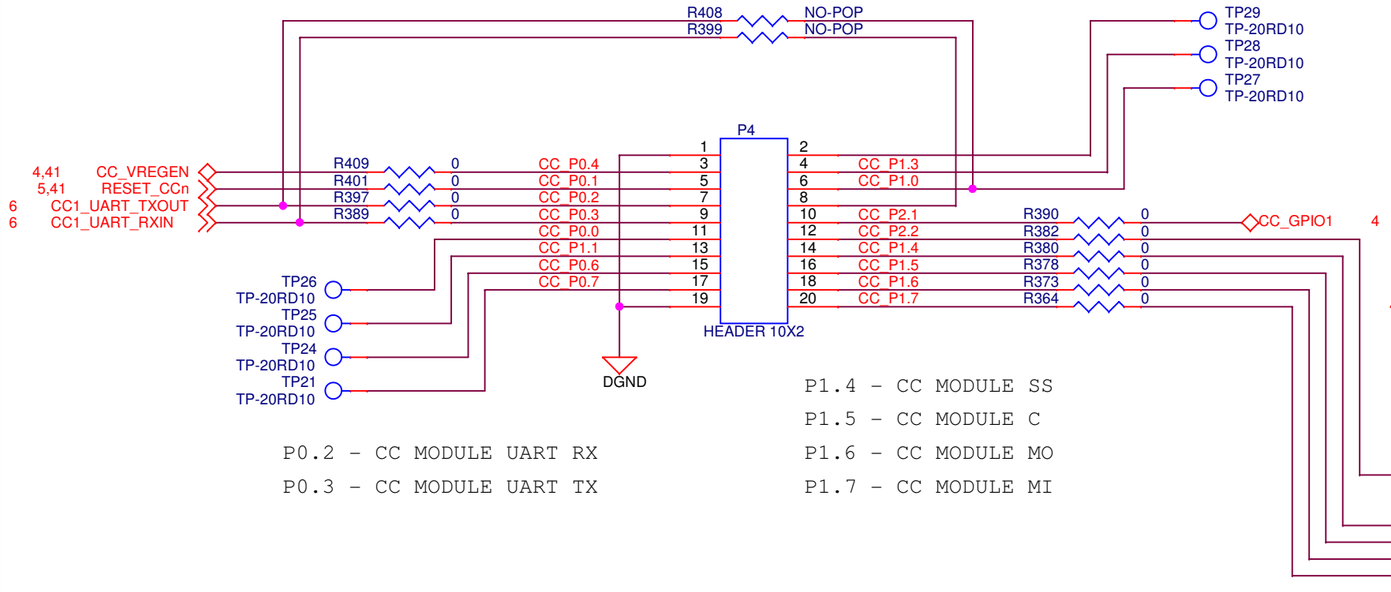


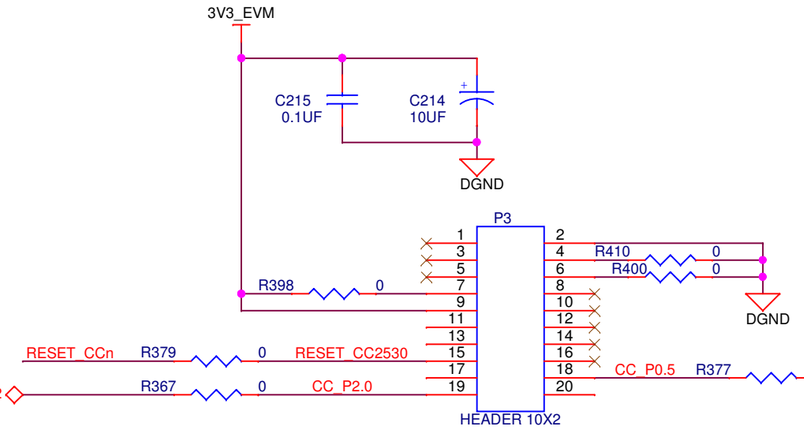
DIFFERENTIAL PAIR
100 OHM DIFFERENTIAL IMPEDANCE
SHORT AND STRAIGHT AS POSSIBLE,
MINIMUM NUMBER OF VIAS

SPECTRUM DIGITAL INCORPORATED		
Title: TIDEP0059 AM335X DATA CONCENTRATOR		
Page Contents: ETHERNET - OUTPUT CONNECTORS		
Size:B	DWG NO 516882-0001	Revision: B
Date: Friday, June 21, 2013	Sheet 39 of 51	

NOTE: DIMENSIONS AND LOCATIONS OF THESE CONNECTORS MUST MEET SPECIFICATION FOR INTERFACE MODULES
REFERENCE CC2530-EVM-UG







SPECTRUM DIGITAL INCORPORATED		
Title: TIDEP0059 AM335X DATA CONCENTRATOR		
Page Contents: CC CARD INTERFACE1		
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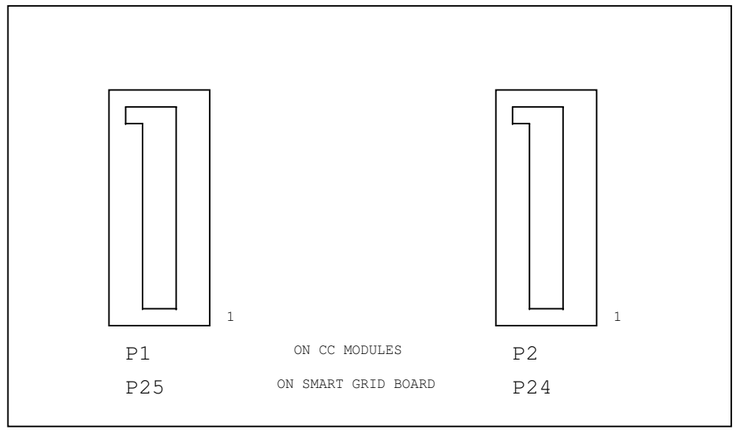
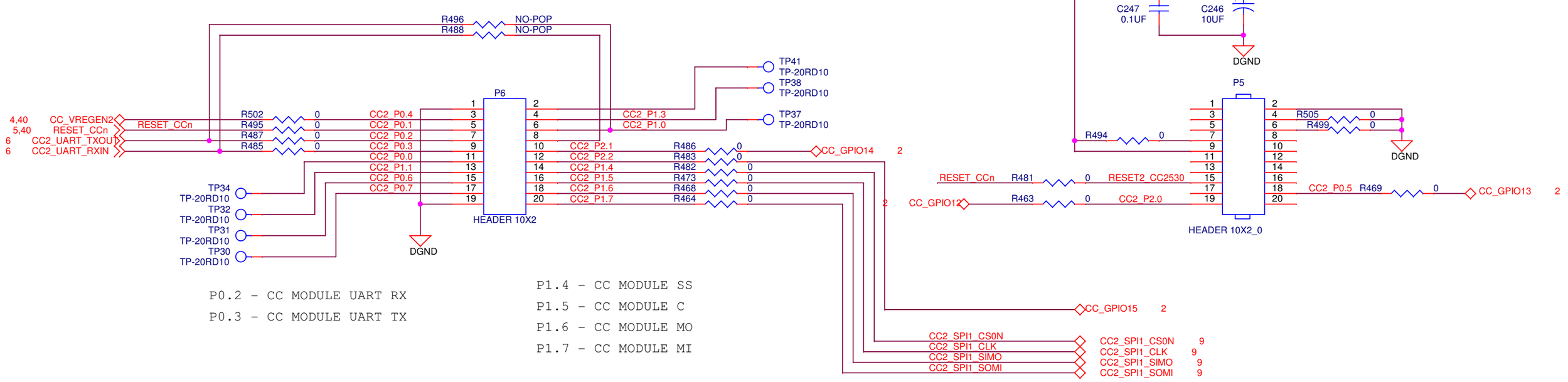
NOTE: DIMENSIONS AND LOCATIONS OF THESE CONNECTORS MUST MEET SPECIFICATION FOR INTERFACE MODULES REFERENCE





P0.2 - CC MODULE UART RX
P0.3 - CC MODULE UART TX

P1.4 - CC MODULE SS
P1.5 - CC MODULE C
P1.6 - CC MODULE MO
P1.7 - CC MODULE MI

SPECTRUM DIGITAL INCORPORATED		
Title: TIDEP0059 AM335X DATA CONCENTRATOR		
Page Contents: CC CARD INTERFACE2		
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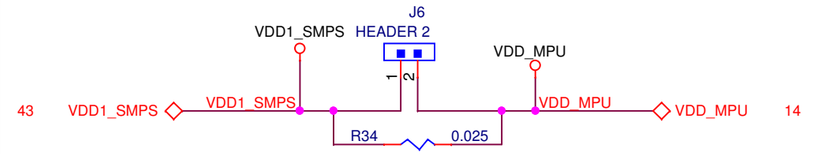
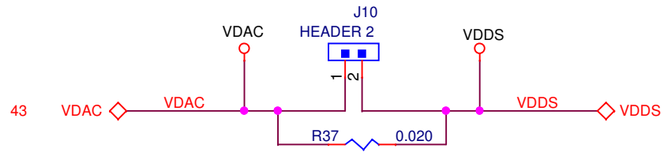
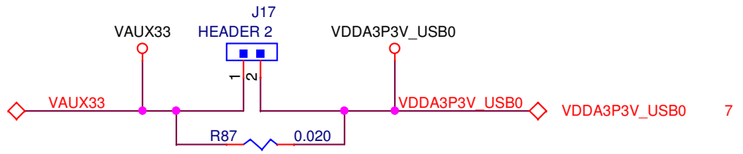
VDD1_SMPS = 1.1 V



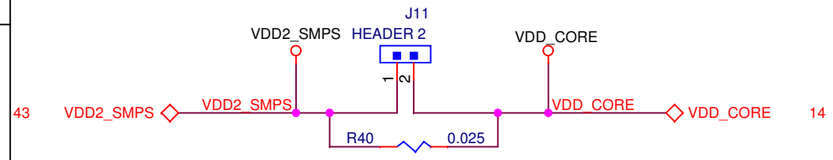
VDAC = 1.8V



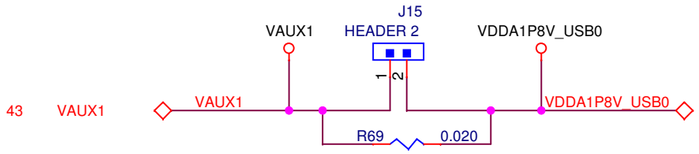
VAUX33 = 3.3V



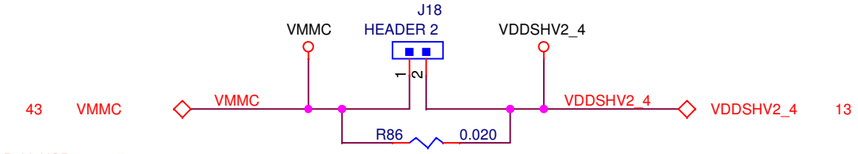
VDD2_SMPS = 1.1 V



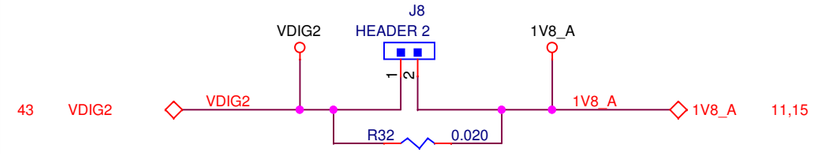
VAUX1 = 1.8V



VMMC = 3.3V

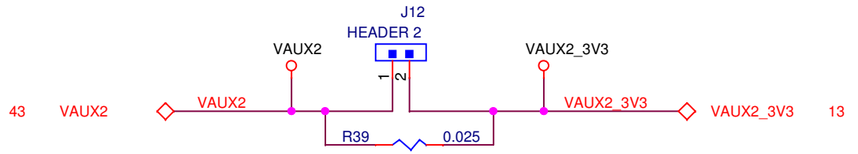


VDIG2 = 1.8V

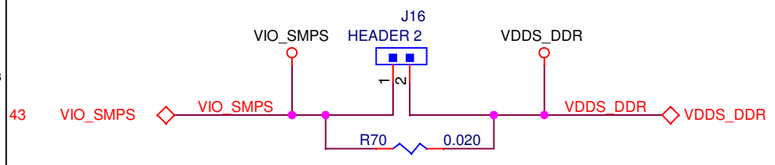


VDIG1 = 1.8V

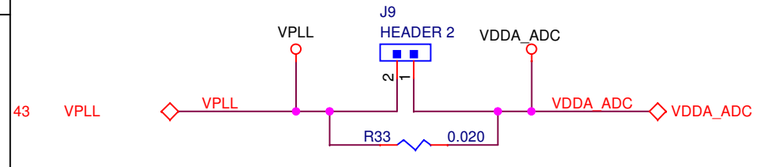
VAUX2 = 3.3V



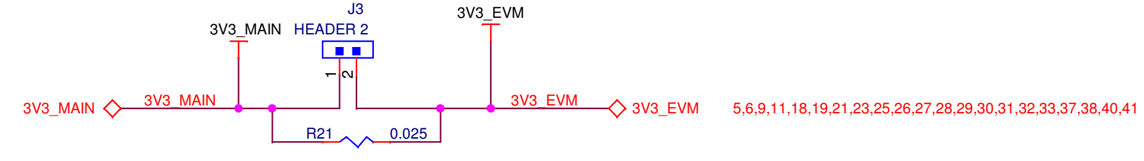
VIO_SMPS = 1.8V



VPLL = 1.8V



3V3_EVM = 3.3V (MAIN)



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Power Management IC

VDD3_SMPS = NOT USED

VDD3_SMPS = NOT USED

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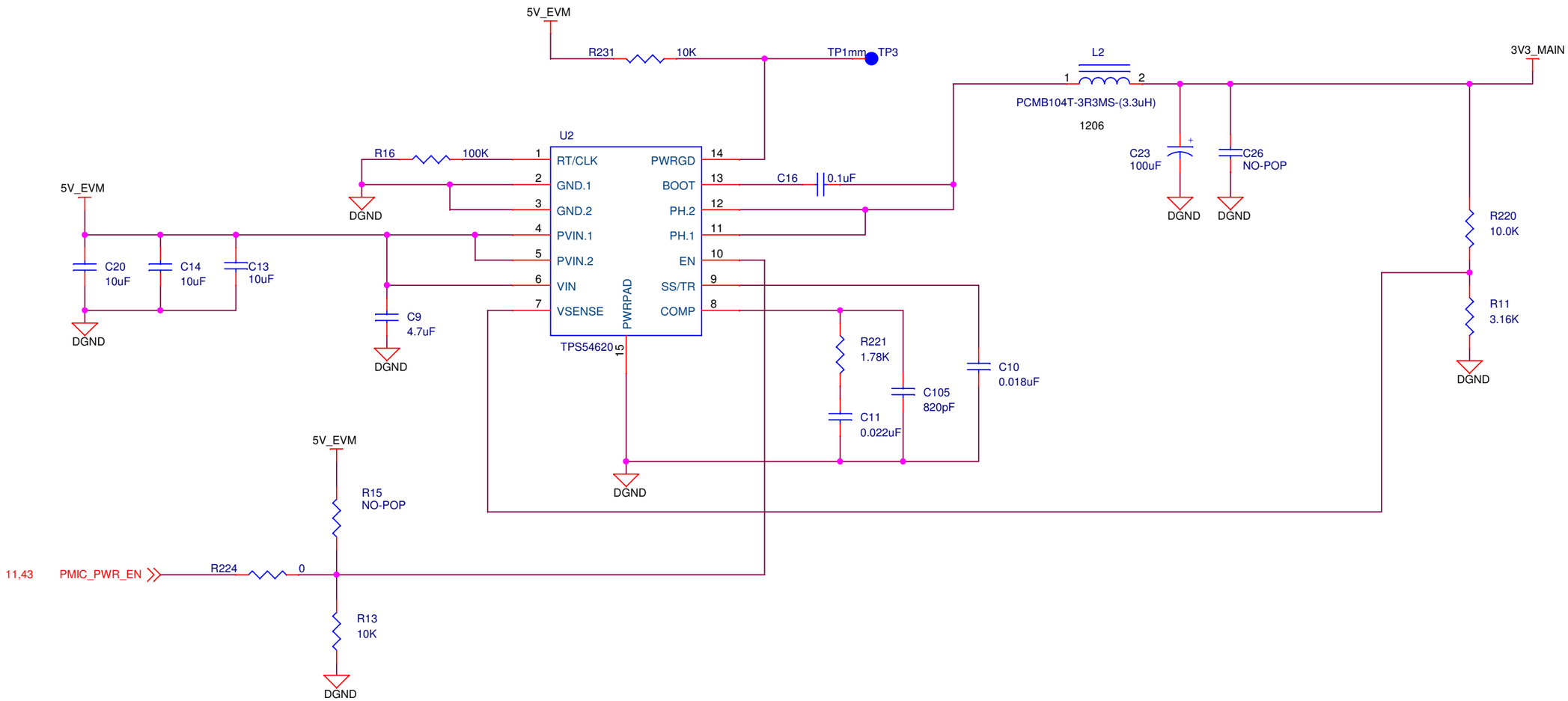

5V_EVM — 5V_EVM — 5V_EVM — 20,26,28,29,34,35,36,43,45,47

3V3_MAIN — 3V3_MAIN — 3V3_MAIN — 42

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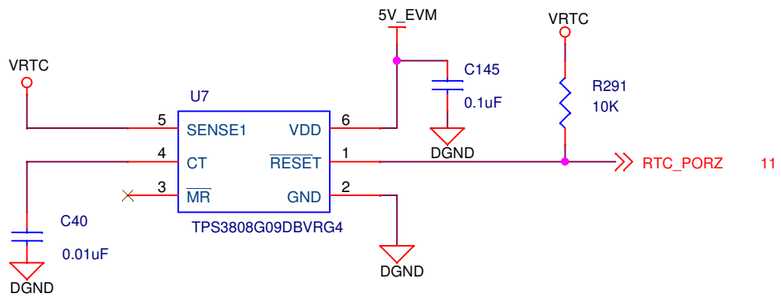
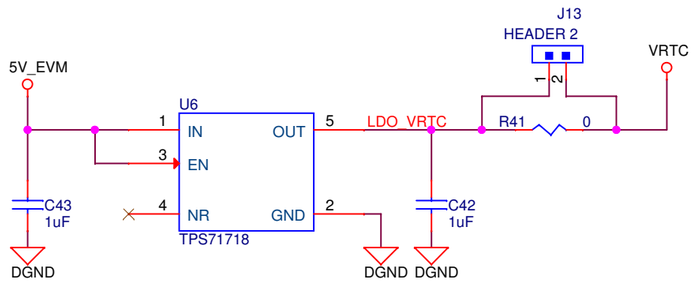
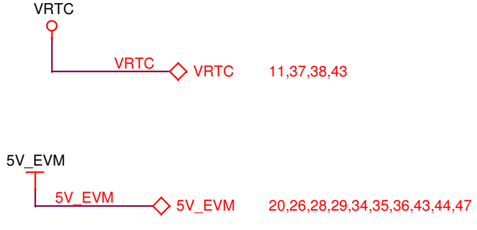


VRTC = 1.8V





SPECTRUM DIGITAL INCORPORATED		
Title: TIDEP0059 AM335X DATA CONCENTRATOR		
Page Contents: RTC POWER RESET		
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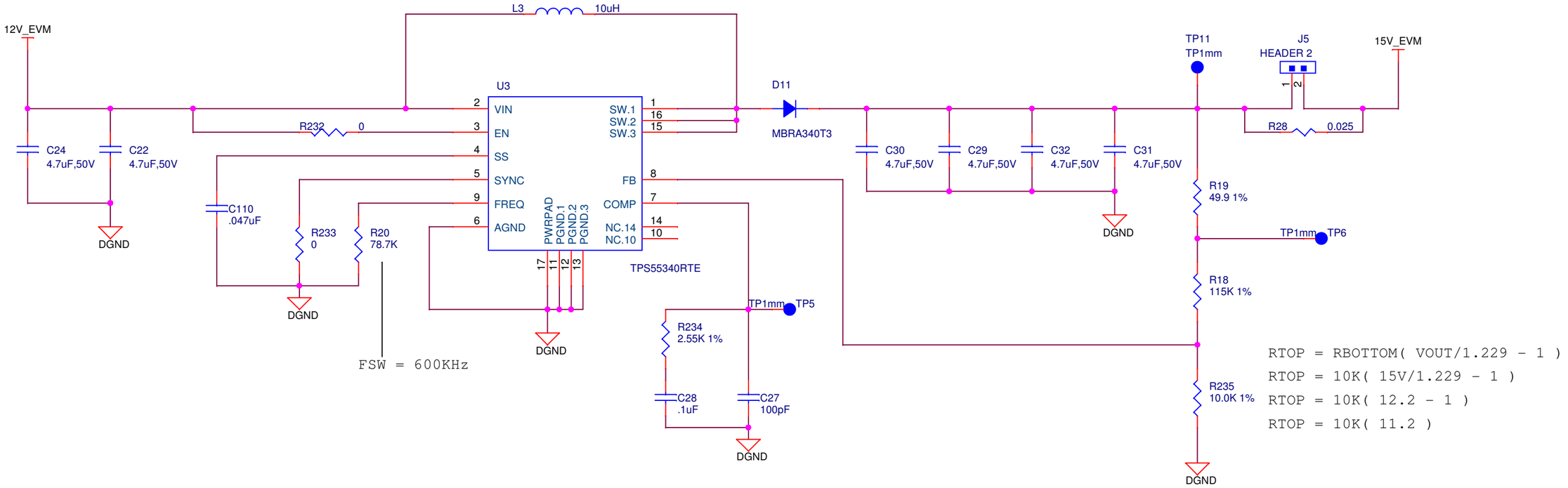

12V_EVM

12V_EVM — 12V_EVM 47,49

15V_EVM

15V_EVM — 15V_EVM 26

SPECTRUM DIGITAL INCORPORATED		
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Page Contents: 12V TO 15V BOOST		
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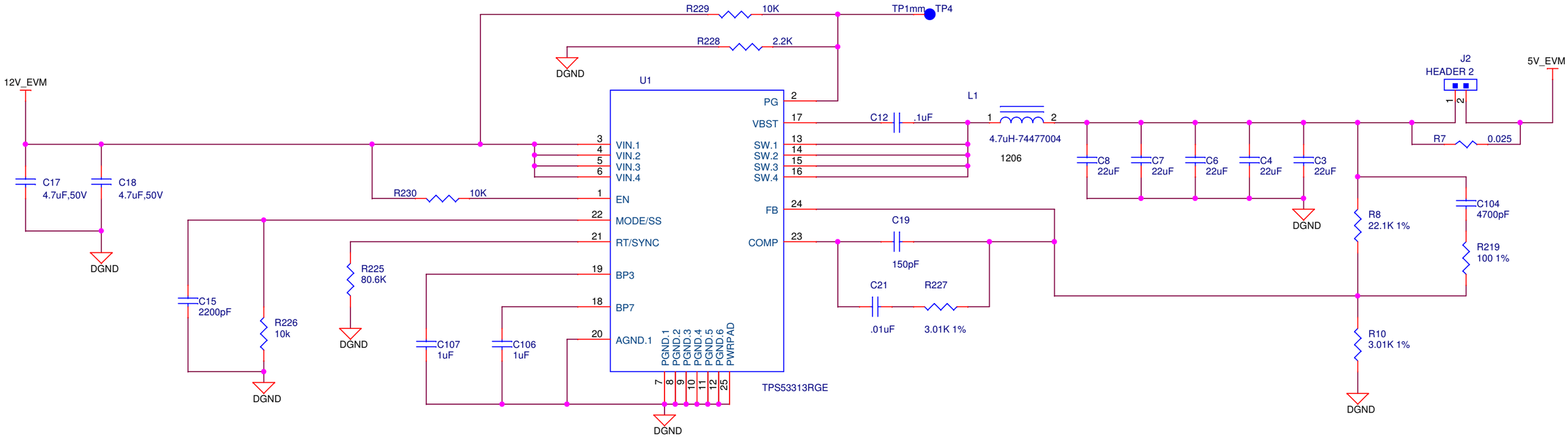

5V_EVM

5V_EVM — 5V_EVM — 5V_EVM 20,26,28,29,34,35,36,43,44,45

12V_EVM

12V_EVM — 12V_EVM — 12V_EVM 46,49

SPECTRUM DIGITAL INCORPORATED		
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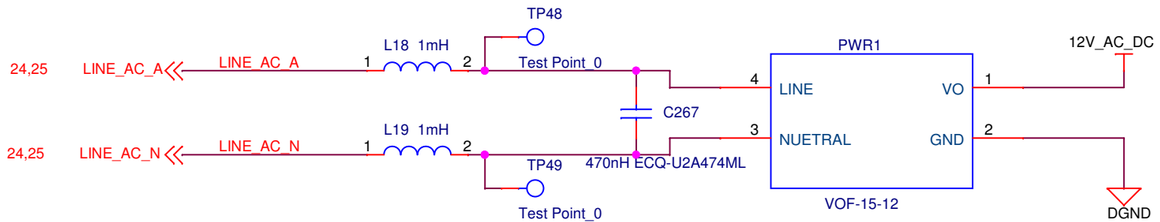
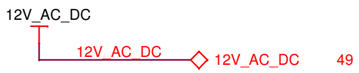
100 MILLIMETER BY 60 MILLIMETER RESERVE





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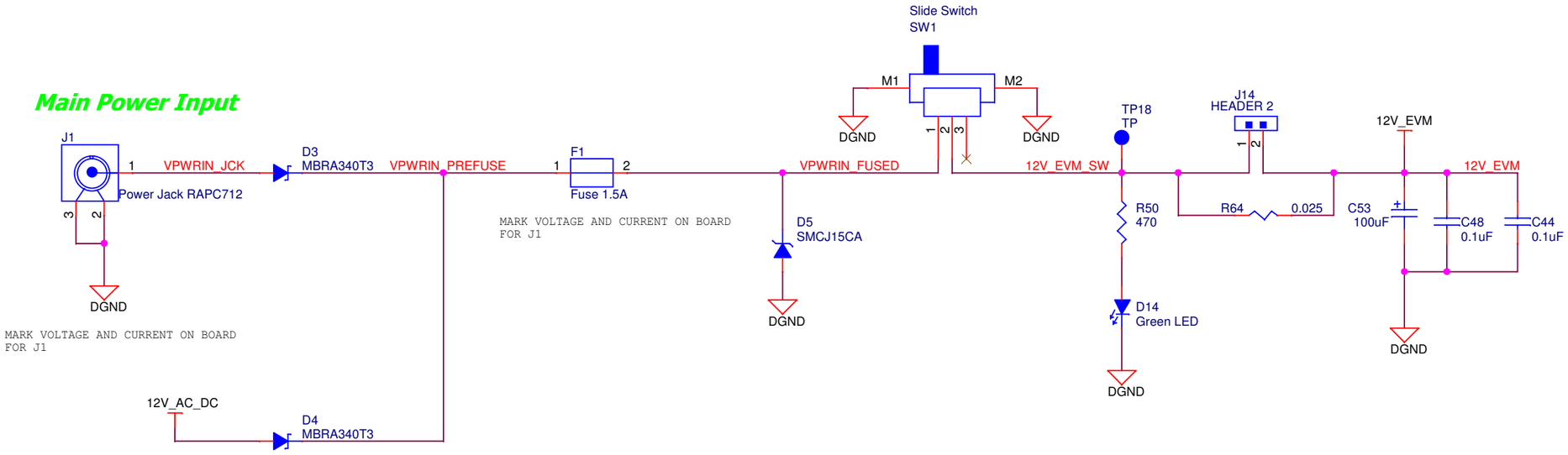
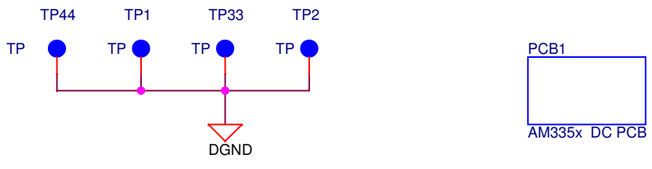
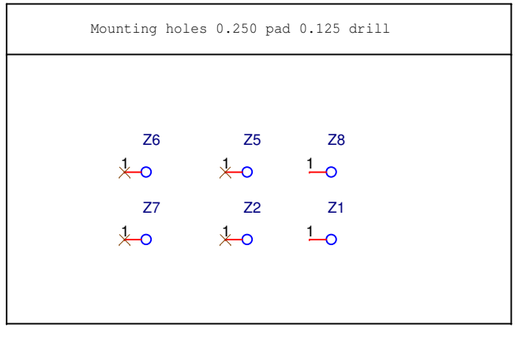
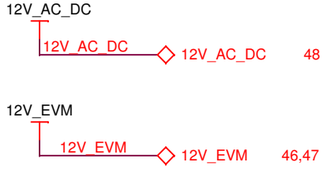
Main Power Input









SPECTRUM DIGITAL INCORPORATED		
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GENERAL
USE 4 MIL LINES AND 4 MIL SPACE

USE 20-10 VIA OR 18-8 VIA

IMPEDANCE CONTROLED 50 OHMS AT 4 MIL

USB0
DIFFERENTIAL PAIR DP/DM 90 OHMS
SET PHASE TO 0
ROUTE PAIR WITH 3X CLEARANCE TO NEXT CLOSET SIGNAL

USB1
DIFFERENTIAL PAIR DP/DM 90 OHMS
SET PHASE TO 0
ROUTE PAIR WITH 3X CLEARANCE TO NEXT CLOSET SIGNAL

DDR

USE TIMING MODEL

TURN ON Z VIA

SET ADDRESS AND CONTROL TO 20 PICOSECONDS

SET DATA TO 20 PICOSECONDS

CONTROL HAS DIFFERENTIAL PAIR ON CLOCKS

DATA HAS 2 DIFFERENTIAL PAIRS FOR DATA STROBES

ETHERNET PORT 0

MAC TO PHY INTERFACE HAS 2 GROUPS WITH CONSTRAINTS, TX GROUP AND RX GROUP 100 MIL TRACE MATCHING

4 SETS OF DIFF PAIRS FROM PHY TO ETHERNET JACK 100 OHM

ETHERNET PORT 1

MAC TO PHY INTERFACE HAS 2 GROUPS WITH CONSTRAINTS, TX GROUP AND RX GROUP 100 MIL TRACE MATCHING

4 SETS OF DIFF PAIRS FROM PHY TO ETHERNET JACK 100 OHM

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516880-E001				
6/11/2013				
Gus Martinez				
Tony C				
516880-0001R				
B				
C				
6/11/2013				
Init Date	**Priority**	**Status**	**Description**	**Stat Schematic**
			Need at least 8mm spacing between high voltage components (>33Vrms, 46.7Vpk, 70Vdc) on the board. Noticeble violations: 1. PWR1 block too close to RS495 components (ISO4-ISO9 and U15), 2. Transformer T1 low-voltage pins too close to ISO3 high-voltage signals.	na
			1. Sheet 28 (IR interface) missing from title page list, 2. Hide Sheet 33 (ESAM interface) and sheet 34 (ESAM power) from public schematics, 3. Correct fuse rating (should be 1.5A) on Sheet 49 (Power Input).	
			F1 From 100872-0004R To 100872-1500R	done
			Sheet 33: Do not populate final boards with DIP8 (U4).	done
			U4 From 100186-0008R to NO-POP	
			Sheet 24: Change layout/schematic such that JP1-JP4 can be used to fully disconnect Neutral and line phases from board, i.e. zero-crossing does not tap directly from P1.	
			1. Change D10 to SM6T7V5CA. 2. Change C25 to C0805C222KARACTU. 3. Change C109, C101, C103 to C1608X5R1H104M080AA.	
			Sheet 24: D10 From 103533-0001R To 104356-0001R SM6T7V5CA	done
			Sheet 24: C25 From 103532-1101R To 103532-1222R C0805C222KARACTU	done
			Sheet 25: C109, C101, C103 From 103594-1330R To 100993-1100R	done
			Add a multifunction gate (SN74LVC1G57DBVR) to ZERO_PLC_A, ZERO_PLC_B, ZERO_PLC_C. See schematic on "Zero Crossing" sheet.	
			Add U39, U40, U41 102872-0001R	done
			Add C264, C265, C266 101587-1100R	done
			Sheet 26: Replace R248 and R242 with jumper. R252 can stay as a 0 Ohm.	
			Remove R248 and R242 101370-0001R	done
			Add JP8 and JP9 100115-0002R	done
			Sheet 24: Replace capacitive coupling on all three phases with circuit shown on "PLC Interface" sheet.	
			Remove C261, C262, C263 NO-POP	done
			C1, C2, C5 From 101079-0470R To 101410-1470R 0.47uF 400V (ECQ-E4474KF)	done
			Add L12,L14,L16 15uH 103084-0150R DR1040-150-R	done
			Add L13,L15,L17, 600nH 104357-0600R ETQ-P5LR60XFA	done
			Add JP10, JP11, JP12, JP13, JP14 100115-0002R	done
			Remove "Data Concentrator EVM" and TI logo. Add "TMDSDC3359" and TI logo to the assembly and serial number information. Move this logo and text to somewhere on the board where it will not be obscured. See TI Logo sheet.	na
			Sheet 48: Need to add filter at the input of the AC/DC to block PLC high-frequency signals. See "ACDC Filter" tab. Connect filter at PWR1 nets LINE_AC_A and LINE_AC_N.	
			Add L18, L19 1mH LPS6235-105MLC 104358-0103R	done
			Add C267 470nH ECQ-U2A474ML 104359-1470R	done
			Add TP48, TP49 NO-POP	
			Sheet 3 and Sheet 27: Currently UART3 connects to SCIA on the PLC SOM. Need a jumper option to bring out SCIA to an existing RS232 port (P8B). See sheet titled "SCIA-RS232".	
			Add JP16, JP17, JP18, JP19 100115-0003R	done
			Sheet 26. Depopulate some of the IR components	
			C96 From 102895-0101R To C0805-NOPOP	done
			C94 From 101587-1100R To C0402-NOPOP	done
			R511 NO-POP	done
			U38 From 101689-0125R To 101057-0125R (SN74CBTLV1G125DCKR -> SN74LVC1G125DCKR)	done

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