

# **Designing with SN74LVCXT245 and SN74LVCHXT245 Family of Direction Controlled Voltage Translators/Level-Shifters**

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## ABSTRACT

The proper understanding and interpretation of feature sets of SN74LVCXT245 and SN74LVCHXT245 product families, helps when designing with this family of products. This application report explains the feature sets in detail and enables system-design engineers to derive the maximum benefit from SN74LVCXT245 and SN74LVCHXT245 devices. It also seeks to address the most frequently asked questions when designing applications using these products.

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## 1 Introduction

Dual-supply devices are the best choice for most voltage level-translation applications. These devices can perform bidirectional level translation between a wide range of voltage nodes. They offer low power consumption, fast propagation delays and active current drive. LVC, the 5 V tolerant logic device family is buffer-based, whose basic operation is shown in Figure 1.

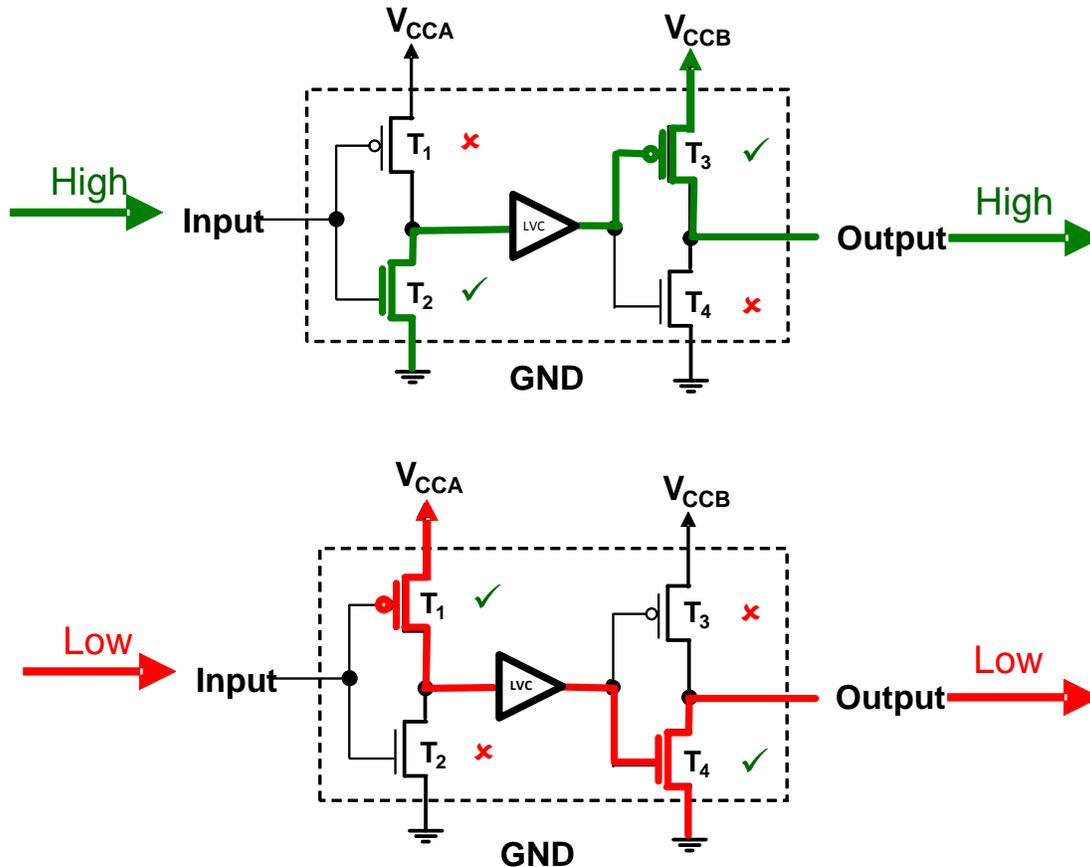


Figure 1. Basic Operation of LVC Devices

## 2 Logic Compatibility

Comparing the output DC steady-state logic-high and logic-low voltage levels ( $V_{OH}$  min and  $V_{OL}$  max) to the input threshold ( $V_{IH}$  min and  $V_{IL}$  max) helps determine if a port from one technology is compatible to another. If the output voltage levels ( $V_{OH}$  and  $V_{OL}$ ) are outside of the minimum  $V_{IH}$  and maximum  $V_{OL}$  range of an input port, it can be considered that the ports are compatible (see Figure 2).

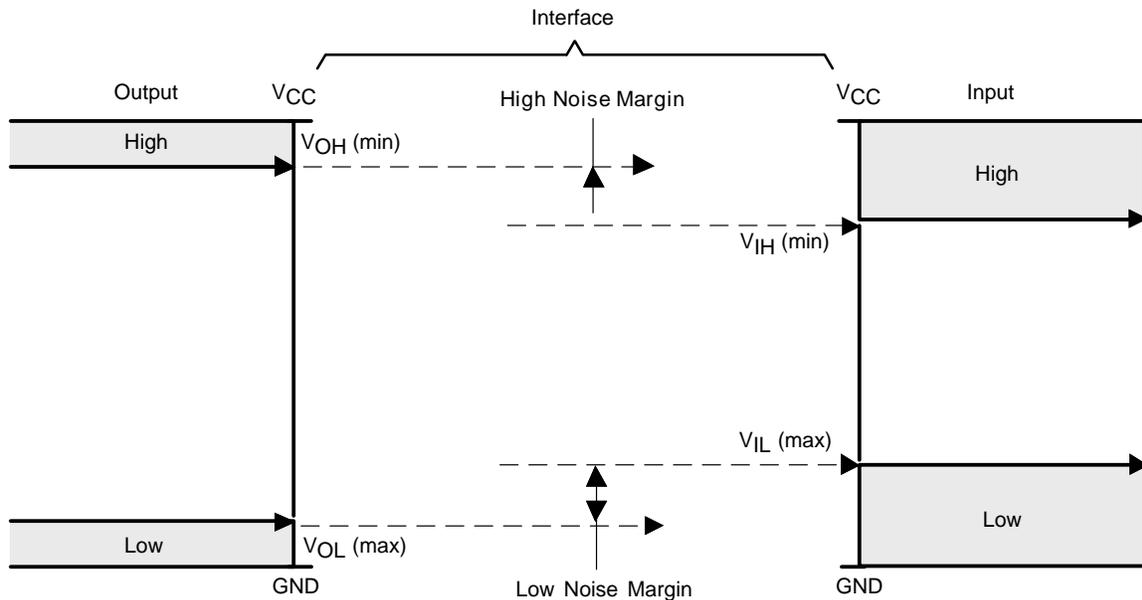


Figure 2. Logic Compatibility Between I/Os

Failure to supply a voltage to the input of a CMOS device that meets the  $V_{IH}$  or  $V_{IL}$  recommended operating conditions can cause:

1. Propagation of incorrect logic states resulting in bit errors
2. High  $I_{CC}$  currents in the level translator and also in the interfacing device
3. High input noise gain and oscillations
4. Power and ground rail surge currents and noise
5. Catastrophic device and circuit failure

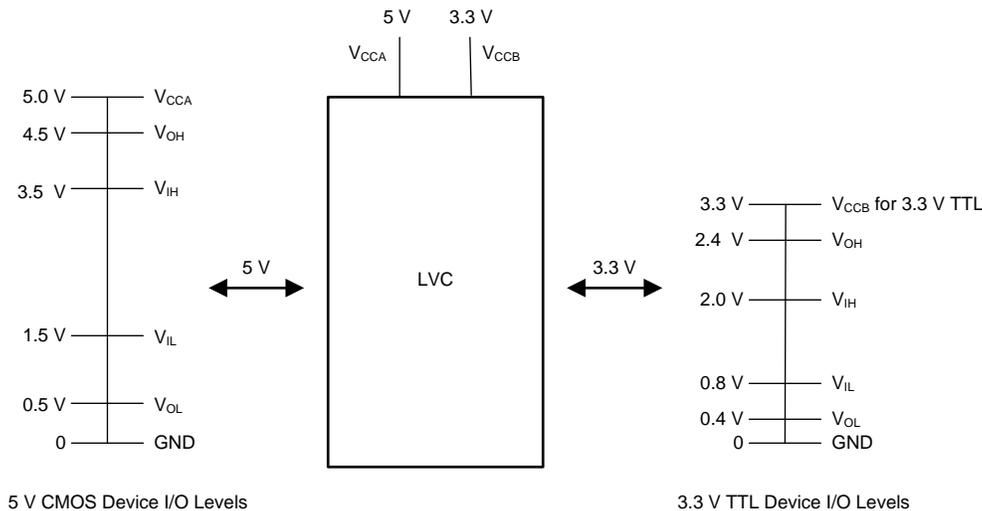


Figure 3. Device at 3.3 V  $V_{CC}$  With 3.3 V I/Os on One Side and 5 V on the Other, Showing Switching Levels

The switching levels for CMOS inputs are 70% of  $V_{CC}$  for  $V_{IH}$  and 30% of  $V_{CC}$  for  $V_{IL}$ . A 5 V driver must reach 3.5 V to meet the  $V_{IH}$  level. Use the  $\Delta I_{CC}$  specification as a reference when driving a CMOS device input with a TTL output. The  $\Delta I_{CC}$  specification also demonstrates the high currents that can occur if  $V_{IH}$  and  $V_{IL}$  recommended operating conditions are not observed.

### 3 CMOS Input Structure

In some cases, legacy 5 V signal chains co-exist with newer low voltage devices, and there is a need for the different voltage systems to interface to each other. There are a number of low voltage families that have capability to interface with 5 V devices on the inputs, outputs, or both. Also, 3.3 V devices need the capability to interface to either 2.5 V or 1.8 V devices. When mixing logic devices from different voltage systems, the I/O pins must be able to tolerate voltages from the higher voltage system. The SN74LVCXT245 and SN74LVCHXT245 CMOS level-shifter product families remove diode paths to  $V_{CC}$  thus providing overvoltage tolerance (Figure 4).

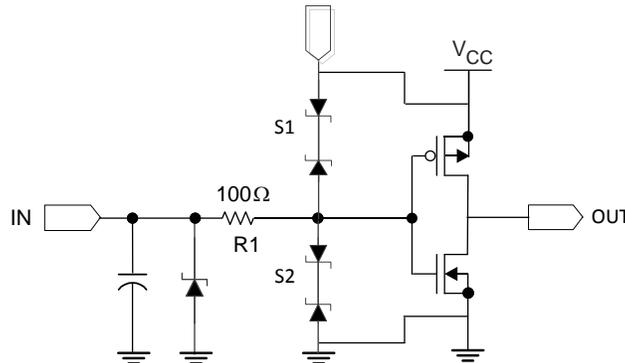


Figure 4. CMOS Input Circuits With ESD Diodes

In the event that there are no clamp diodes between the device inputs and the  $V_{CC}$  supply, the positive absolute maximum rating is a limitation of the process technology and is specified as an absolute voltage (that is, 5.5 V). Negative input-voltage rating may be exceeded if it is ensured that not too much current (less than  $I_{IK}$  maximum rating) is being passed through the ground-clamp diode. The  $I_{IK}$  absolute maximum rating specifies the maximum current that may be put through the ground-clamp diode.

### 4 CMOS Output Structure

#### 4.1 Drive Current

When strong current drive is required, one can connect the two outputs of the level-shifter to double the drive capability as shown in Figure 5. To prevent damaging the part, the following rules must be adhered to:

1. The two outputs must be from the same part
2. The two inputs and outputs should be adjacent pins and shorted with a trace between the two pins
3. The two outputs must be in the same state; high or low
4. The maximum current level of the component  $V_{CC}$  or GND as shown in the *Absolute Maximum Ratings* table of the data sheet ([SCES584](#)) should not be exceeded

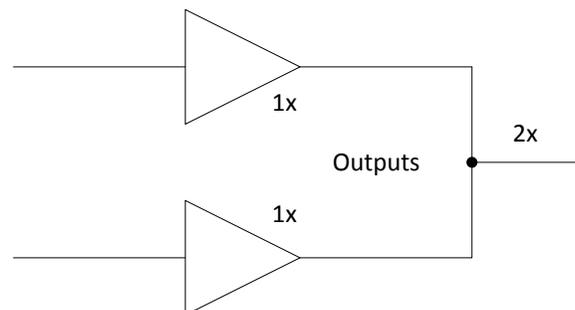


Figure 5. Connecting Two Output Together for Increased Drive Current

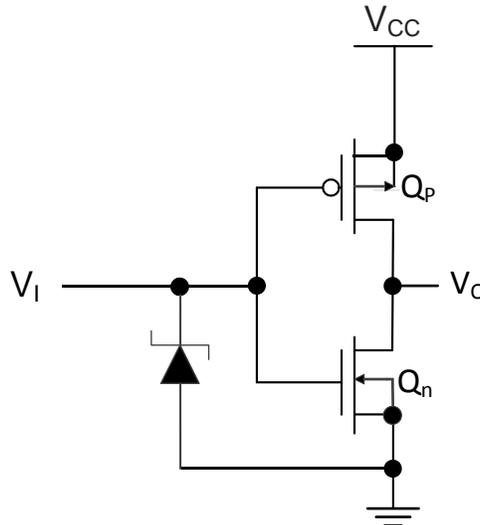
## 5 Floating Inputs With Non Bus-hold I/O

The LVC (no H in the part number) families have no bus-hold ([SCLA015](#)) on their inputs. In this configuration, the input impedance of the components is very high, limited to the leakage levels only.

Important design considerations:

- Inputs or I/O ports that do not have bus-hold should not be left floating. If the inputs are not tied high or low but are left floating, excessive output glitching or oscillations can result due to induced voltage transients on the parasitic lead inductance inherent to the device input and output structure.
- Unused non bus-hold inputs should be tied directly to  $V_{CC}$  or GND to achieve very low input power dissipation.
- All non bus-hold I/O ports that are not being driven should have a pull-up or pull down resistor attached. The exact value depends upon the tradeoffs between a quick recovery, after an I/O port shuts off, and low power dissipation if the I/O port should drive. The value of the resistor should be approximately 1 Kohm.

A circuit element that must be addressed when designing with a CMOS family, such as LVC, is circuit inputs. With the simplified totem-pole structure (see [Figure 6](#)) that characterizes the inputs of CMOS devices, the input node must be held as close to the  $V_{CC}$  or GND rails as possible. When the NMOS transistor ( $Q_n$ ) turns off and the PMOS transistor ( $Q_p$ ) turns on and begins to conduct, the output voltage ( $V_O$ ) is pulled high. Conversely, when  $Q_p$  turns off,  $Q_n$  begins to conduct and  $V_O$  is pulled low.



**Figure 6. Totem Pole Structure**

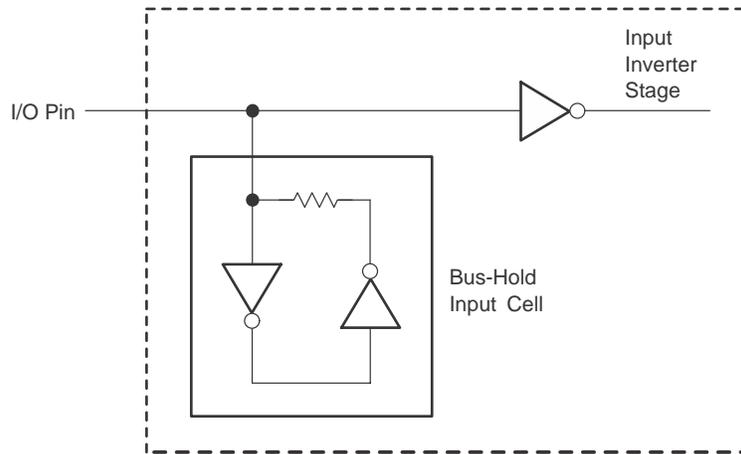
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**NOTE:** Precautions should be taken to prevent the input voltage from floating near the threshold voltage because this biases both input transistors on and creates undesirably high  $I_{CC}$  currents at the  $V_{CC}$  pin of the device. Under certain conditions, this can damage the device. One way to address this concern is to place external pullup resistors at any input that might be in a high-impedance, undriven state. This is costly in terms of component count, reliability, and board area.

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## 6 Floating Inputs With Bus-hold I/O

LVC devices with bus-hold circuitry are designated as LVCH. Bus hold is beneficial because of the decreased expense of purchasing additional resistors, reduced overall power consumption, and because it frees up limited board space.



**Figure 7. Typical Bus-Hold Cell**

The bus-hold circuit consists of two series inverters with the output fed back to the input through a resistor. This provides a weak positive feedback by sinking or sourcing current to the input node. The bus-hold cell holds the input at its last-known valid logic state until forcibly changed by a driving circuit. The input characteristics of the bus-hold are similar to a weak bistable latch. The bus-hold cell sinks current when the input is low, and sources current when the input is high. When the input voltage is near the threshold, the circuit sinks or sources maximum current to force the input node toward either the  $V_{CC}$  or GND rail.

Important design considerations:

- Generally, pull-up and pull-down resistors should not be used on the inputs of devices with bus-hold.
- In applications that require pull-up or pull-down resistors to hold the inputs at a specific logic level, the  $I_{I(\text{hold})}$  maximum specification should be considered. The resistor value should be chosen to overcome bus-hold under worst-case conditions. The resistor must supply enough current so that the input is pulled through the threshold to the desired logic level. If the current supplied is too weak, the input node could be held near the threshold, causing a high ICC that could damage the level-shifter.
- For bidirectional (transceiver) devices that have bus-hold on the data input/output pins, there will not be an  $I_{OZ}$  specification because the bus-hold output supplies enough current to overcome any internal output leakage.

## 7 Power Consumption Calculation

The continued industry trend is to make devices more robust and faster while reducing their size and power consumption. The LVC family of devices uses a CMOS output structure that has low power consumption and provides a medium drive current capability. ([SCAA035](#))

Total power consumption is the sum of static and dynamic power consumption.

$$P_{(\text{tot})} = P_{(\text{static})} + P_{(\text{dynamic})} \quad (1)$$

### 7.1 Static Power Consumption ( $P_{(\text{static})}$ )

This static power consumption is defined as quiescent, or  $P_{(\text{static})}$ , and can be calculated by [Equation 2](#).

$$P_{(\text{static})} = V_{\text{CC}} \times I_{\text{CC}} \quad (2)$$

Where:

- $V_{\text{CC}}$  = supply voltage
- $I_{\text{CC}}$  = current into a device (sum of leakage currents as in [Equation 2](#))

Another source of static current is  $\Delta I_{\text{CC}}$ . This results when the input levels are not driven all the way to the rail, causing the input transistors to not switch off completely.

### 7.2 Dynamic Power Consumption ( $P_{(\text{dynamic})}$ ):

The dynamic power consumption of a CMOS IC is calculated by adding the transient power consumption ( $P_T$ ), and capacitive-load power consumption ( $P_L$ ).

#### 7.2.1 Transient Power Consumption:

Transient power consumption is due to the current that flows only when the transistors of the devices are switching from one logic state to another. This is a result of the current required to charge the internal nodes (switching current) plus the through current (current that flows from  $V_{\text{CC}}$  to GND when the P-channel transistor and n-channel transistor turn on briefly at the same time during the logic transition). The frequency at which the device is switching, plus the rise and fall times of the input signal, as well as the internal nodes of the device, have a direct effect on the duration of the current spike. For fast input transition rates, the through current of the gate is negligible compared to the switching current. For this reason, the dynamic supply current is governed by the internal capacitance of the IC and the charge and discharge current of the load capacitance.  $C_{\text{pd}}$  is an important parameter in determining dynamic power consumption in CMOS circuits. It includes both internal parasitic capacitance (e.g., gate-to-source and gate-to-drain capacitance) and through currents present while a device is switching and both n-channel and p-channel transistors are momentarily conducting.

Transient power consumption can be calculated :

$$P_T = C_{\text{PD}} \times V_{\text{CC}}^2 \times F_I \times N_{\text{SW}} \quad (3)$$

Where:

- $P_T$  = transient power consumption
- $V_{\text{CC}}$  = supply voltage
- $F_I$  = input signal frequency
- $N_{\text{SW}}$  = number of bits switching
- $C_{\text{PD}}$  = dynamic power-dissipation capacitance.

### 7.2.2 Capacitive-Load Power Consumption

Additional power is consumed in charging external load capacitance and is dependent on switching frequency. The following equation can be used to calculate this power if all outputs have the same load and are switching at the same output frequency.

$$P_L = C_L \times V_{CC}^2 \times F_O \times N_{SW} \quad (C_L \text{ is the load per output}) \quad (4)$$

Where:

- $P_L$  = capacitive-load power consumption
- $V_{CC}$  = supply voltage
- $F_O$  = output signal frequency
- $C_L$  = external (load) capacitance
- $N_{SW}$  = total number of outputs switching

Therefore, dynamic power consumption ( $P_D$ ) is the sum of these two power consumptions :

$$P_D = P_T + P_L$$

$$P_D = (C_{PD} \times F_I \times V_{CC}^2) + (C_L \times F_O \times V_{CC}^2)$$

$$P_D = [(C_{PD} \times F_I \times N_{SW}) + \sum(C_{Ln} \times F_{On})] \times V_{CC}^2 \quad (5)$$

Where:

- $C_{PD}$  = power consumption capacitance (F)
- $F_I$  = input signal frequency (Hz)
- $F_{ON}$  = all different output signal frequencies at each output numbered 1 through n (Hz)
- $N_{SW}$  = total number outputs switching
- $V_{CC}$  = supply voltage
- $C_{Ln}$  = all different load capacitance at each output numbered 1 through n.

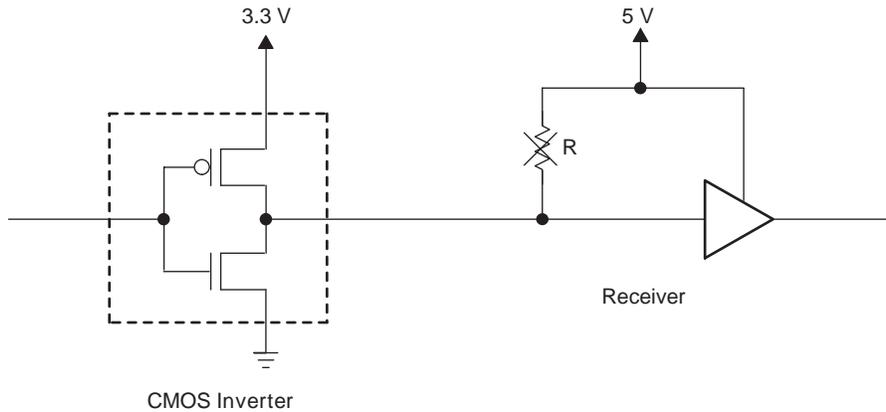
Note: The operating characteristics section of the datasheet ([SCES584](#)) includes the parameter that specifies the power-dissipation capacitance (Cpd) in a CMOS device. For additional information on how Cpd is measured and used to calculate total CMOS-device power consumption in the application, refer to the TI application report, *CMOS Power Consumption and Cpd Calculation* ([SCAA035](#)).

Total power consumption is the sum of static and dynamic power consumption.

$$P_{(tot)} = P_{(static)} + P_{(dynamic)} \quad (6)$$

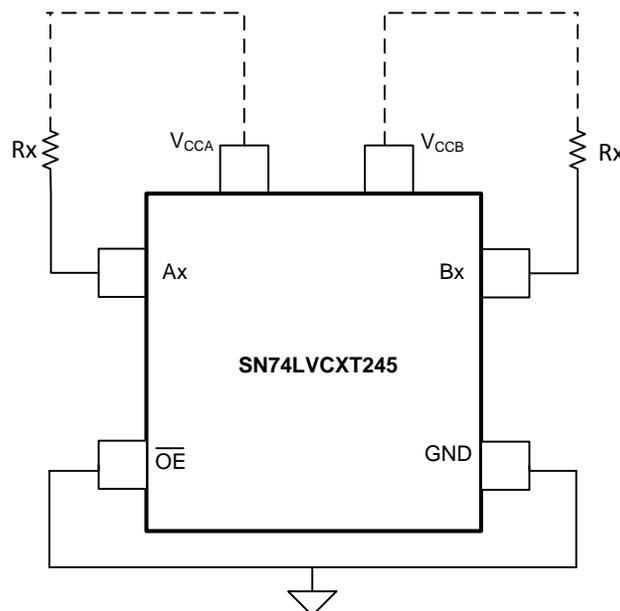
## 8 Pull-up Resistors at Inputs/Outputs of CMOS Drivers

To achieve level translation, system designers should not use a pull-up resistor at the output of a device with CMOS (push-pull) outputs. This technique has several flaws and should be avoided. One drawback is increased power consumption whenever the output switches low. Another problem occurs when the output of the CMOS driver is high. In this state, the lower N-channel transistor is off, while the upper P-channel transistor is on. This results in a backflow of current from the high supply to the low supply through the resistor R and the upper P-channel transistor. This current flow into the low supply could cause undesirable effects.



**Figure 8. Avoiding Pull-up Resistors at Output**

Pull-up resistors are recommended on input ports ( $R_x$  is connected on  $A_x$  or  $B_x$ , whichever is the input), when the part is powered up in a permanently enabled state. This ensures proper/glitch free operation during power up. The value of the pull-up resistor needs to be such that the input follows its supply voltage  $V_{CC}$ , as it ramps up. If the designer can ensure a high state at the input during power up, pull-up resistors are not needed.



**Figure 9. Pull-up Resistors on Inputs**

## 9 Partial Power Down Feature

To partially power down a device, no paths from  $V_I$  to  $V_{CC}$  or from  $V_O$  to  $V_{CC}$  can exist. The inputs and outputs of the LVC logic family have been designed with all reverse-current paths to  $V_{CC}$  blocked. This low  $I_{OFF}$  current feature allows the device to remain electrically connected to a bus during partial power down without loading the remaining live circuits. This feature also allows the use of this family in a mixed-voltage environment. If the inputs or outputs are at a voltage greater than the  $V_{CC}$  of the device, there is no current sourcing back through the device from the higher voltage node to the lower voltage  $V_{CC}$  supply.

$I_{OFF}$  protection circuitry ensures that no excessive current is drawn from or to an input, output, or combined I/O that is biased to a specified voltage while the device is powered down. In this case, the device is said to support partial-power-down mode of system operation. This condition can occur when subsections of a system are powered down (partial power down) to reduce power consumption. For p-channel transistors, which are directly connected to external pins, the back gate is blocked with a diode to prevent excess currents flowing from the external pin to the supply voltage  $V_{CC}$ , when the output voltage is greater than  $V_{CC}$  by at least 0.7 V. This blocking diode and additional FET circuitry (to prevent the upper output P-channel from turning on during a partial-power-down event) constitute the partial power down sub circuitry and eliminate the path from  $V_O$  to  $V_{CC}$ .

## 10 $V_{CC}$ Isolation Feature

If either of the  $V_{CC}$  inputs are at GND ( $< 0.4$  V), all of the outputs are in high impedance state. [Table 1](#) shows the I/O states.

**Table 1. Logic Table for  $V_{CC}$  Isolation Feature**

$V_{CCA}$	$V_{CCB}$	OE	Translator I/O s
$<0.4V$	H	X	High-Z
H	$<0.4V$	X	High-Z
H	H	L	High-Z
H	H	H	Active

## 11 Possible Translation Combinations With LVC Parts

**Table 2. Translation Combinations**

Device	Supply Voltage	Possible Voltage-Translation Combinations	
		A Port	B Port
SN74LVC1T45	$1.65\text{ V} \leq V_{CCA} \leq 5.5\text{ V}$ $1.65\text{ V} \leq V_{CCB} \leq 5.5\text{ V}$	1.8-V CMOS	1.8-V CMOS, 2.5-V CMOS, 3.3-V LVCMOS/LVTTL, 5-V CMOS
SN74LVC2T245		2.5-V CMOS	1.8-V CMOS, 2.5-V CMOS, 3.3-V LVCMOS/LVTTL, 5-V CMOS
SN74LVC8T245, SN74LVCH8T245		3.3-V LVCMOS/LVTTL	1.8-V CMOS, 2.5-V CMOS, 3.3-V LVCMOS/LVTTL, 5-V CMOS
SN74LVC16T25, SN74LVCH16T25		5-V CMOS	1.8-V CMOS, 2.5-V CMOS, 3.3-V LVCMOS/LVTTL, 5-V CMOS

## 12 Acknowledgement

The author thanks Oscar Moreira-Tamayo for reviewing the document and providing meaningful feedback.

## 13 References

*Understanding and Interpreting Standard-Logic Data Sheets*, [SZZA036](#)

*AVC Logic Family Technology and Applications*, [SCEA006](#)

*Implications of Slow or Floating CMOS Inputs*, [SCBA004](#)

*Bus-Hold Circuit*, [SCLA015](#)

*CMOS Power Consumption and Cpd Calculation*, [SCAA035](#)

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