TI 设计：TIDA-01355

采用 73dB SNR、7.5MSPS 时间交织 SAR ADC 且适用于成像应用的模拟前端参考设计

说明

此参考设计展示了如何以较低的 BOM 成本实现高采样频率和高分辨率的多个交错式 ADC。此参考设计在构建时考虑到了电子成像系统的一些要求。高清成像和其它高速信号处理 应用 需要使用 ADC 才能实现高分辨率、高 SNR、高速和低功耗等特性。借助单个芯片无法始终满足这些要求。通过实施多个交错式 SAR ADC，该设计可优化不同 ADC 之间的优缺点，以满足所有系统要求。

资源

TIDA-01355	设计文件夹
TINA-TI™	SPICE 仿真器
ADS7056	产品文件夹
OPA836	产品文件夹
REF2033	产品文件夹
SN74AUCH244	产品文件夹
LP5907	产品文件夹

TI E2E™ Community

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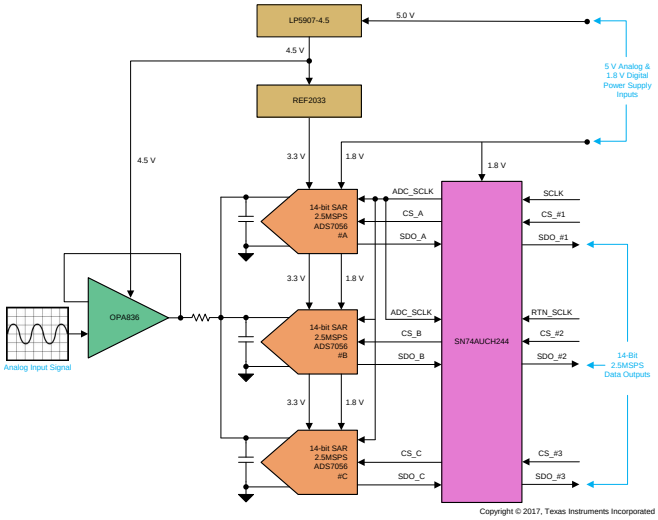
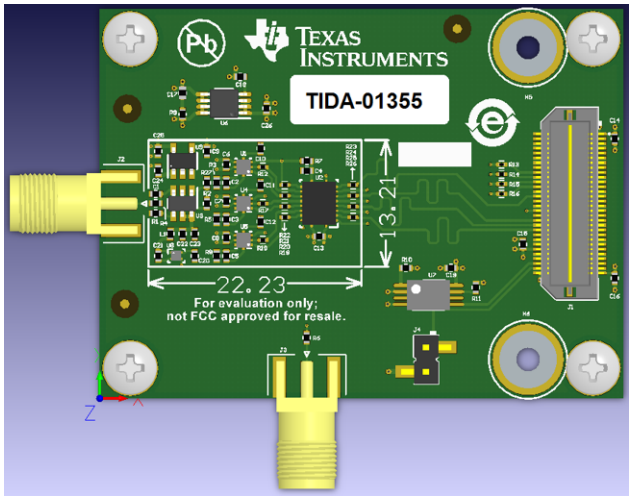
特性

- 分辨率：14 位
- 输入类型：单极单端
- 系统 SNR：> 73dB
- 系统 ENOB：12 位
- 系统 THD：< –84dB
- 功耗：< 33mW
- 与管线式 ADC 的解决方案相比，延迟更低
- 小封装尺寸：22mm × 13mm

应用范围

- 热成像摄像机
- 手持热成像仪
- 医疗成像系统





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1 System Description

Applications with high-speed signal processing such as high definition imaging require ADCs that can meet the characteristics of high resolution, high SNR, high speed, and low power consumption. Some ADC architectures like flash and pipeline achieve a high sampling rate but do not have the best SNR and are very power hungry architectures. Other ADC architectures like SAR or Delta-Sigma achieve very good SNR but their sampling rate is limited. Because all these requirements cannot always be met with a single chip, they demand creativity from the system designers.

The TIDA-01355 design presents an alternate solution to this problem. Instead of flash or pipeline ADC architectures, this TI Design uses time-interleaved SAR ADCs. This reference design takes electronic imaging systems as an example to demonstrate how to implement interleaving using multiple low-power SAR ADCs to achieve higher sampling rates at a reasonably high resolution and low cost. Time interleaving provides clear advantages in terms of power and speed. However, these advantages do not come for free. Mismatches among multiple paths of the signal chain result in substantial spurious content in the output spectrum. Correcting unwanted interleaving spurs might come at a heavy cost in terms of complexity and power. Understanding which errors are most significant and which can be ignored in any given application is important for selecting an appropriate calibration scheme.

This design guide addresses component selection, design theory, and test results of the TI Design system. The scope of this design guide gives system designers a head start in integrating TI's amplifier, SAR ADC, voltage reference, and power management devices into their end-equipment systems. This reference design provides a complete set of downloadable documents such as comprehensive design guide, schematic, Altium PCB layout files, bill of materials (BOM), test results, and Gerber files that help system designers in the design and development of their end-equipment systems. The following subsections describe the various blocks within the TI Design system and what characteristics are most critical to best implement the corresponding function.

1.1 Key System Specifications

表 **1. Key System Specifications**

PARAMETER	SPECIFICATIONS
Number of channels	One
Input type	Single-ended unipolar
Input range	0.3 to 3.3 V
Number of interleaved ADCs	Three SAR ADCs (part number: ADS7056)
Resolution	14-bit
System SNR	> 73 dB
System ENOB	> 12-bit
System THD	< –84 dB
Sampling frequency	7.5 MSPS with three interleaved ADCs
Calibration	Offset calibration
Operating voltage	USB powered; no external power supply is required Precision host interface (PHI) controller card supplies 5-V DC, 1.8-V DC
Power consumption	≈ 33 mW
Connector	One SMA connector (J2) for analog input signal one high-speed 30×2 Samtec connector (J1) for PHI controller card
Form factor	22.5 mm × 13.5 mm

2 System Overview

2.1 Block Diagram

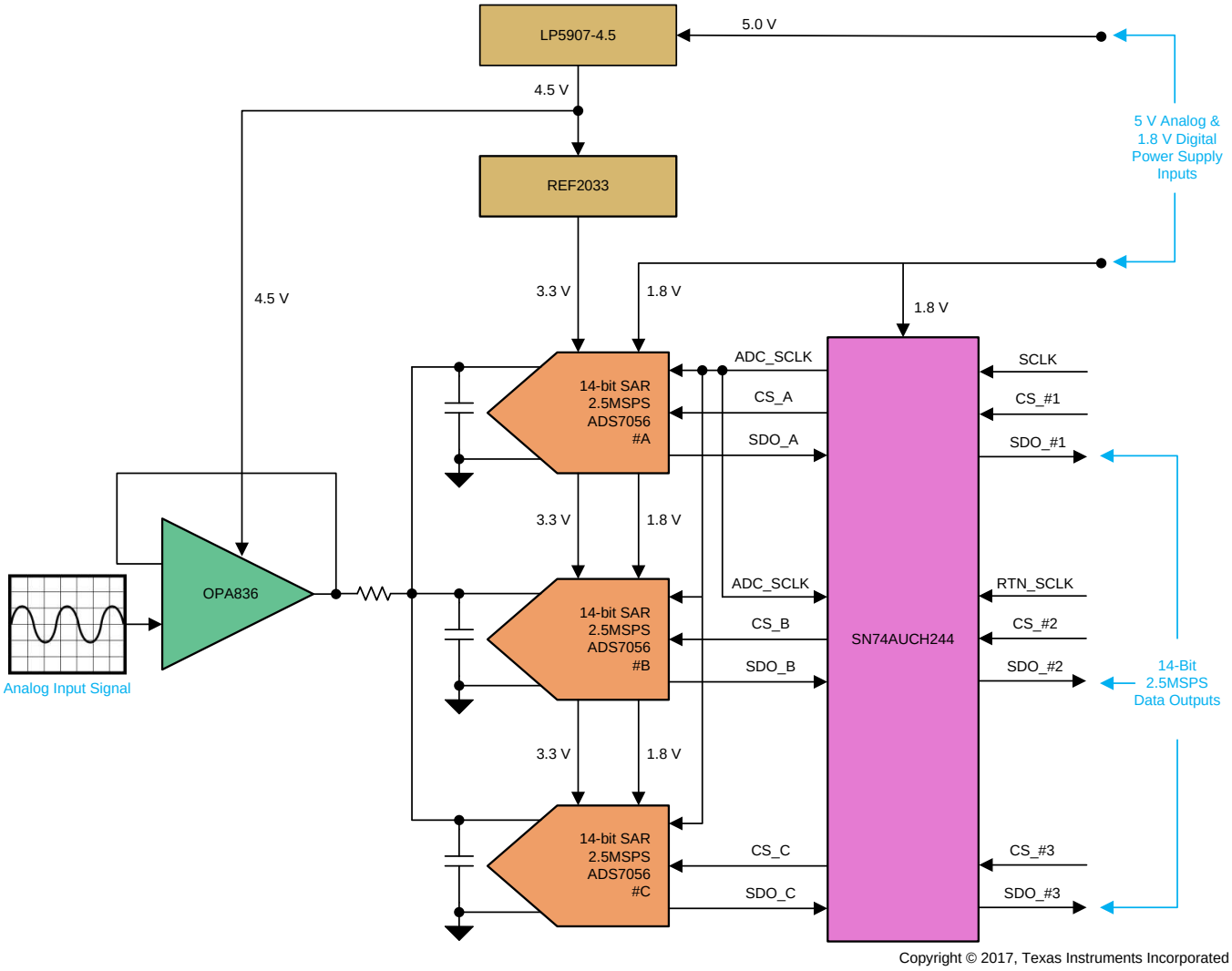

图 **1. Block Diagram of TIDA-01355**

2.2 Highlighted Products

The TIDA-01355 design features the following devices:

- ADS7056: Ultra-Low-Power, Ultra-Small Size, 14-Bit, High-Speed SAR ADC
- OPA836: Very-Low-Power, Rail-to-Rail Out, Negative Rail In, Voltage-Feedback Operational Amplifier
- REF2033: Low-Drift, Low-Power, Dual-Output VREF and VREF/2 Voltage Reference
- SN74AUCH244: Octal Buffer/Driver With Three-State Outputs
- LP5907: 250-mA Ultra-low-Noise Low-IQ LDO

For more information on each of these devices, see their respective product folders at TI.com.

2.2.1 ADS7056

Features:

- 2.5-MSPS throughput
- Ultra-small sized SAR ADC:
  - X2QFN-8 package with 2.25-mm^2 footprint
- Wide operating range:
  - AVDD: 2.35 to 3.6 V
  - DVDD: 1.65 to 3.6 V (independent of AVDD)
  - Temperature range: –40°C to 125 °C
- Unipolar input range: 0 V to AVDD
- Excellent performance:
  - 14-bit NMC DNL, ±2-LSB INL
  - 74.5-dB SINAD at 2-kHz
  - 73.7-dB SINAD at 1-MHz
- Ultra-low-power consumption:
  - 3.5 mW at 2.5-MSPS with 3.3-V AVDD
  - 158 µW at 100-kSPS with 3.3-V AVDD
- Integrated offset calibration
- SPI-compatible serial interface: 60 MHz
- JESD8-7A Compliant Digital I/O

Applications:

- Sonar receivers
- Optical line cards and modules
- Thermal imaging
- Ultrasonic flow meters
- Motor controls
- Handheld radios
- Fire and smoke detection

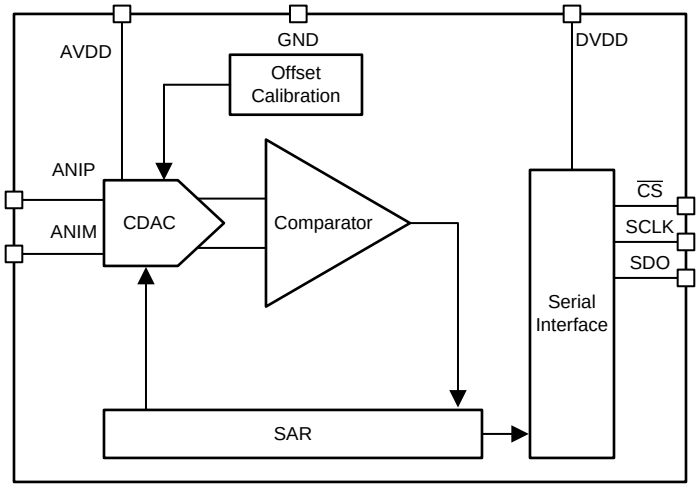

图 **2. Functional Block Diagram of ADS7056**

2.2.2 OPA836

Features:

- Low power:
  - Supply voltage: 2.5 to 5.5 V
  - Quiescent current : 1 mA (typical)
  - Power down mode : 0.5 µA (typical)
- Bandwidth: 206 MHz
- Slew rate: 560 V/µs
- Excellent performance:
  - SNR: 0.00013% (–117.6 dBc) at 1 kHz (1 V_{RMS})
  - THD: 0.00013% (–130 dBc) at 1 kHz (1 V_{RMS})
  - HD_2/HD_3: –85 dBc/–105 dBc at 1 MHz (2 V_{PP})
- Input voltage noise: 4.6 nV/√Hz (f = 100 kHz)
- CMRR: 116 dB
- RRO: Rail-to-rail output

Applications:

- Low-power signal conditioning
- Audio ADC input buffers
- Low-power SAR and ΔΣ ADC drivers
- Low-power systems
- High-density systems
- Portable systems

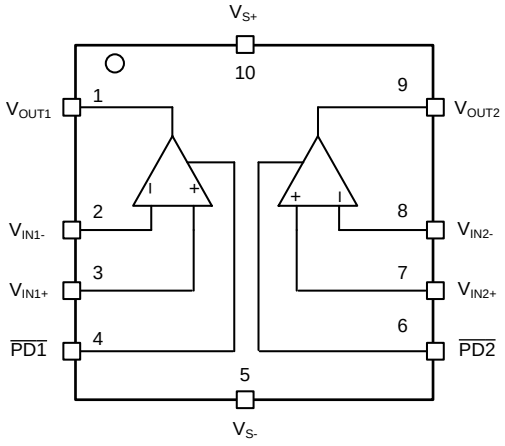

图 **3. Pin Diagram of OPA836**

2.2.3 REF2033

Features:

- Two outputs, V_{REF} and $V_{REF}/2$, for convenient use in single-supply systems
- Excellent temperature drift performance:
  - 8 ppm/°C (max) from –40°C to 125°C
- High initial accuracy: ±0.05% (max)
- V_{REF} and V_{BIAS} tracking overtemperature:
  - 6 ppm/°C (max) from –40°C to 85°C
  - 7 ppm/°C (max) from –40°C to 125°C
- Low dropout voltage: 10 mV
- High output current: ±20 mA
- Low quiescent current: 360 μA
- Regulation:
  - Line regulation: 3 ppm/V
  - Load regulation: 8 ppm/mA

Applications:

- Digital signal processing
- Current sensing
- Industrial process controls
- Medical equipment
- Data acquisition systems

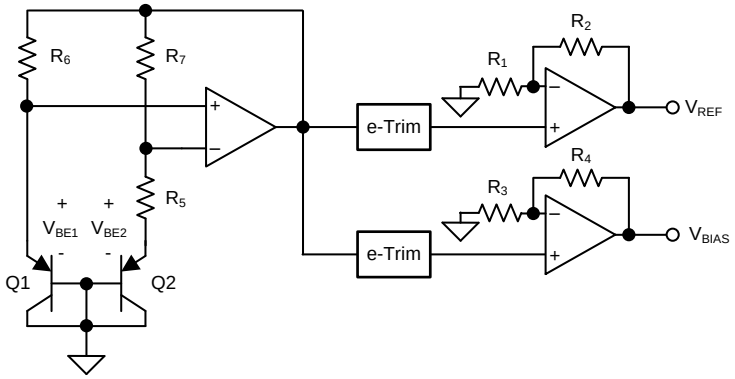

图 **4. Functional Block Diagram of REF2033**

2.2.4 SN74AUCH244

Features:

- Optimized for 1.8-V operation and is 3.6-V I/O tolerant to support mixed-mode signal operation
- I_{off} supports partial-power-down mode operation
- Max t_{pd} of 1.9 ns at 1.8 V
- Low power consumption, 20- μA max I_{CC}
- ±8-mA output drive at 1.8 V

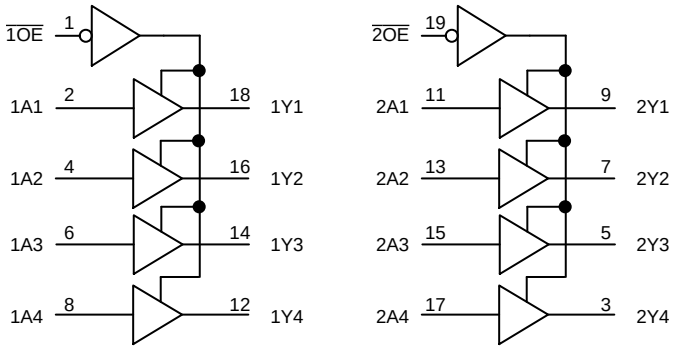

图 **5. Functional Block Diagram of SN74AUCH244**

2.2.5 LP5907

Features:

- Input voltage range: 2.2 to 5.5 V
- Output voltage range: 1.2 to 4.5 V
- Very low I_q (enabled): 12 µA
- Low output voltage noise: < 6.5 μV_{RMS}
- PSRR: 82 dB at 1 kHz
- Low dropout: 120 mV (typical)

Applications:

- Mobile phones, tablets
- Current sensing
- Digital cameras and audio phones
- Portable and battery-powered equipment
- IP cameras and drones

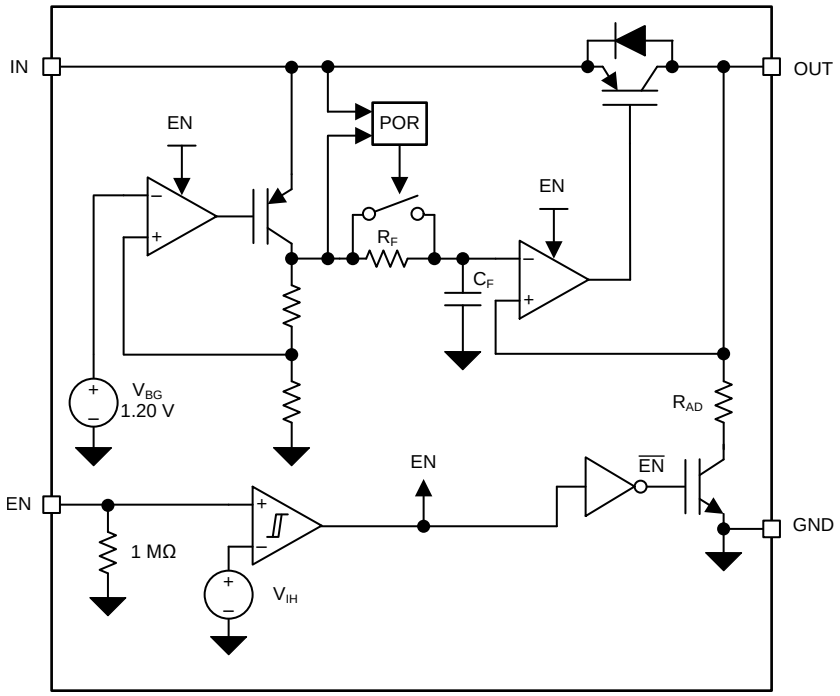

图 **6. Functional Block Diagram of LP5907**

2.3 System Design Theory

2.3.1 Theory of Operation

Time interleaving is a smart technique to achieve an overall high sample rate by operating multiple identical, lower sampling rate ADCs in parallel. In time-interleaved architecture, a system of n number of N-bit ADCs are used, which alternately take one sample at a time as shown in 图 7. As a rule of thumb, operating n number of ADCs in parallel increases the system's sampling rate by approximately a factor of n as given in 公式 1. The result is that the sample rate is increased n times compared to what each individual ADC can manage. For example, by interleaving three 14-bit, 2.5-MSPS ADCs one could in principle realize a 14-bit, 7.5-MSPS ADC. The chip-select (ADC CS) of each ADC is controlled to take the sample of input signal at slightly different instants and finally the sampled data is combined in to one data stream at the output.

$$f_{SYSTEM} = n \times f_{ADC} \quad (1)$$

Where:

- n is number of ADCs in the system
- f_{ADC} is sampling speed of individual ADC
- f_{SYSTEM} is sampling speed of time-interleaved system

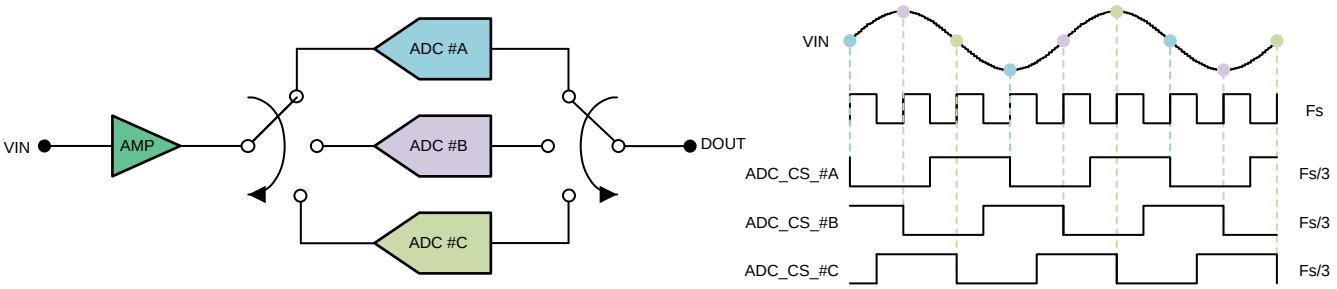

图 7. Three Time-Interleaved ADCs

For time interleaving, the phase relationship between ADC chip-select signals is given by 公式 2:

$$\text{Phase}\left(\theta_K\right) = 2 \times \pi \times \left(k - \frac{1}{n}\right) \quad (2)$$

Where:

- k is sequence in which ADC is given chip-select signal
- n is number of ADCs in the system

To achieve a 7.5-MSPS sampling speed, each ADC should run at full throughput of 2.5 MSPS, which requires an SPI clock (SCLK) frequency of 60 MHz (one clock period = 16.67 ns). From 图 8, the conversion process requires a minimum of 18 SCLK falling edges to be provided within the frame. After the end of conversion process, the device automatically moves from CNV state to ACQ state. To acquire the next sample, a minimum acquisition time of 95 ns must be provided. In terms of SCLK cycles, 95 ns corresponds to six clocks cycles. Therefore, one ADS7056 needs 24 clock cycles to complete the ACQ and CNV processes. The falling edge on the chip-select signal indicates the start of CNV state. After the end of CNV state, the device automatically enters into ACQ state. Thus, for a system that uses three ADCs in time-interleaved manner, phase difference between chip-select signals should be 120 degrees. This difference can be achieved by keeping chip-select signals for each ADC by eight clock cycles apart from each other (24 SCLK / divide by of ADCs) as shown in 图 9.

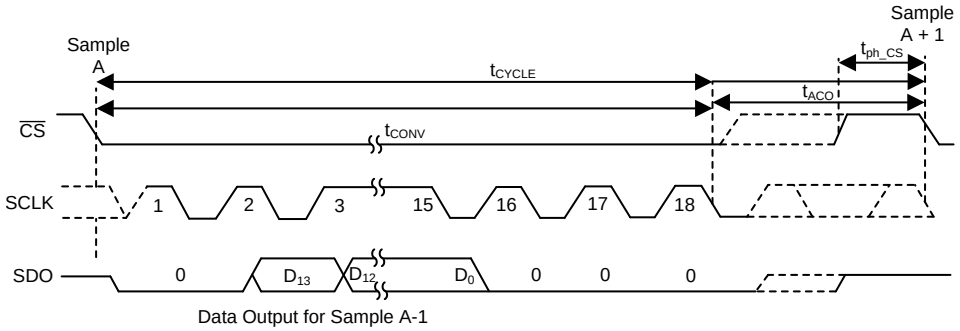

图 8. Serial Interface Timing Diagram of ADS7056

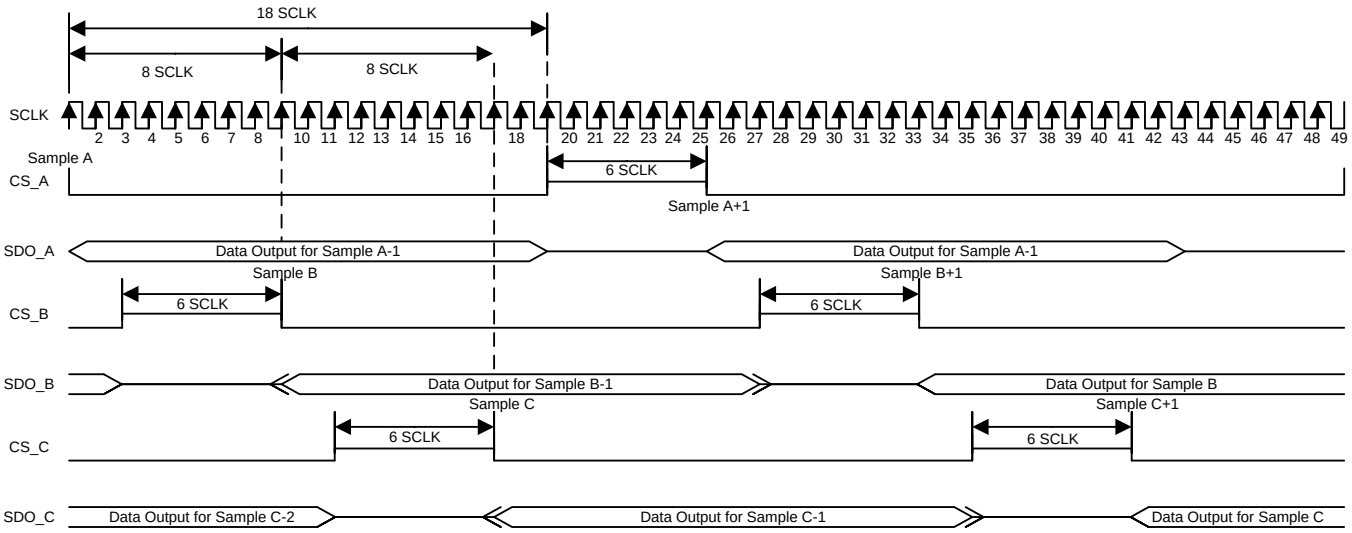

图 9. Timing Diagram to Achieve 7.5 MSPS With Three ADS7056s Using Time-Interleaved Technique

2.3.2 Challenges With Interleaving

Time-interleaved systems provide clear advantages in terms of power and speed because of clever architectural innovations with lower-speed circuits.

However, this powerful technique is not free from practical challenges. The very nature of interleaving forces the input signal to traverse through multiple paths on its way to the output. The major challenge of time-interleaved systems is the substantial spurious content in the output spectrum, called "interleaving spurs" due to untreated mismatch among different subsections. These interleaving spurs or artifacts can be seen as time-domain fixed pattern noise. On the practical side, an interleaving digitizing system will suffer some performance penalty. The amount of degradation depends on how well the converters are matched and how much digital signal processing the designer is willing to do. Although ADCs used in time-interleaved system are identical, they still possess mismatches with respect to offset, gain, timing, and bandwidth coming from unavoidable random variations during semiconductor processing. The gain and offset mismatches are considered as DC effects, whereas the effects of timing and bandwidth mismatch become worse at higher frequency analog inputs.

Various forms of calibration are used to correct these mismatches in order to reduce the spurs. Gain and offset mismatch correction are the most straightforward ones; however, correcting timing and bandwidth mismatches might become more tricky and complex. Choosing an appropriate calibration scheme greatly depends on the intended application as errors impact various systems quite differently. Therefore, calibrating only what is important can lead to a more efficient design.

As discussed already, this TI Design takes an example of imaging systems. The analog video output of an image sensor is pseudo-DC waveform that resembles to a series of steps with different DC levels. In each cycle, pixel information is contained in the lower portion of the waveform. The characteristics of video waveform dictate time rather than frequency. ADC samples the analog video signal only during a relatively slow-moving portion of the waveform, preferably in the end where pixel is most settled. Therefore, electronic imaging differs for signal reconstruction applications as it is strictly a time domain data acquisition application. In time domain applications, the spectral purity is not very important. The main focus of this TI Design is on minimizing errors due to DC mismatches (offset and gain) rather than putting efforts on optimizing AC mismatches (bandwidth and timing).

The first considerations are offset and gain mismatches. 图 10 shows two interleaved converters digitizing a sine wave. Converter A has an offset problem and converter B a gain problem. The digitized codes represent not only the original sine wave but also an error signal. In the discrete digital domain, the error signal is seen to contain two sine frequencies. The first one is a frequency of half the sample rate (due to the offset error), and the other with a frequency of half the sample rate minus the frequency of the original input signal (due to the gain error). The offset mismatch introduces tones at fixed frequency with power proportional to amount of mismatch. The gain mismatch generates errors that are amplitude modulated with input frequency.

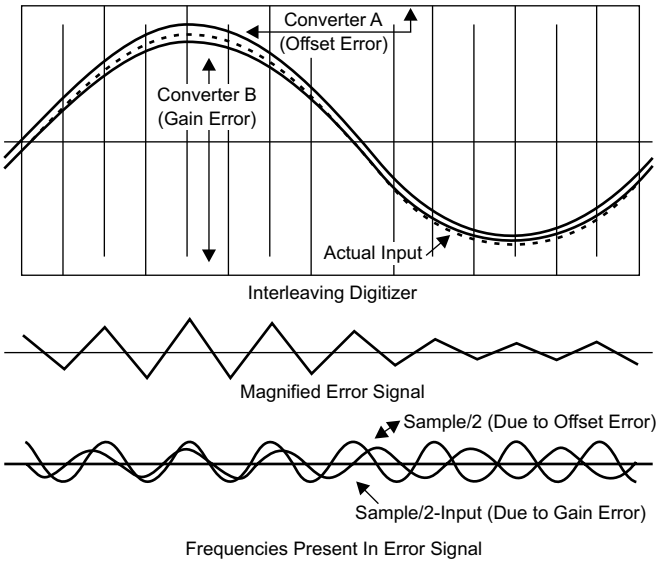

图 10. Digitized Signal of Two Time-Interleaved Converters

The next consideration is bandwidth mismatch. A sensor's video output is a pseudo-DC signal. Therefore, it is possible to encounter a full-scale change between adjacent pixels (or two consecutive conversions). The frequency content of resulting waveform can greatly exceed the Nyquist frequency derived from the ADC sampling rate. These high-frequency contents in the waveform do not contain any information of interest but must be processed by the ADC input circuitry. The insufficient BW of the ADC input circuitry may degrade system performance.

The last consideration is timing mismatch. The error due to timing mismatch can be ignored as the ADCs take the sample of settled pixel voltage.

With careful design, many of these problems can be greatly reduced. Consider the following aspects:

- Single amplifier to drive all interleaving ADCs: Helps in minimizing the errors due to offset mismatch among multiple analog signal paths. This way spurs are limited by the offset mismatch among ADCs. Therefore, select ADCs with lower offset error or with internal offset correction feature. The ADS7056 has a calibrated offset error of ±6 LSBs (max). The device also has internal offset calibration and correction capabilities. The device enters to enter OFFCAL state when host controller provides 24 SCLK cycles. In OFFCAL state, the sampling capacitors are disconnected from the analog input pins (AINP and AINM). The offset calibration is effective for all the subsequent conversions till the device is powered off. An offset calibration cycle is recommended at power-up and whenever there is a significant change in the operating conditions for the device (AVDD voltage and operating temperature).
- Single external voltage reference for all interleaving ADCs: Helps in minimizing the errors due to gain mismatch. Gain mismatch is mainly related to the accuracy of ADC's internal voltage reference. Select an ADC that supports operation with external voltage reference. The ADS7056 uses analog supply voltage (AVDD) as the voltage reference for analog-to-digital conversion.
- ADCs with wide enough bandwidth: During production, the components (sampling switch resistance and sampling cap) of the ADC's internal sampling circuit can vary. The easiest way to deal with this problem is to select an ADC with a full-power BW at least 100 times the half of the sampling rate. The full-power BW of the ADS7056 is 200 MHz, which is much higher than the half of sampling rate (1.25 MSPS). ADC input circuitry is much faster. As a result, the error due to BW mismatch among

ADCs can be ignored for imaging (multiplexed input) applications.

2.3.3 Component Selection

2.3.3.1 Front-End Design

An ADC input driver circuit mainly consists of two parts: a driving amplifier and a flywheel RC filter as shown in 图 11. The amplifier is used for signal conditioning of the input voltage, and its low-output impedance provides a buffer between the signal source and the ADC input. The RC filter helps attenuate the sampling charge-injection from the switched-capacitor input stage of the ADC as well as acts as an antialiasing filter to band-limit the wideband noise contributed by the front-end circuit. The design of the ADC input driver involves optimizing the bandwidth of the circuit, driven primarily by the following requirements:

- The RC filter bandwidth must be low enough to band-limit the noise fed into the input of the ADC, thereby increasing the signal-to-noise ratio (SNR) of the system.
- The overall system bandwidth must be large enough to accommodate optimal settlings of the input signal at the ADC input before the start of conversion.

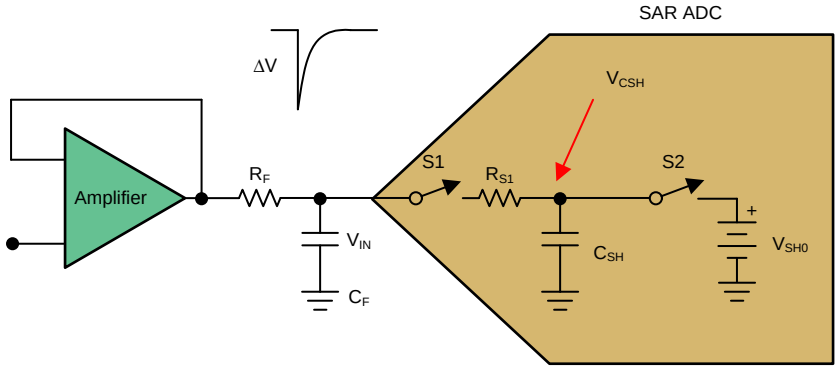

图 **11. Analog Front End for SAR ADC**

The topology of the capacitive digital-to-analog converter (CDAC)-SAR ADCs contains a capacitive-redistribution network. 图 12 shows a simplified model of the SAR input stage. The equivalent input elements for the CDAC-SAR ADC include an internal input R-C pair (R_{S1}, C_{SH}), two switches (S1, S2), and a V_{SH0}. The initial voltage across the sampling capacitor, C_{SH}, is V_{SH0}. This voltage can be equal to the previous conversion, ground, or V_{REF} (depending on the converter input structure). Signal acquisition occurs by opening S2 and closing S1. With the closure of S1, the voltage across the sample capacitor (C_{SH}) changes to V_{IN}. Charge from the voltage source, V_{IN}, passes through the sampling switch path of S1 and R_{S1} onto C_{SH}. As this process is accomplished, the charge previously on C_{SH} changes so that V_{CSH} equals V_{IN}. The device datasheet shows the equivalent input analog circuit that provides the values of an internal input R-C pair (R_{S1}, C_{SH}). For example, the ADS7056 datasheetshows that the input switch resistance R_{S1} is 50 Ω and the sampling capacitor C_{SH} is 16 pF.

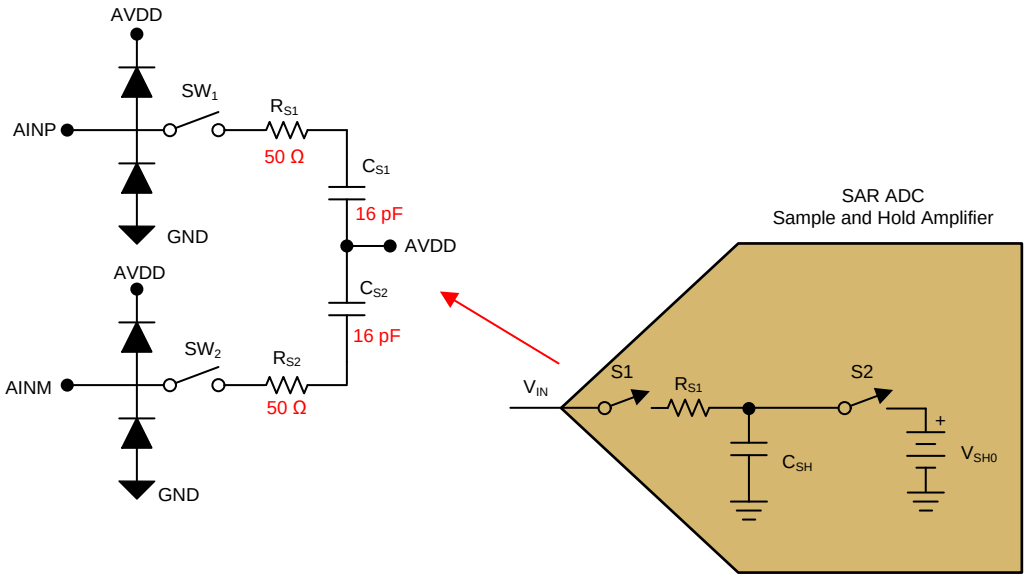

图 12. Equivalent Input Circuit for Sampling Stage

There are two distinctive stages to ADC operation. The datasheet specifies these two timings as acquisition time (t_{ACQ}) and conversion time (t_{CONV}). For the ADS7056, the minimum acquisition time (t_{ACQ}) is 95 ns. From 图 13 shows that during this time the sampling switch S1 is closed, and the sampling capacitor C_{SH} is connected to the analog input signal. The minimum conversion time (t_{CONV}) for this converter is specified as 18 × t_{SCLK}. To have maximum throughput, keep this value at the minimum. During the conversion time, the sampling switch is open and the sampling capacitor is disconnected from the input signal.

Parameter		Test Conditions	MIN	TYP	MAX	Unit
Sampling Dynamics						
t_{CONV}	Conversion time			18 × t_{SCLK}		ns
t_{ACQ}	Acquisition time		95			ns
f_{SAMPLE}	Maximum throughput rate	60-MHz SCLK, AVDD = 2.35 V to 3.6 V			2.5	MHz
	Aperture delay			3		ns
	Aperture jitter, RMS			12		ps

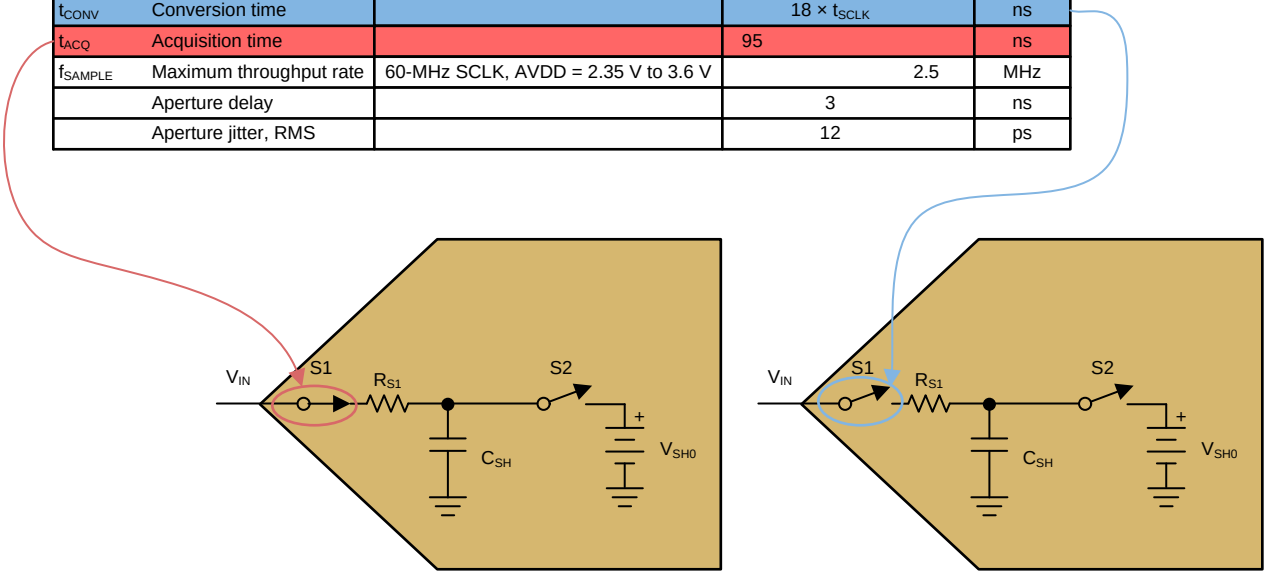

图 **13. State of Internal Sampling Switch With Respect to ACQ and CNV Timings**

From the ADS7056 datasheet, observe the serial interface timing diagram. After the end of conversion process, the ADS7056 automatically moves from conversion state to acquisition state. As discussed previously, during the acquisition time, the input sampling switch is closed, and during the conversion time, the same switch is open. The most critical moment that determines the accuracy of this TI Design occurs at the moment when the sampling switch is opened.

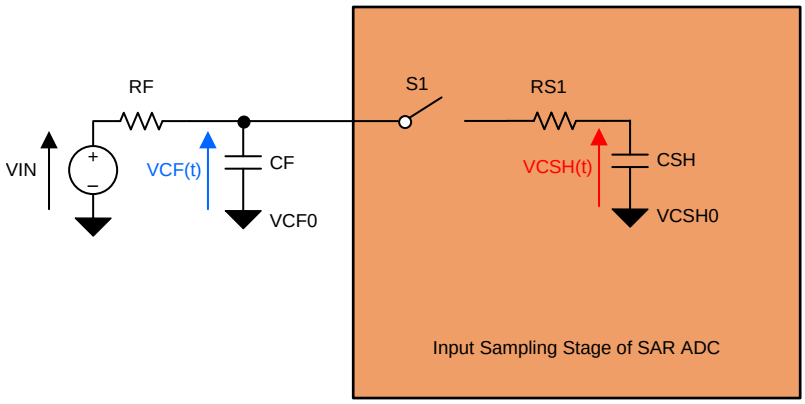

图 **14. SAR ADC Input With External RC Filter**

From 图 14, with an assumption $V_{CF0} > V_{CSH0}$, the sampling capacitor (C_{SH}) is quickly charged at first by the energy of the external input capacitor through R_{S1} at the start of the conversion. The process of charging the sampling capacitance causes a voltage drop (or peak) across external input capacitor C_F as shown in 图 15. The subsequent process of charging the sampling capacitor is much slower due to this higher input impedance. The acquisition time must be properly set while considering the time constant of the sampling capacitor charging. Hence, the external RC components essentially affect the accuracy of the analog-to-digital conversion. The magnitude of the voltage drop across the input capacitor (C_F) at the time switch S1 is closed as given in 公式 3:

$$\Delta V = \frac{C_{SH}}{C_F + C_{SH}} \times \left(V_{CF0} - V_{CSH0}\right) = \frac{1}{\frac{C_F}{C_{SH}} + 1} \times \left(V_{CF0} - V_{CSH0}\right) \quad (3)$$

A higher ratio between the input capacitor and sampling capacitor produces a smaller voltage drop. The input capacitor C_F helps to reduce the kickback noise at the ADC input and provides a charge bucket to quickly charge the input capacitor C_{SH} during the sampling process. The value of the capacitor C_F must be chosen such that when switch S1 closes, the voltage droop (ΔV) on C_F is less than 5% of the input voltage. Therefore, the generalization show in Equation 4 can be used to estimate the necessary size of the external capacitor C_F.

$$C_F \geq 20\, C_{SH} \quad (4)$$

Based on Equation 4 and value of C_{SH} (= 16pF),

$$C_F \geq 320\ pF \quad (5)$$

For low distortion, the external filter capacitor (C_F) must be a C0G/NP0 type. C0G type capacitors exhibit minimal change in capacitance over input voltage, frequency, temperature, and so on, and are typically available in values of 10 nF or less. Thus, a C0G type capacitor with a value of C_F = 330 pF is selected for this TI Design.

At this point, it is important to understand the trade-offs involved in selecting the values of C_F and R_F. If the value of C_F is high, it provides better attenuation against the kickback noise when the sampling switch closes. However, C_F cannot be made arbitrarily high because it degrades the phase margin of the driving amplifier, thus making it unstable. The series resistor R_F acts as an isolation resistor, which helps to stabilize the driving amplifier. A higher value of R_F is helpful from the amplifier stability perspective, but degrades AC performance and must be balanced with the amplifier stability to ensure that the distortion does not exceed the required specifications. The distortion happens due to the nonlinear input impedance of the ADC and it increases with source impedance, input signal frequency, and amplitude.

The maximum value of R_F depends upon the fact that by the end of the acquisition time (t_{ACQ}), the sampling capacitor (C_{SH}) must be charged to an acceptable level of the measured input voltage (V_{IN}). That means the signal must settle within 0.5 LSB at the input of the ADC for the worst-case full-scale change at the end of acquisition time as shown in 图 15. The value of the external filter resistance required is given by 公式 6:

$$R_F \times \left(C_F + C_{SH}\right) \leq \frac{t_{ACQ}}{k} \quad (6)$$

Where k is number of time constants as defined in 公式 7.

$$k = \ln\left|\frac{\left(V_{IN} - V_{CSH0}\right)}{\left(1 + \frac{C_F}{C_{SH}}\right) \times V_{FSR}} \times 2^{(N+1)}\right| \quad (7)$$

For this TI Design, the values of the parameters used in 公式 6 and 公式 7 are:

- t_{ACQ} = 95 ns
- C_F = 330 pF
- C_{SH} = 16 pF
- V_{IN} = 3.3 V
- V_{CSH0} = 0 V
- V_{FSR} = 3.3 V
- N = 14

After putting these values in 公式 6 and 公式 7, The maximum value of filter resistance (R_F) should be 37 Ω.

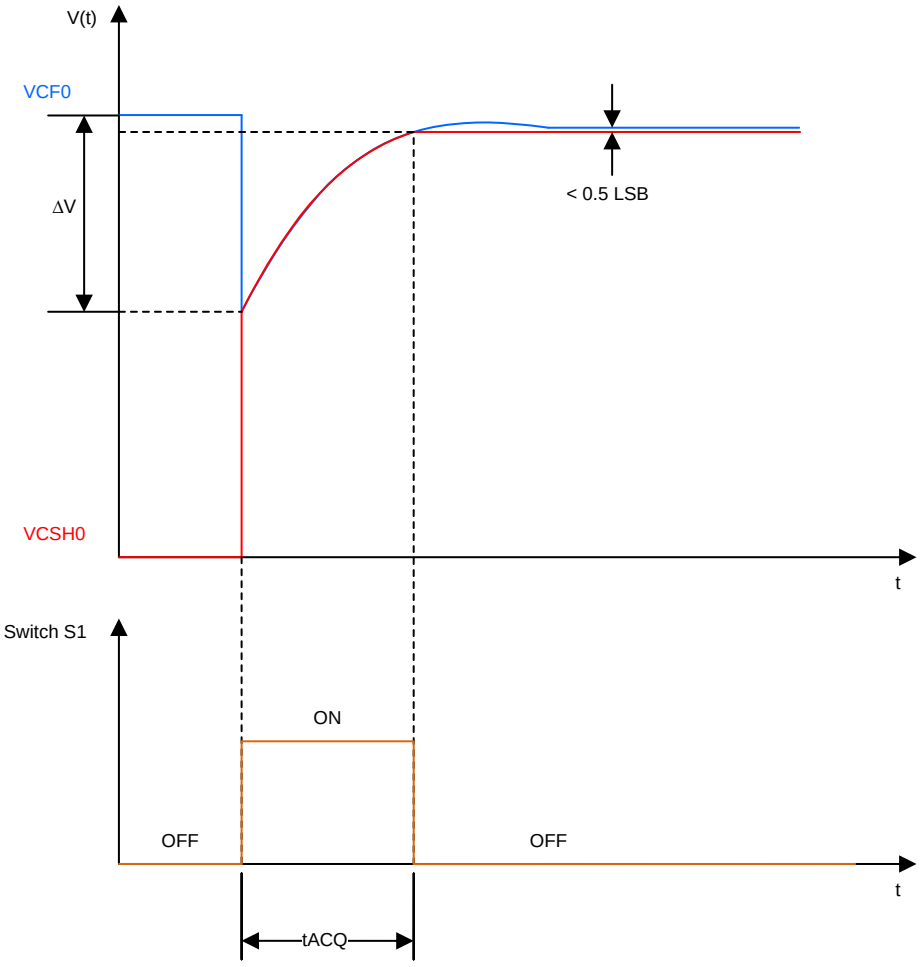

图 15. Voltage Waveform Across External Filter and Internal Sampling Capacitors at Start and End of ACQ State

The minimum value for R_F is dependent on the output impedance of the amplifier based on stability considerations. If the open-loop output impedance of the driving amplifier is equal to R_O, its stability can be analyzed by evaluating the effect of R_F and C_F on the open-loop response of the amplifier. The combination of R_O, R_F and C_F introduces one pole, f_{PX} (公式 7) and one zero, f_{ZX} in the open-loop response of the amplifier. The frequency of the additional pole and zero can be calculated from 公式 8 and 公式 9.

$$f_{PX} = \frac{1}{2\pi (R_O + R_F) \times C_F} \tag{8}$$

$$f_{ZX} = \frac{1}{2\pi \times R_F \times C_F} \tag{9}$$

To ensure that the phase change from the zero negates the phase change that the pole initiates, the frequency distance between the pole and zero must be less than or equal to one decade as given by 公式 10.

$$f_{ZX} \leq 10\, f_{PX} \tag{10}$$

Using 公式 8, 公式 9, and 公式 10, the minimum value for R_F can be derived as given in 公式 11.

$$R_F \geq \frac{R_O}{9} \tag{11}$$

The nominal value of R_O is derived from the closed-loop output impedance versus frequency plot shown in the OPA836 datasheet. From 公式 12, the magnitude of the operational amplifier's closed-loop output impedance (R_{OUT}) is a function of the operational amplifier's open-loop output impedance (R_O) and loop gain (Aβ):

$$R_O = R_{OUT}(f) \times (1 + A\beta(f)) \tag{12}$$

At f = UGBW, A = 1 and 1/β = 1, so loop gain Aβ = 1. As a result:

$$R_O = R_{OUT}(f = \text{UGBW} = 205\ \text{MHz}) \times (1 + 1) = 100\ \Omega \times 2 = 200\ \Omega \tag{13}$$

From 公式 11 and 公式 13, the constraint on R_F becomes 22.22 Ω ≤ R_F ≤ 37 Ω, and a standard value of R_F = 33 Ω can be used.

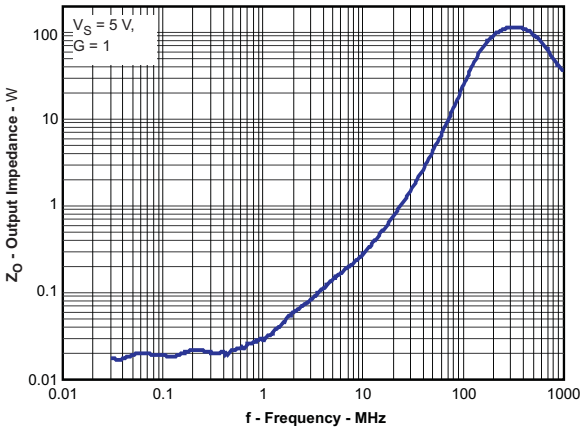

图 16. OPA836 Closed-Loop Output Impedance versus Frequency

2.3.3.2 Selecting Driver Amplifier

Consider the following aspects when selecting a suitable amplifier to drive the ADC:

- Bandwidth of the amplifier
- Settling time
- Amplifier noise
- Distortion

For multiplexed applications (for example, pixel-by-pixel reading in imaging applications), the large signal bandwidth may be more important due to the large voltage swings. The driving operational amplifier for such applications must have a high slew rate and bandwidth along with low noise and distortion. The input of the driver amplifier may see a maximum step of 3.3 V because it is possible to encounter a full-scale change between adjacent pixels.

In the interest of stability, the effects of f_{ZX} must occur at a frequency lower than the unity gain bandwidth of the amplifier (f_U). In order to account for the fabrication process variations over different production lots associated with the amplifier's performance and temperature variations, a good practice is to choose f_{ZX} such that the unity gain bandwidth of the amplifier (f_U) is at least four times the frequency of the zero (f_{ZX}).

$$f_U \geq 4\, f_{ZX} = \frac{4}{2\pi R_F C_F} = \frac{4}{2\pi \times 33\ \Omega \times 330\ pF} = 58.5\ MHz \tag{14}$$

With three ADCs in system and each ADC working at full throughput of 2.5 MSPS in order to achieve 7.5 MSPS, the two consecutive samples are 133.33 ns apart. Assuming that the pixels are switched immediately after taking the sample, the output of the amplifier must already be settled to a 14-bit accuracy even before the sampling switch R_{S1} is opened for the next 95 ns. Therefore, the selected amplifier has only 38.33 ns to settle to an acceptable level. The OPA836 has been selected for this TI Design for its 205-MHz GBWP, 560-V/µs slew rate, 4.6-nV/√Hz noise, and 0.01% settling time of 40 ns (rise) and 45 ns (fall).

2.3.3.2.1 Calculating 14-bit Settling Time for OPA836

The settling time mainly consists of dead time, slew time, recovery time, and linear settling time as shown in 图 17.

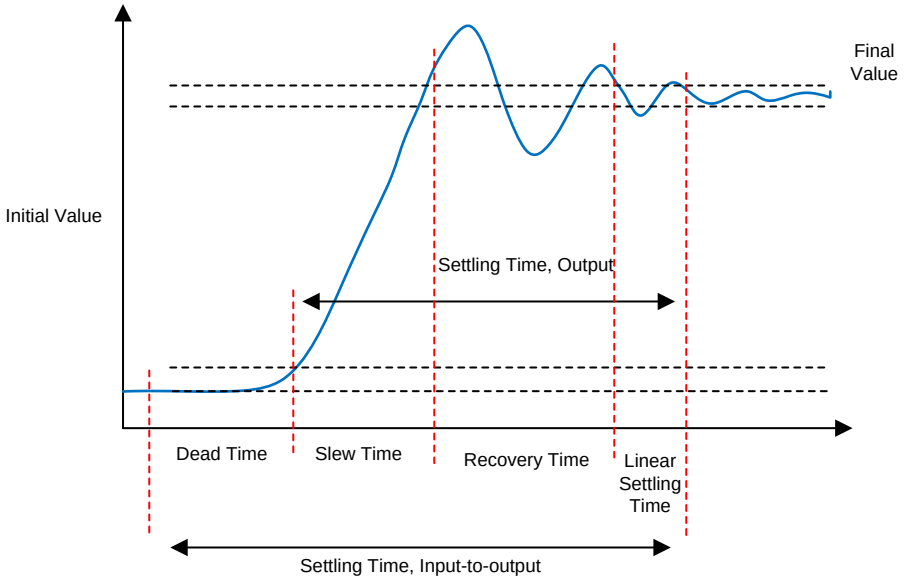

图 **17. Settling Time**

A close approximation of the amplifier's settling time for the required system accuracy can be given using 公式 15:

$$t_{SETTLING} = t_{SLEW} + \frac{k}{2\pi \times LSBW} \quad (15)$$

Where:

- $t_{SETTLING}$ is the settling time of the amplifier
- t_{SLEW} is the slew time of the amplifier
- k is number of time constants required by the amplifier for N-bit settling as defined by 公式 16
- LSBW is the large signal bandwidth of the amplifier

$$k = (N+1)\ln 2 = (14+1) \times \ln 2 = 10.4 \quad (16)$$

For a step input (VSTEP) of 3.3 V, the slew time for the OPA836 with a slew rate (SR) of 560 V/µs can be calculated using 公式 17:

$$t_{SLEW} = \frac{VSTEP}{SR} = \frac{3.3\ V}{560\ \frac{V}{\mu s}} = 5.9\ ns \quad (17)$$

The OPA836 op amp has a large signal bandwidth (LSBW) of 87 MHz. Calculate the settling time of the amplifier ($t_{SETTLING}$) using the results from 公式 15, 公式 16, and 公式 17:

$$t_{SETTLING} = 5.9\ ns + \frac{10.4}{2\pi \times 87\ MHz} = 25\ ns \quad (18)$$

公式 18 shows that the OPA836 settles to a 14-bit accuracy in approximately 25 ns, which is lower than the allowed 38.33 ns.

To minimize the distortion, it is important that the ADC and driver amplifier do not introduce any non-linearity into the system. To achieve the least possible distortion, the amplifier needs to have a distortion that is negligible in comparison to the ADC. The THD of the amplifier must be 10 dB smaller than the THD of the ADC at the frequency of interest as given by 公式 19 to ensure overall system distortion does not degrade by more than –0.5 dB. The THD of the ADS7056 is –85 dB at a 2-kHz input frequency.

$$THD_{AMP} < THD_{ADC} - 10\ dB = -95\ dB \quad (19)$$

The THD of the selected amplifier OPA836 is much lesser than –95 dB.

2.3.3.2.2 Noise Analysis of System

Achieving good noise performance requires the noise contribution of the driver amplifier to be much less than that of the ADC to have minimal impact on the overall SNR. More specifically, this requirement may be restated by 公式 20:

$$V_{n\,rms,\,AMP} \le \frac{V_{n\,rms,\,ADC}}{3} \tag{20}$$

The RC filter bandwidth is important to determine the maximum amount of noise from the amplifier entering the ADC. First, calculate the referred-to-output (RTO) noise of the amplifier over the RC bandwidth using 公式 21:

$$V_{n\,rms,\,AMP} = NG\, e_{n,\,AMP} \sqrt{\frac{\pi}{2} BW_F} \tag{21}$$

Where:

- $e_{n,\ AMP}$ is input noise spectral density in nV/√Hz
- NG is the noise gain of amplifier
- BW_F is the bandwidth of the external RC filter in Hz

A high-performance, 14-bit, 2.5-MSPS SAR ADC has a typical SNR specification of 74.9 dB. It is critical that this SNR performance is maintained when noise from the external front-end circuit is added. As a result, it is important to analyze the noise and SNR of the system.

For the ADC with an input full-scale range of V_{FSR}, calculate the input referred noise from the SNR of the ADC specified in the datasheet by using 公式 22:

$$V_{n\,rms,\,ADC} = \frac{V_{FSR}}{2\sqrt{2}} \times 10^{-\frac{SNR(dB)}{20}} \tag{22}$$

Now, $e_{n,\ AMP}$ can be calculated using the results from 公式 20, 公式 21, and 公式 22:

$$e_{n,\,AMP} \le \frac{V_{FSR}}{3 \times 2\sqrt{2}} \times 10^{-\frac{SNR(dB)}{20}} \times \sqrt{\frac{2}{\pi \times BW_F}} = \frac{3.3\ V}{3 \times 2\sqrt{2}} \times 10^{-\frac{74.9}{20}} \times \sqrt{\frac{2}{\pi \times 14.625\ MHz}} \tag{23}$$

Thus, the amplifier must have a noise density less than or equal to 14.65 nV/√Hz. The OPA836 meets this criterion with 4.6 nV/√Hz.

2.3.3.2.3 Selecting Voltage Reference

The precision of a data acquisition system is only as good as its reference source which can directly impact most of the performance parameters of the ADC. The reference source is comprised of a low drift reference voltage and low impedance buffer. DC accuracy, stability, and drive capability are the main design criteria for the reference system.

In this TI Design, the external voltage reference used to drive the all three ADS7056 SAR ADCs is the REF2033. The REF2033 reference is a low-drift, low-power TI solution with dual outputs, V_{REF} and V_{BIAS} (= V_{REF}/2). If needed, the second output (V_{BIAS}) can be used by the input driver amplifier to scale its output. The REF2033 offers excellent temperature drift (8 ppm/°C) and an initial accuracy of 0.05% on both V_{REF} and V_{BIAS} outputs while operating at a quiescent current less than 430 µA. In addition, the V_{REF} and V_{BIAS} outputs track each other with a precision of 6 ppm/°C across the temperature range of –40°C to 85°C.

The reference design hardware also has a provision to populate the REF6030. This reference comes with an integrated low-output impedance buffer and filter that enable users to directly drive the REF pin of the precision SAR and delta-sigma ADCs. The 3-dB frequency of the filter can be varied by connecting a capacitor of the user's requirement to the FILT pin. The REF6030 also offers excellent drift performance at 5 ppm/°C. With very low noise (total noise is 5 μV_{RMS} with a 47-µF capacitor) and distortion, the device is perfect to use in applications where the dynamic performance of the ADC is the key requirement.

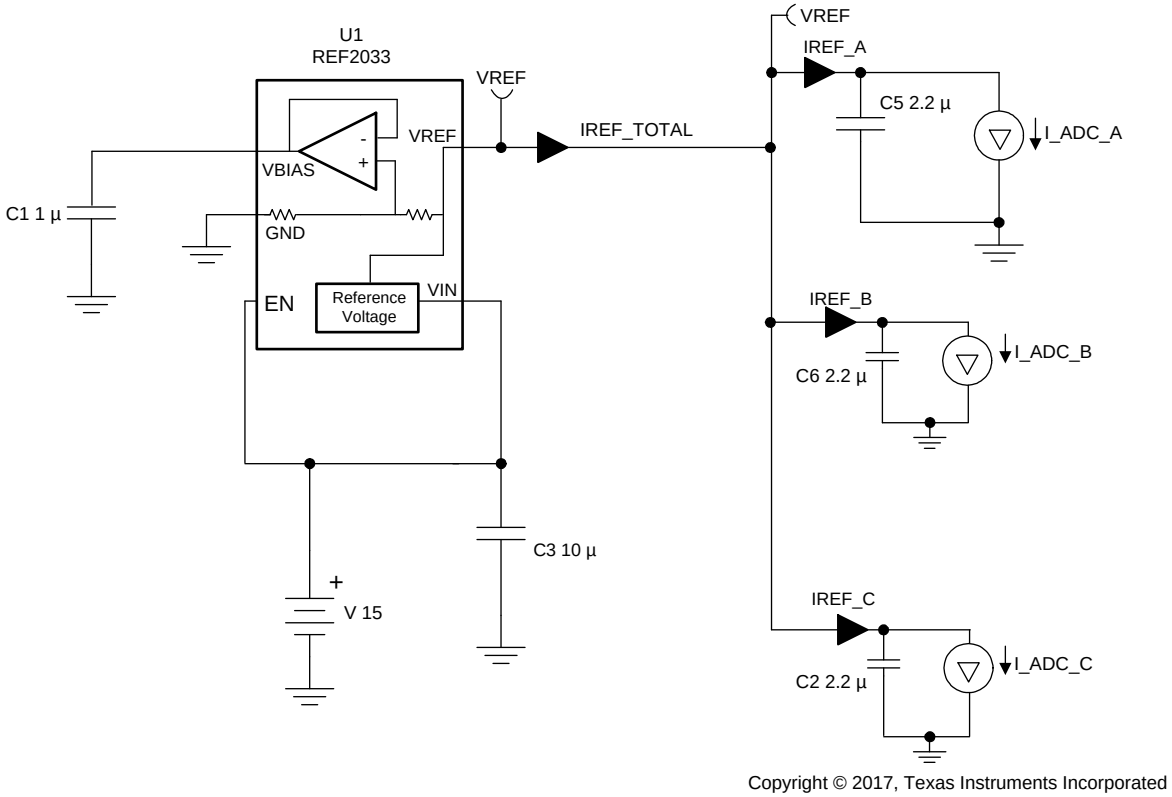

图 18. TINA-TI Schematic for REF2033 Settling

The TINA-TI schematic shown in 图 18 is used to check the settling of the reference, which is used to power the ADC. To maintain the overall system performance, the voltage at the REF2033 output pin must settle to less than one LSB of the ADS7056 ADC. To simulate reference settling performance, the REF2033 is loaded with equivalent current sources modeled for the AVDD current of the ADS7056. From the simulation results shown in 图 19, the ADS7056 consumes ≈ 1-mA current at 2.5 MSPS of throughput from the AVDD supply, and the switching current consumed by each ADC is provided by the decoupling capacitor (2.2 µF) on the AVDD pin of the ADC. The reference sees a DC load current of 3.5 mA and settles to VREF-1/2 LSB in less than 1 ms and remains stable while all the ADCs are converting at a 2.5-MSPS throughput.

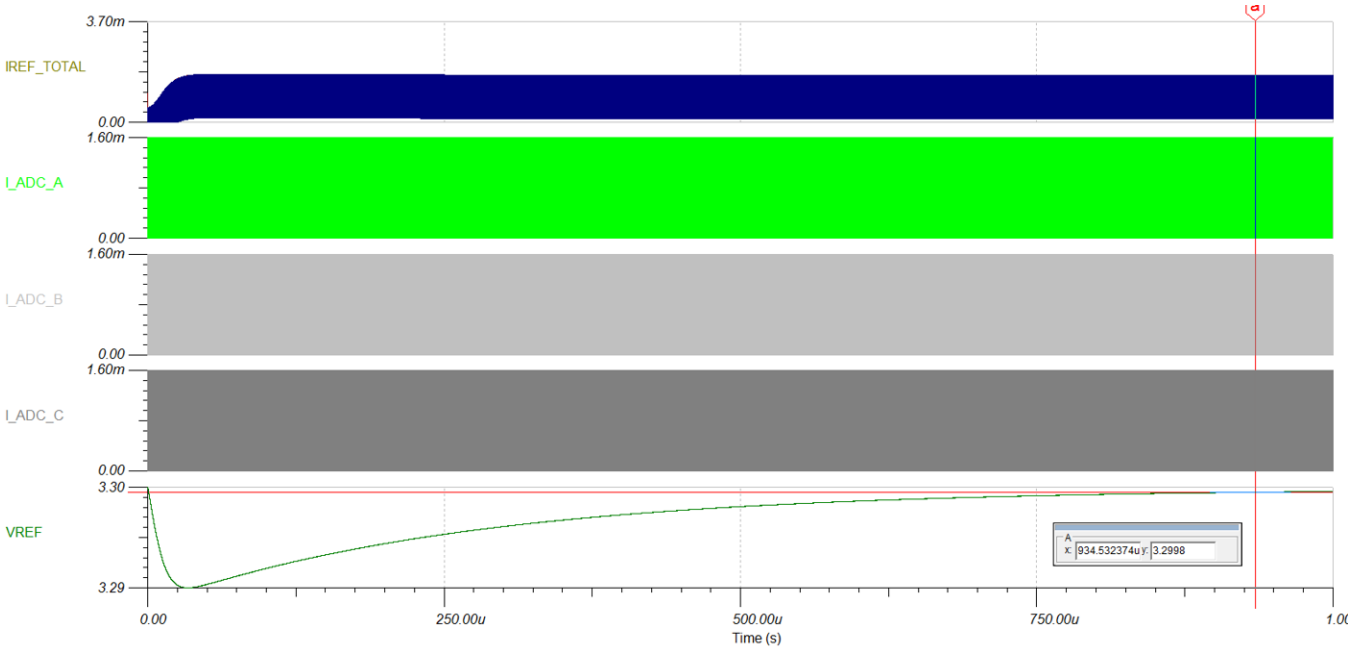

图 19. TINA-TI Simulation Result for REF2033 Settling

3 Hardware, Testing Requirements, and Test Results

3.1 Required Hardware

图 20 shows the hardware of this TI Design. The printed circuit board (PCB) size comes in at a 54.61-mm×40.64-mm rectangular form factor and comes with 0.5-inch nylon standoffs to ensure ease of use while performing lab measurements. However, the main analog front-end circuit that includes the driver amplifier, voltage reference, three SAR ADCs, LDO, voltage level translator, and other discrete occupy only 22.33 mm × 13.21 mm. All the integrated circuits (ICs) are located only on top side of the PCB.

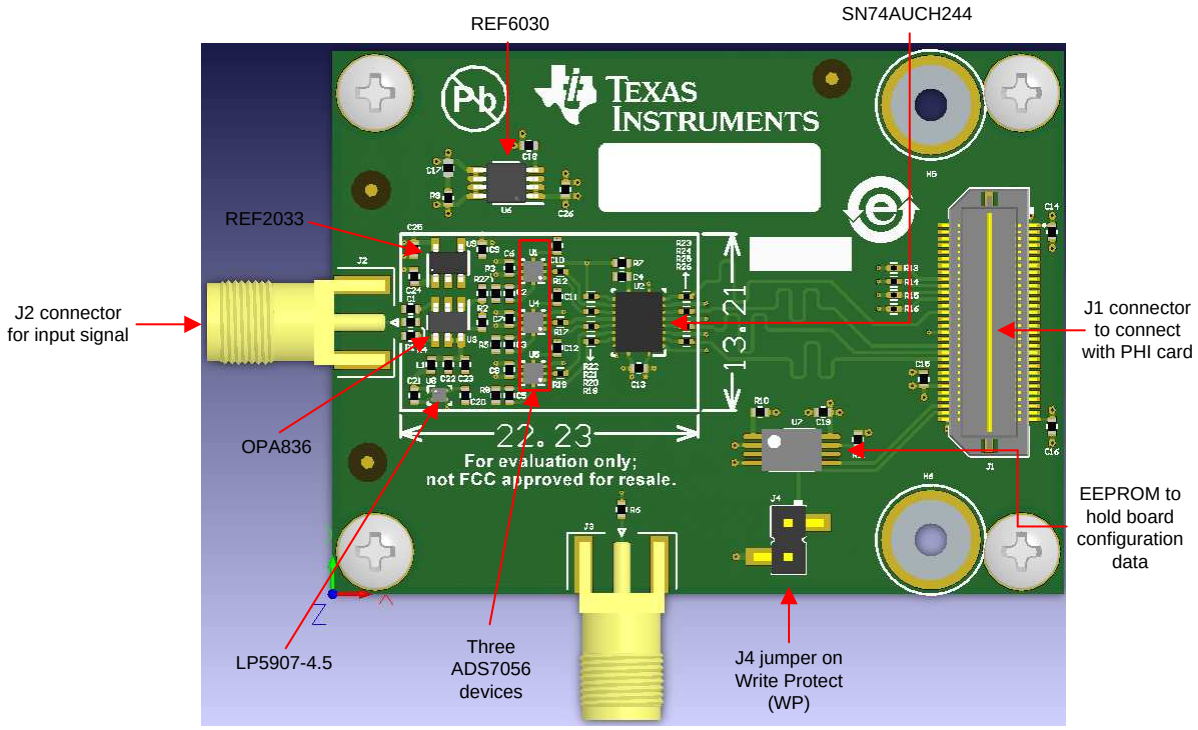

图 20. TIDA-01355 Hardware

3.2 Testing and Results

The following subsections show the results of testing and characterization.

注: Unless otherwise noted, the test data in the following sections were measured with the system at room temperature.

注: All of the measurements in this section were measured with calibrated lab equipment.

3.2.1 DC Histogram

A DC histogram is a well-known technique used for measuring the referred-to-input (RTI) RMS noise of the ADC signal chain. The DC histogram is referred to as a grounded input histogram if the input is connected to ground (0 V). An ideal ADC (noiseless) produces codes that fall only in one bin; however, a real ADC (noisy) produces codes that also fall outside the main bin for a given DC input due to the presence of noise. For histogram testing, the input signal was connected to the circuit ground (0 V) at the J2 connector on the PCB. A histogram was plotted by collecting a large number of samples (more than 2 million output codes) and observing the peak-to-peak code spread at the output of ADC to determine the input RMS noise. Because the noise is random in nature, it would have Gaussian distribution. The cumulative effect of noise coupling to the ADC output from sources such as the input drive circuits, the reference drive circuit, the ADC power supply, and the ADC itself is reflected in the standard deviation of the ADC output code histogram. Therefore, standard deviation (σ) of the histogram corresponds to the RMS noise in terms of the number of LSBs that can be multiplied by the size of 1 LSB to convert it in to input RMS noise voltage.

图 21 and 图 22 shows the grounded input histogram for the interleaved system before and after the internal offset calibration, respectively. 图 21 clearly shows the offset mismatch among the three time-interleaved ADS7056 SAR ADCs where the peak-to-peak code spread is around 88 codes. The offset mismatch can be minimized to a great extent by initiating internal offset calibration cycles to each ADC independently either once after power-up or periodically during the run-time depending upon specific application requirements. As a result, the peak-to-peak code spread is around 9 codes as shown in 图 22.

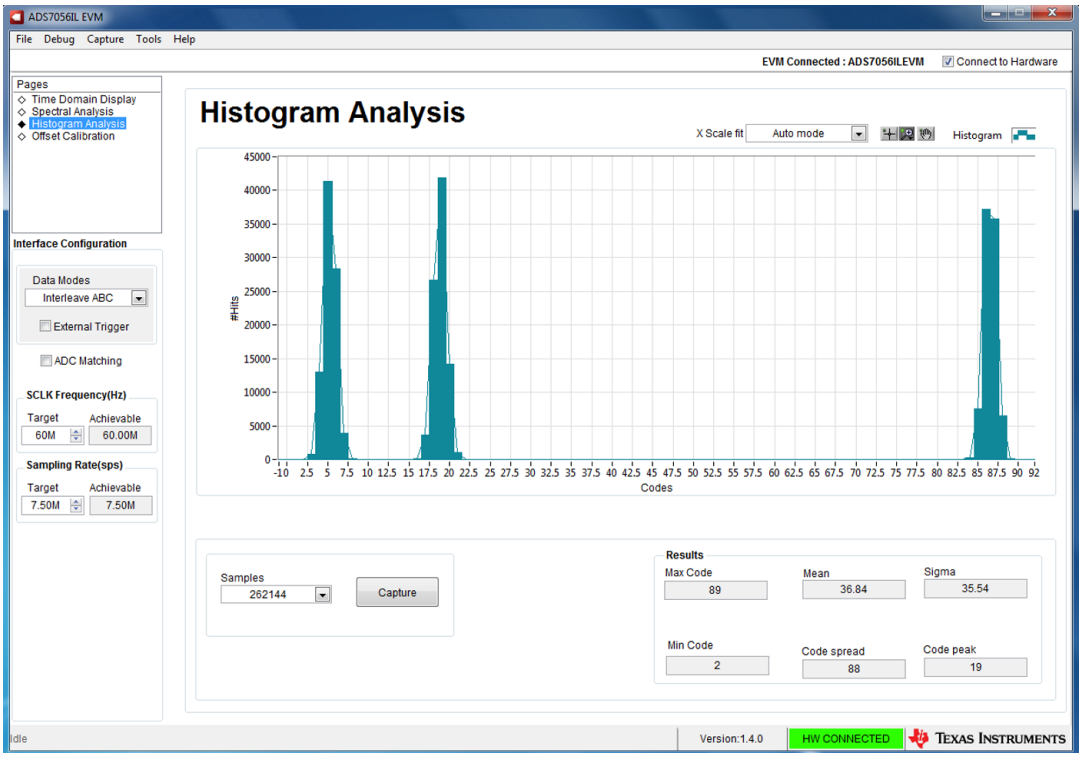

图 21. Grounded Input Histogram Before Internal Offset Calibration

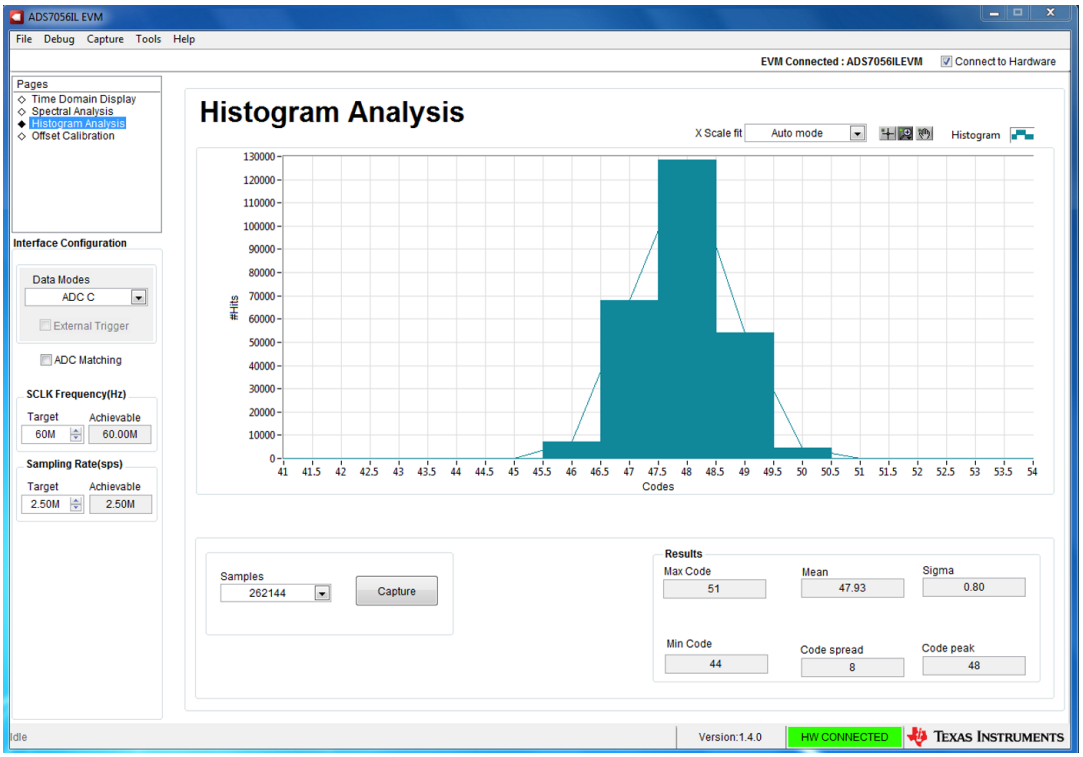

图 22. Grounded Input Histogram After Internal Offset Calibration

From 图 22, the standard deviation (σ) of the histogram = Input RMS noise (in LSBs) = 0.89 LSB. Therefore, multiplying the standard deviation (σ) with a size of 1 LSB gives the input RMS noise voltage as given by 公式 24:

$$\text{Input RMS Noise Voltage} = \sigma \times \frac{V_{REF}}{2^N} = 0.89 \times \frac{3.3\ V}{2^{14}} = 179\mu V \quad (24)$$

3.2.2 Spectrum Analysis

The spectral analysis tool is intended to evaluate the dynamic performance (SNR, THD, SFDR, SINAD, and ENOB) of any ADC through an FFT analysis of a single-tone sinusoidal signal using the 7-term Blackman-Harris window setting. To evaluate dynamic performance, the external differential source must have better specifications than the ADC itself to ensure that the measured system performance is not limited by the performance of the signal source. Therefore, the external reference source must have very low noise and low distortion and meet the source requirements mentioned in 表 2.

表 2. External Signal Source Requirements to Evaluate TIDA-01355

SPECIFICATION DESCRIPTION	SPECIFICATION VALUE
Signal frequency	2 kHz
External source type	Unbalanced
Maximum noise	Better than 10 μV_{RMS}
SNR	Better than 100 dB
THD	Better than –130 dB

Finally, the FFT tool includes windowing options that are required to mitigate the effects of non-coherent sampling (this discussion is beyond the scope of this document). The 7-Term Blackman Harris window is the default option.

The expected ADC input is a sinusoidal signal of peak-to-peak amplitude close to the full-scale input range (FSR) of the ADC. The RMS power of the input signal normalized to FSR is shown in the Signal Power (dBFS) field and is about –0.5 dBFS (or about 95% × FSR) to avoid the input clipping.

A 2-kHz sinusoidal signal was applied to the TI Design board at connector J2. For spectrum analysis at a maximum throughput of 7.5 MSPS, the numbers of samples were set to 262144. 图 23 and 图 24 shows the spectral analysis before and after the internal offset calibration.

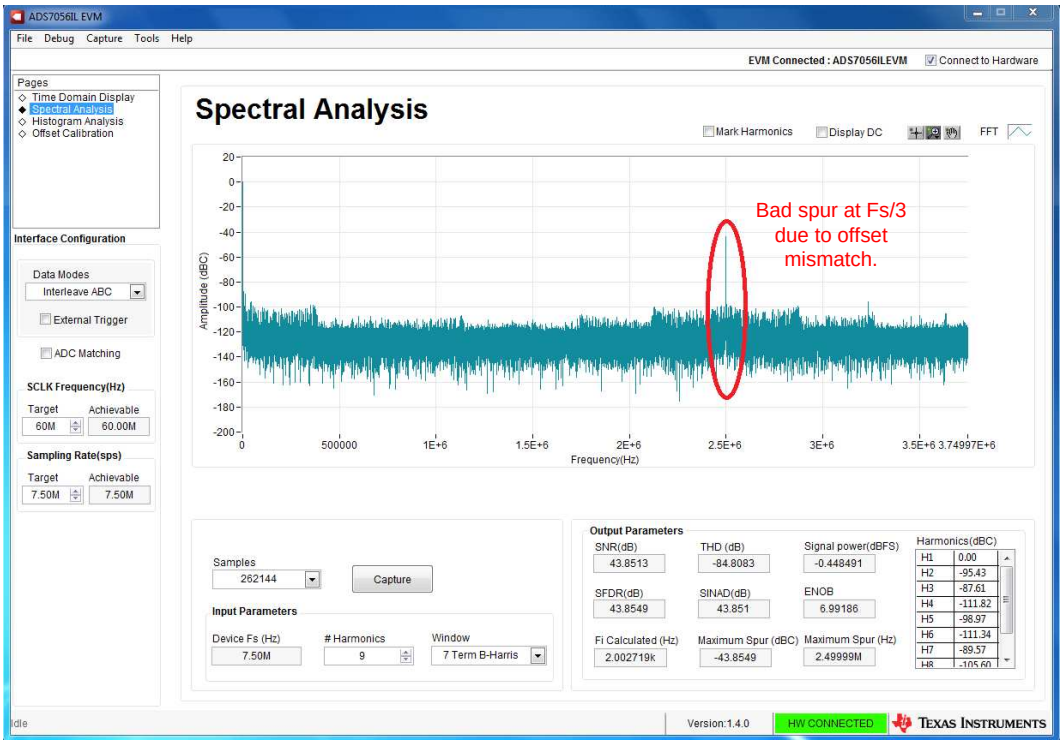

图 23. Spectral Analysis Before Internal Offset Calibration

图 24. Spectral Analysis After Internal Offset Calibration

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01355.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01355.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01355.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01355.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01355.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01355.

5 Software Files

To download the software files, see the design files at TIDA-01355.

6 Related Documentation

1. Texas Instruments, *ADS7056 Ultra-Low Power, Ultra-Small Size, 14-Bit, High-Speed SAR ADC*, ADS7056 Datasheet (SBAS769)
2. Texas Instruments, *OPAx836 Very-Low-Power, Rail-to-Rail Out, Negative Rail In, Voltage-Feedback Operational Amplifiers*, OPA836 Datasheet (SLOS712)
3. Texas Instruments, *REF20xx Low-Drift, Low-Power, Dual-Output, VREF and VREF / 2 Voltage References*, REF2033 Datasheet (SBOS600)
4. Texas Instruments, *REF60xx High-Precision Voltage Reference With Integrated ADC Drive Buffer*, REF6030 Datasheet (SBOS708)
5. Texas Instruments, *LP5907 250-mA Ultra-Low-Noise, Low-IQ LDO*, LP5907 Datasheet (SNVS798)
6. Texas Instruments, *SN74AUCH244 Octal Buffer/Driver with 3-STATE Outputs*, SN74AUCH244 Datasheet (SCES433)
7. N. Kurosawa, H. Kobayashi, K. Maruyama, H. Sugawara, K. Kobayashi, *Explicit Analysis of Channel Mismatch Effects in Time-interleaved ADC Systems*, IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications (Volume: 48, Issue: 3, Mar 2001)
8. Christian Vogel, *The Impact of Combined Channel Mismatch Effects in Time-Interleaved ADCs*, IEEE Transactions on Instrumentation and Measurement (Volume: 54, Issue: 1, Feb. 2005)
9. Behzad Razavi, *Design Considerations for Interleaved ADCs*, IEEE Journal of Solid-State Circuits (Volume: 48, Issue: 8, Aug. 2013)
10. Peter Händel, *Properties of the IEEE-STD-1057 Four-Parameter Sine Wave Fit Algorithm*, IEEE Transactions on Instrumentation and Measurement (Volume: 49, Number: 6, Dec. 2000)
11. Texas Instruments, *Low-Cost, Low-Power, Small Size,14-bit AFE: Interleaved ADCs Scalable up to*

7.5 MSPS Sampling With 73-dB SNR, Application Note (SBAA231)

6.1 商标

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