Errata

IWRL1432 Device Silicon Errata

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ADVANCE INFORMATION

1 Introduction

This document describes the known exceptions to the functional and performance specifications to TI CMOS Radar Devices (IWRL1432)

2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of Radar / mmWave sensor devices. Each of the Radar devices has one of the two prefixes: XIx or IWRLx (for example: XI1432BGABL). These prefixes represent evolutionary stages of product development from engineering prototypes (XI) through fully qualified production devices IWRLx.

Device development evolutionary flow:

XI — Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

IWRL — Production version of the silicon die that is fully qualified.

XIx devices are shipped with the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Texas Instruments recommends that these devices not to be used in any production system as their expected end –use failure rate is still undefined.

3 Device Markings

Figure 3-1 shows an example of the IWRL1432 Radar Device's package symbolization.

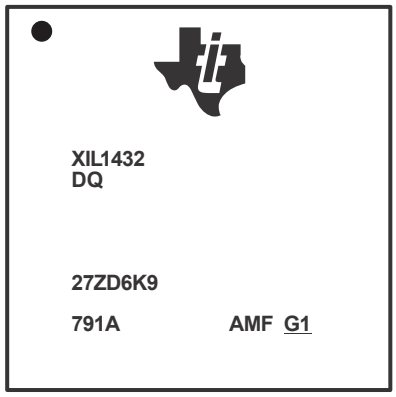

Figure 3-1. Example of Device Part Markings

This identifying number contains the following information:

- **Line 1:** TI Logo
- **Line 1:** Device Number
- **Line 2:** Safety Level and Security Grade
  - D = Deep Sleep Enabled
  - Q = Non-Functional Safety
- **Line 3:** Lot Trace Code
  - 27 = Year/Month Code
  - Z = Assembly Site Code
  - D6M = Assembly Lot
  - 9= Primary Site Code
- **Line 4:**
  - 791A = Device Identifier
  - AMF = Package Identifier
  - G1 = "Green" Package Build (must be underlined)

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4 Advisory to Silicon Variant / Revision Map

Table 4-1. Advisory to Silicon Variant / Revision Map

Advisory Number	Advisory Title	IWRL1432 ES1.1
Analog / Millimeter Wave		
ANA #51	Continuous Wave Streaming CZ mode: Sudden jump in RX output codes every 20.97152 msec	x
ANA #52	Slicer LDO Test LOAD (TLOAD) not disabled after startup	x
Digital Subsystem		
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DIG #2	UART: UARTA cannot be used to wake up the sequencer from Deep Sleep Low Power Mode	x
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DIG #6	CRC: CRC 8-bit data width and CRC8-SAE-J1850 and CRC8-H2F possible use in CAN module is not supported	x
DIG #7	APPSS Cortex-M4 doesn't get the correct error response when cluster 3 retention memories are accessed in low-power deep-sleep powered down state	x
DIG #8	Shared RAM clock gating default values	x
DIG #9	TOP_IO_MUX register space not accessible from RS232 for debug purposes	x
DIG #10	Incorrect behavior of chirp stop in Infinite chirp mode	x

5 Known Design Exceptions to Functional Specifications

ANA #51 ***Continuous Wave Streaming CZ mode: Sudden jump in RX output codes every 20.97152 msec***

Revision(s) Affected IWRL1432 ES1.1

Details

On Continuous Wave Streaming CZ mode, the Rx data shows a sudden jump in output codes every 20.97152 milliseconds.

This is not an issue in the Radar Functional mode when chirps are used. However, this issue will be seen when testing Rx chain in lab using continuous stream mode.

Workaround

In order to use Continuous stream (CW) mode for testing, it is recommended to start data capturing from the first sample itself to make sure the glitch occurs at deterministic samples. Please follow the below sequence to achieve this:

- Configure the RDIF (Radar Data Interface)
- Arm the DCA1000 (Data capture card)
- Enable the continuous stream mode.

The glitch will not be seen with this sequence. For example, if the user analyzes first 20ms of data or between 21 and 41ms.

ANA #52	*Slicer LDO Test LOAD (TLOAD) not disabled after startup*
Revisions Affected	IWRL1432 ES1.1
Details	By default, the slicer LDO TLOAD is enabled during startup for stability purposes. After the oscillator is enabled, the current loading should be disabled automatically to reduce power and extend reliability. Since presently the loading is not turned OFF automatically, higher than expected current is observed (~8mA).
Workaround	It is recommended to disable the load bit explicitly by setting the following field to save unnecessary power burnout : TOP_PRCM: CLK_CTRL_REG1_LDO_CLKTOP = 0x1

DIG #1 ***ePWM: Glitch during Chopper mode of operation***

Revision(s) Affected IWRL1432 ES1.1

Details During chopper mode operation, a glitch may be observed on the ePWMA and ePWMB output signals from the ePWM module.

Workaround If the use case is impacted by a glitch, it is recommended to disable the PWM chopper control function by setting the LPRADAR:APP_PWM:PCCTL:CHPEN register bit to 0.

The below table shows the Register Address for above workaround.

Bits	Name	Address
0	LPRADAR:APP_PWM:PCCTL:CHPEN	0X57F7 FC3C

DIG #2	***UART: UARTA cannot be used to wake up the sequencer from Deep Sleep Low Power Mode***
Revision(s) Affected	IWRL1432 ES1.1
Details	Universal Asynchronous Receiver-Transmitter A (UART A) cannot be used to wake up from Deep-Sleep mode of the processor. Currently UART B interrupts are connected to Wake-up Interrupt Controller lines.
Workaround	It is recommended to use other wake-up sources (Controller Area Network - Flexible Data-rate (CAN-FD)/ UARTB/ Serial Peripheral Interface(SPI))

DIG #3 ***UART: Limited UART baud rates***

Revision(s) Affected IWRL1432 ES1.1

Details

Due to a design limitation (related to the clocking scheme), UART doesn't support standard baud rates above 115200 bits per second. Higher baud rates up to 1.25Mbps can be supported but they are non-standard.

Applications requiring UART cannot use standard baud rates above 115200 bits per second

Standard Baud Rates supported :

XTAL (MHz)	40	
Ideal Baud rate (bps)	Actual Baud	Error %
115200	113636.36	1.36
76800	75757.58	1.36

Non- Standard baud rates supported:

XTAL (MHz)	**40**
Maximum baud (bps)	1250K
	833.33k
	625K
	500K
	416.66k
	357.14
	312.5k

Workaround

It is recommended to use the following workarounds based on application needs:

- Use of non-standard baud rates can provide up to 1.25Mbps throughput, if external MCU can support the same non-standard baud rates.
- Use SPI instead, if use-case needs higher throughput.

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DIG #4	***RS232: Auto Baud Rate feature doesn't support trimmed RCOSC variation***
Revision(s) Affected	IWRL1432 ES1.1
Details	Once RCOSC is trimmed, the expected clock frequency and the variation observed in frequency (tolerance on RC clock) do not support the required Auto Baud rate setting for RS232. Currently Auto Baud is disabled by default for 14xx ES1.1

DIG #6	***CRC: CRC 8-bit data width and CRC8-SAE-J1850 and CRC8-H2F possible use in CAN module is not supported***
Revision(s) Affected	IWRL1432 ES1.1
Details	CRC types CRC8-SAE-J1850 and CRC8-H2F are not supported for 8-bit data width. Minimum data width supported is 16-bit.
Workaround	It is recommended to not use the above mentioned unsupported polynomials.

DIG #7	***APPSS Cortex-M4 doesn't get the correct error response when cluster 3 retention memories are accessed in low-power deep-sleep powered down state***
Revision(s) Affected	IWRL1432ES1.1
Details	The logic to generate error when Cortex-M4F tries to access cluster 3 memories in powered down state is incorrect due to which Cortex-M4F doesn't get the correct error response.
Workaround	Software shouldn't try to access cluster 3 retention memories during low-power deep-sleep powered down state

DIG #8 ***Shared RAM clock gating default values***

Revision(s) Affected IWRL1432ES1.1

Details

Possibility of Shared RAM data corruption while exiting from deep sleep mode when clock gating registers are not reprogrammed.

The reset value for Front End Controller Sub System (FECSS), Application Sub System (APPSS) and Hardware Accelerator Sub System (HWASS) shared memory clock gate control is 1 . The clock ICG controls are coming from the following registers.

Bits	Name	Address
0	LPRADAR:FEC_CTRL:FECSS_SHARED_MEM_CLK_GATE : FECSS_SHARED_MEM_CLK_GATE_HWA_ENABLE	0x5200002C
0	LPRADAR:APP_CTRL:APPSS_SHARED_MEM_CLK_GATE:APPSS_SHARED_MEM_CLK_GATE_MEM0_HWA_ENABLE	0x56060398
2	LPRADAR:APP_CTRL:APPSS_SHARED_MEM_CLK_GATE:APPSS_SHARED_MEM_CLK_GATE_MEM1_HWA_ENABLE	0x56060398

When APPSS tries to access shared memory bank 0 via VBUSM SCR while FECSS is accessing shared memory via AHB, wrong read values of zero from the shared RAM on the APPSS is observed .

If only one of the clock gates (either HWA or FEC/APP) is enabled based on the allocation, the data is read correctly. Since the clock gating controls are coming from control registers space, these values get reset again and hence needs to be re-programmed after every deep sleep exit.

Workaround

Program ICG controls of clock reaching to shared memory based on different shared memory configuration. The ICG control needs to be re-programmed after every deep sleep exit too.

Configuration	Software care-about
Memory is shared with M3	Disable the following ICG control :- LPRADAR:FEC_CTRL:FECSS_SHARED_MEM_CLK_GATE : FECSS_SHARED_MEM_CLK_GATE_HWA_ENABLE
First 128kb is shared with M4	Disable the following ICG control :- LPRADAR:APP_CTRL:APPSS_SHARED_MEM_CLK_GATE:APPSS_SHARED_MEM_CLK_GATE_MEM0_HWA_ENABLE
256kb is shared with M4	Disable the following ICG controls :- • LPRADAR:APP_CTRL:APPSS_SHARED_MEM_CLK_GATE:APPSS_SHARED_MEM_CLK_GATE_MEM0_HWA_ENABLE • LPRADAR:APP_CTRL:APPSS_SHARED_MEM_CLK_GATE:APPSS_SHARED_MEM_CLK_GATE_MEM1_HWA_ENABLE

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DIG #9 ***TOP_IO_MUX register space not accessible from RS232 for debug purposes***

Revision(s) Affected IWRL1432ES1.1

Details RS232 is not able to write TOP_IO_MUX registers unless the space is programmed for user mode access.

Workaround It is recommended to use the following sequence:

1. From Processor or DAP : Unlock TOP_IO_MUX registers (by programming LPRADAR:TOP_IO_MUX:IOCFGKICK0 = 83E7 0B13h and LPRADAR:TOP_IO_MUX:IOCFGKICK1 = 95A4 F1E0h)
2. From Processor or DAP : Write to TOP_IO_MUX registers, LPRADAR:TOP_IO_MUX:USERMODEEN should be set to 0xADADADAD
3. Now TOP_IO_MUX registers can be accessed from RS232.

The below table shows the Register Addresses for above workaround.

Bits	Name	Address
0:31	LPRADAR:TOP_IO_MUX:IOCFGKICK0	0x5A000068
0:31	LPRADAR:TOP_IO_MUX:IOCFGKICK	0x5A00006C
0:31	LPRADAR:TOP_IO_MUX:USERMODEEN	0x5A000060

DIG #10	***Incorrect behavior of chirp stop in Infinite chirp mode***
Revision(s) Affected	IWRL1432ES1.1
Details	In situations with infinite chirp mode, issuing a *"Chirp Stop"* command when frames are not in progress results in an incorrect behavior for the subsequent frame. The next frame starts to transmit normally, but stops after transmitting only one chirp.
Workaround	It is recommended to check the active status of the current frame and only issue chirp stop command if it is active

6 Trademarks

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Revision History

DATE	REVISION	NOTES
July 2023	*	Initial Release

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