

# ADS7138-Q1

## Functional Safety FIT Rate, FMD and Pin FMA



### Table of Contents

1 Overview.....	2
2 Functional Safety Failure In Time (FIT) Rates.....	3
3 Failure Mode Distribution (FMD).....	4
4 Pin Failure Mode Analysis (Pin FMA).....	5

### Trademarks

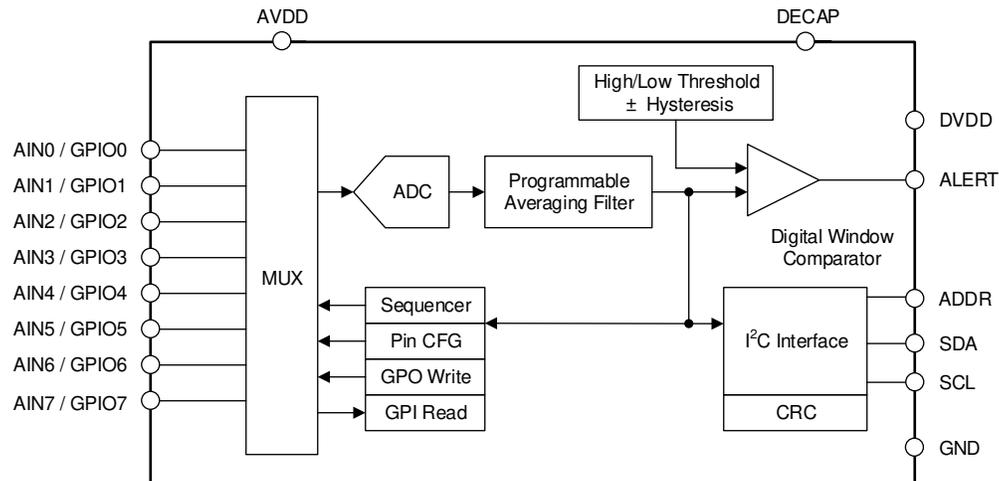
All trademarks are the property of their respective owners.

## 1 Overview

This document contains information for the ADS7138-Q1 (WQFN package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.



**Figure 1-1. Functional Block Diagram**

The ADS7138-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

## 2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for ADS7138-Q1 based on two different industry-wide used reliability standards:

- [Table 2-1](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-2](#) provides FIT rates based on the Siemens Norm SN 29500-2

**Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 <sup>9</sup> Hours)
Total component FIT rate	8
Die FIT rate	2
Package FIT rate	6

The failure rate and mission profile information in [Table 2-1](#) comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor control from table 11
- Power dissipation: 2 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

**Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2**

Table	Category	Reference FIT Rate	Reference Virtual T <sub>J</sub>
5	CMOS, BICMOS Digital, analog, or mixed	60 FIT	77°C

The reference FIT rate and reference virtual T<sub>J</sub> (junction temperature) in [Table 2-2](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

### 3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for ADS7138-Q1 in [Table 3-1](#) comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

**Table 3-1. Die Failure Modes and Distribution**

Die Failure Modes	Failure Mode Distribution (%)
Incorrect channel selected	20
Channel-channel short	15
ADC output code bit error	10
ADC gain error out of specification	10
ADC offset error out of specification	10
Communication error	10
Digital window comparator output fails to trip or false trip	10
Incorrect GPIOx pin configuration	5
Incorrect AINx/GPIOx pin operation (input/output stuck-at, floating, or incorrect logic level)	5
Incorrect programmable averaging filter output	5

## 4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the ADS7138-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

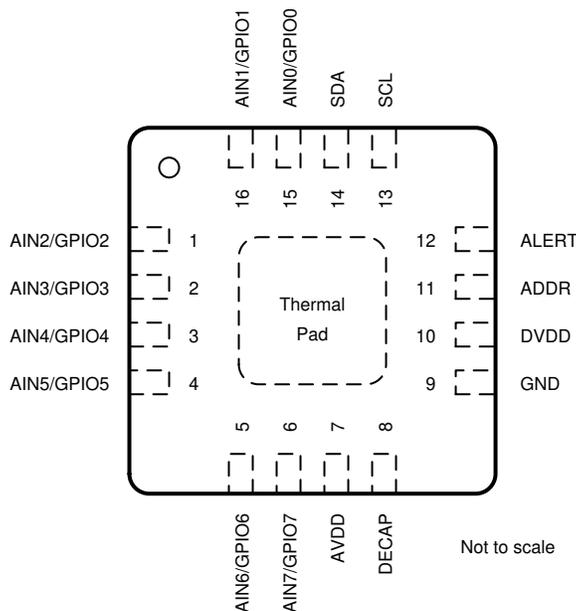
- Pin short-circuited to ground (see [Table 4-2](#))
- Pin open-circuited (see [Table 4-3](#))
- Pin short-circuited to an adjacent pin (see [Table 4-4](#))
- Pin short-circuited to supply (see [Table 4-5](#))

[Table 4-2](#) through [Table 4-5](#) also indicate how these pin conditions can affect the device as per the failure effects classification in [Table 4-1](#).

**Table 4-1. TI Classification of Failure Effects**

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

[Figure 4-1](#) shows the ADS7138-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the ADS7138-Q1 data sheet.



**Figure 4-1. Pin Diagram**

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- AVDD and DVDD use the same supply voltage.
- *Short-circuit to power* means short to AVDD = DVDD.
- RC filters are on every analog input, AINx. Series resistors are sized to limit the input currents into the analog inputs to <10 mA in all circumstances (for example, if the device is unpowered and an input signal is applied).
- The device is the only target on the I<sup>2</sup>C bus.

**Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground**

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
AIN2/GPIO2	1	AIN2/GPIO2 is configured as an analog input. The conversion result for this channel will be close to 0x000.	B
		AIN2/GPIO2 is configured as a digital input: GPIO2 is stuck low. The readback value of GPI_VALUE[2] will be 0b.	B
		AIN2/GPIO2 is configured as a digital output: GPIO2 is stuck low. Increase in supply current when GPIO2 tries to drive high. Device damage may be plausible.	A
AIN3/GPIO3	2	AIN3/GPIO3 is configured as an analog input. The conversion result for this channel will be close to 0x000.	B
		AIN3/GPIO3 is configured as a digital input: GPIO3 is stuck low. The readback value of GPI_VALUE[3] will be 0b.	B
		AIN3/GPIO3 is configured as a digital output: GPIO3 is stuck low. Increase in supply current when GPIO3 tries to drive high. Device damage may be plausible.	A
AIN4/GPIO4	3	AIN4/GPIO4 is configured as an analog input. The conversion result for this channel will be close to 0x000.	B
		AIN4/GPIO4 is configured as a digital input: GPIO4 is stuck low. The readback value of GPI_VALUE[4] will be 0b.	B
		AIN4/GPIO4 is configured as a digital output: GPIO4 is stuck low. Increase in supply current when GPIO4 tries to drive high. Device damage may be plausible.	A
AIN5/GPIO5	4	AIN5/GPIO5 is configured as an analog input. The conversion result for this channel will be close to 0x000.	B
		AIN5/GPIO5 is configured as a digital input: GPIO5 is stuck low. The readback value of GPI_VALUE[5] will be 0b.	B
		AIN5/GPIO5 is configured as a digital output: GPIO5 is stuck low. Increase in supply current when GPIO5 tries to drive high. Device damage may be plausible.	A
AIN6/GPIO6	5	AIN6/GPIO6 is configured as an analog input. The conversion result for this channel will be close to 0x000.	B
		AIN6/GPIO6 is configured as a digital input: GPIO6 is stuck low. The readback value of GPI_VALUE[6] will be 0b.	B
		AIN6/GPIO6 configured as a digital output: GPIO6 is stuck low. Increase in supply current when GPIO6 tries to drive high. Device damage may be plausible.	A
AIN7/GPIO7	6	AIN7/GPIO7 is configured as an analog input. The conversion result for this channel will be close to 0x000.	B
		AIN7/GPIO7 is configured as a digital input: GPIO7 is stuck low. The readback value of GPI_VALUE[7] will be 0b.	B
		AIN7/GPIO7 is configured as a digital output: GPIO7 is stuck low. Increase in supply current when GPIO7 tries to drive high. Device damage may be plausible.	A
AVDD	7	Device unpowered and not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
DECAP	8	Device not functional. Increase in supply current. Device damage may be plausible.	A
GND	9	No effect. Normal operation.	D
DVDD	10	Device unpowered and not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
ADDR	11	I <sup>2</sup> C address is 0x10. If the device is supposed to be configured for a different I <sup>2</sup> C address, then no I <sup>2</sup> C communication with the device is possible.	B
		I <sup>2</sup> C address is 0x10. If the device is supposed to be configured for I <sup>2</sup> C address 0x10, then normal operation.	D
ALERT	12	The ALERT pin is configured as an open-drain output: no alert indication is possible. Otherwise, normal operation.	B
		The ALERT pin is configured as a push-pull output. No alert indication is possible. Increase in supply current when ALERT tries to drive high. Device damage plausible if ALERT drives high for an extended period of time.	A
SCL	13	SCL is stuck low. No I <sup>2</sup> C communication with the device is possible.	B

**Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)**

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SDA	14	SDA is stuck low. No I <sup>2</sup> C communication with the device is possible.	B
AIN0/GPIO0	15	AIN0/GPIO0 is configured as an analog input. The conversion result for this channel will be close to 0x000.	B
		AIN0/GPIO0 is configured as a digital input: GPIO0 is stuck low. The readback value of GPI_VALUE[0] will be 0b.	B
		AIN0/GPIO0 is configured as a digital output: GPIO0 is stuck low. Increase in supply current when GPIO0 tries to drive high. Device damage may be plausible.	A
AIN1/GPIO1	16	AIN1/GPIO1 is configured as an analog input. The conversion result for this channel will be close to 0x000.	B
		AIN1/GPIO1 is configured as a digital input: GPIO1 is stuck low. The readback value of GPI_VALUE[1] will be 0b.	B
		AIN1/GPIO1 is configured as a digital output: GPIO1 is stuck low. Increase in supply current when GPIO1 tries to drive high. Device damage may be plausible.	A
Thermal Pad	—	No effect. Normal operation.	D

**Table 4-3. Pin FMA for Device Pins Open-Circuited**

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
AIN2/GPIO2	1	AIN2/GPIO2 is configured as an analog input. The conversion result for this channel will be undetermined.	B
		AIN2/GPIO2 is configured as a digital input. The readback value of GPI_VALUE[2] will be undetermined.	B
		AIN2/GPIO2 is configured as a digital output. No logic signaling between GPIO2 and the external circuit is possible. Otherwise, normal operation.	D
AIN3/GPIO3	2	AIN3/GPIO3 is configured as an analog input. The conversion result for this channel will be undetermined.	B
		AIN3/GPIO3 is configured as a digital input: GPIO3 is stuck low. The readback value of GPI_VALUE[3] will be undetermined.	B
		AIN3/GPIO3 is configured as a digital output. No logic signaling between GPIO3 and the external circuit is possible. Otherwise, normal operation.	D
AIN4/GPIO4	3	AIN4/GPIO4 is configured as an analog input. The conversion result for this channel will be undetermined.	B
		AIN4/GPIO4 is configured as a digital input: GPIO4 is stuck low. The readback value of GPI_VALUE[4] will be undetermined.	B
		AIN4/GPIO4 is configured as a digital output. No logic signaling between GPIO4 and the external circuit is possible. Otherwise, normal operation.	D
AIN5/GPIO5	4	AIN5/GPIO5 is configured as an analog input. The conversion result for this channel will be undetermined.	B
		AIN5/GPIO5 is configured as a digital input: GPIO5 is stuck low. The readback value of GPI_VALUE[5] will be undetermined.	B
		AIN5/GPIO5 is configured as a digital output. No logic signaling between GPIO5 and the external circuit is possible. Otherwise, normal operation.	D
AIN6/GPIO6	5	AIN6/GPIO6 is configured as an analog input. The conversion result for this channel will be undetermined.	B
		AIN6/GPIO6 is configured as a digital input: GPIO6 is stuck low. The readback value of GPI_VALUE[6] will be undetermined.	B
		AIN6/GPIO6 is configured as a digital output. No logic signaling between GPIO6 and the external circuit is possible. Otherwise, normal operation.	D

**Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)**

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
AIN7/GPIO7	6	AIN7/GPIO7 is configured as an analog input. The conversion result for this channel will be undetermined.	B
		AIN7/GPIO7 is configured as a digital input: GPIO7 is stuck low. The readback value of GPI_VALUE[7] will be undetermined.	B
		AIN7/GPIO7 is configured as a digital output. No logic signaling between GPIO7 and the external circuit is possible. Otherwise, normal operation.	D
AVDD	7	Device functionality undetermined. The device is unpowered and not functional if all external analog pins are held low. Observe that the absolute maximum ratings for all analog pins of the device are met, otherwise device damage may be plausible. The device may power up through internal ESD diodes to AVDD if voltages above the device power-on reset threshold are present on any of the analog pins.	A
DECAP	8	Device not functional. Increase in supply current. Device damage may be plausible.	A
GND	9	Device functionality undetermined. The device may be unpowered or connect to ground internally through alternate pin ESD diode and power up.	B
DVDD	10	Digital interface is not powered up if all external digital pins are held low. No I <sup>2</sup> C communication with the device is possible. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible. Digital interface may power up through internal ESD diodes to DVDD if voltages above the device power-on reset threshold are present on any of the digital pins.	A
ADDR	11	I <sup>2</sup> C address is 0x10. If the device is supposed to be configured for a different I <sup>2</sup> C address, then no I <sup>2</sup> C communication with the device is possible.	B
		I <sup>2</sup> C address is 0x10. If the device is supposed to be configured for I <sup>2</sup> C address 0x10, then normal operation.	D
ALERT	12	The ALERT pin is configured as an open-drain output. No alert indication possible. Otherwise, normal operation.	B
		The ALERT pin is configured as push-pull output. No alert indication possible. Otherwise, normal operation.	B
SCL	13	No I <sup>2</sup> C communication with the device is possible.	B
SDA	14	No I <sup>2</sup> C communication with the device is possible.	B
AIN0/GPIO0	15	AIN0/GPIO0 is configured as an analog input. The conversion result for this channel will be undetermined.	B
		AIN0/GPIO0 is configured as a digital input: GPIO0 is stuck low. The readback value of GPI_VALUE[0] will be undetermined.	B
		AIN0/GPIO0 is configured as digital output. No logic signaling between GPIO0 and the external circuit is possible. Otherwise, normal operation.	D
AIN1/GPIO1	16	AIN1/GPIO1 is configured as an analog input. The conversion result for this channel will be undetermined.	B
		AIN1/GPIO1 is configured as digital input: GPIO1 is stuck low. The readback value of GPI_VALUE[1] will be undetermined.	B
		AIN1/GPIO1 is configured as a digital output. No logic signaling between GPIO1 and an external circuit is possible. Otherwise, normal operation.	D
Thermal Pad	—	No effect. Normal operation.	D

**Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin**

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
AIN2/GPIO2	1	AIN3/GPIO3	AIN2/GPIO2 and AIN3/GPIO3 are configured as analog inputs. The conversion results for AIN2 and AIN3 are the same. Depending on the external circuits driving AIN2 and AIN3, the conversion results may be incorrect.	B
			AIN2/GPIO2 is configured as an analog input and AIN3/GPIO3 is configured as a digital input. The conversion result for AIN2 may be incorrect depending on the external circuit driving GPIO3. The readback value of GPI_VALUE[3] may be incorrect.	B
			AIN2/GPIO2 is configured as an analog input and AIN3/GPIO3 is configured as a digital output. The conversion result for AIN2 may be incorrect. There may be an increase in supply current when GPIO3 tries to drive high when the AIN2 voltage is low and vice versa. Device damage may be plausible.	A
			AIN2/GPIO2 is configured as a digital input and AIN3/GPIO3 is configured as analog input. The conversion result for AIN3 may be incorrect depending on the external circuit driving GPIO2. The readback value of GPI_VALUE[2] may be incorrect.	B
			AIN2/GPIO2 and AIN3/GPIO3 are configured as digital inputs. The readback values of GPI_VALUE[2] and GPI_VALUE[3] are the same. The readback values may be incorrect depending on the external circuits driving these pins.	B
			AIN2/GPIO2 is configured as a digital input and AIN3/GPIO3 is configured as a digital output. The readback value of GPI_VALUE[2] depends on the output drive on GPIO3.	B
			AIN2/GPIO2 is configured as a digital output and AIN3/GPIO3 is configured as an analog input. The conversion result for AIN3 may be incorrect. There may be an increase in supply current when GPIO2 tries to drive high when AIN3 voltage is low and vice versa. Device damage may be plausible.	A
			AIN2/GPIO2 is configured as a digital output and AIN3/GPIO3 is configured as a digital input. The readback value of GPI_VALUE[3] depends on the output drive on GPIO2.	B
			AIN2/GPIO2 and AIN3/GPIO3 are configured as digital outputs. Increase in supply current when GPIO2 tries to drive low and GPIO3 tries to drive high and vice versa. Device damage may be plausible.	A

**Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)**

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
AIN3/GPIO3	2	AIN4/GPIO4	AIN3/GPIO3 and AIN4/GPIO4 are configured as analog inputs. The conversion results for AIN3 and AIN4 are the same. Depending on the external circuits driving AIN3 and AIN4, the conversion results may be incorrect.	B
			AIN3/GPIO3 is configured as an analog input and AIN4/GPIO4 is configured as a digital input. The conversion result for AIN3 may be incorrect depending on the external circuit driving GPIO4. The readback value of GPI_VALUE[4] may be incorrect.	B
			AIN3/GPIO3 is configured as an analog input and AIN4/GPIO4 is configured as a digital output. The conversion result for AIN3 may be incorrect. There may be an increase in supply current when GPIO4 tries to drive high when the AIN3 voltage is low and vice versa. Device damage may be plausible.	A
			AIN3/GPIO3 is configured as a digital input and AIN4/GPIO4 is configured as an analog input. The conversion result for AIN4 may be incorrect depending on the external circuit driving GPIO3. The readback value of GPI_VALUE[3] may be incorrect.	B
			AIN3/GPIO3 and AIN4/GPIO4 are configured as digital inputs. The readback values of GPI_VALUE[3] and GPI_VALUE[4] are the same. The readback values may be incorrect depending on the external circuits driving these pins.	B
			AIN3/GPIO3 is configured as a digital input and AIN4/GPIO4 is configured as a digital output. The readback value of GPI_VALUE[3] depends on the output drive on GPIO4.	B
			AIN3/GPIO3 is configured as a digital output and AIN4/GPIO4 is configured as an analog input. The conversion result for AIN4 may be incorrect. There may be an increase in supply current when GPIO3 tries to drive high when the AIN4 voltage is low and vice versa. Device damage may be plausible.	A
			AIN3/GPIO3 is configured as a digital output and AIN4/GPIO4 is configured as a digital input. The readback value of GPI_VALUE[4] depends on the output drive on GPIO3.	B
AIN3/GPIO3 and AIN4/GPIO4 are configured as digital outputs. Increase in supply current when GPIO3 tries to drive low and GPIO4 tries to drive high and vice versa. Device damage may be plausible.	A			

**Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)**

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
AIN4/GPIO4	3	AIN5/GPIO5	AIN4/GPIO4 and AIN5/GPIO5 are configured as analog inputs. The conversion results for AIN4 and AIN5 are the same. Depending on the external circuits driving AIN4 and AIN5, the conversion results may be incorrect.	B
			AIN4/GPIO4 is configured as an analog input and AIN5/GPIO5 is configured as a digital input. The conversion result for AIN4 may be incorrect depending on the external circuit driving GPIO5. The readback value of GPI_VALUE[5] may be incorrect.	B
			AIN4/GPIO4 is configured as analog input and AIN5/GPIO5 is configured as a digital output. The conversion result for AIN4 may be incorrect. There may be an increase in supply current when GPIO5 tries to drive high when the AIN4 voltage is low and vice versa. Device damage may be plausible.	A
			AIN4/GPIO4 is configured as a digital input and AIN5/GPIO5 is configured as an analog input. The conversion result for AIN5 may be incorrect depending on the external circuit driving GPIO4. The readback value of GPI_VALUE[4] may be incorrect.	B
			AIN4/GPIO4 and AIN5/GPIO5 are configured as digital inputs. The readback values of GPI_VALUE[4] and GPI_VALUE[5] are the same. The readback values may be incorrect depending on the external circuits driving these pins.	B
			AIN4/GPIO4 is configured as a digital input and AIN5/GPIO5 is configured as a digital output. The readback value of GPI_VALUE[4] depends on the output drive on GPIO5.	B
			AIN4/GPIO4 is configured as a digital output and AIN5/GPIO5 is configured as an analog input. The conversion result for AIN5 may be incorrect. There may be an increase in supply current when GPIO4 tries to drive high when the AIN5 voltage is low and vice versa. Device damage may be plausible.	A
			AIN4/GPIO4 is configured as a digital output and AIN5/GPIO5 is configured as a digital input. The readback value of GPI_VALUE[5] depends on the output drive on GPIO4.	B
			AIN4/GPIO4 and AIN5/GPIO5 are configured as digital outputs. Increase in supply current when GPIO4 tries to drive low and GPIO5 tries to drive high and vice versa. Device damage may be plausible.	A
AIN5/GPIO5	4	—	Not considered. Corner pin.	-

**Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)**

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
AIN6/GPIO6	5	AIN7/GPIO7	AIN6/GPIO6 and AIN7/GPIO7 are configured as analog inputs. The conversion results for AIN6 and AIN7 are the same. Depending on the external circuits driving AIN6 and AIN7, the conversion results may be incorrect.	B
			AIN6/GPIO6 is configured as an analog input and AIN7/GPIO7 is configured as a digital input. The conversion result for AIN6 may be incorrect depending on the external circuit driving GPIO7. The readback value of GPI_VALUE[7] may be incorrect.	B
			AIN6/GPIO6 is configured as an analog input and AIN7/GPIO7 is configured as a digital output. The conversion result for AIN6 may be incorrect. There may be an increase in supply current when GPIO7 tries to drive high when the AIN6 voltage is low and vice versa. Device damage may be plausible.	A
			AIN6/GPIO6 is configured as a digital input and AIN7/GPIO7 is configured as an analog input. The conversion result for AIN7 may be incorrect depending on the external circuit driving GPIO6. The readback value of GPI_VALUE[6] may be incorrect.	B
			AIN6/GPIO6 and AIN7/GPIO7 are configured as digital inputs. The readback values of GPI_VALUE[6] and GPI_VALUE[7] are the same. The readback values may be incorrect depending on the external circuits driving these pins.	B
			AIN6/GPIO6 is configured as a digital input and AIN7/GPIO7 is configured as a digital output. The readback value of GPI_VALUE[6] depends on the output drive on GPIO7.	B
			AIN6/GPIO6 is configured as a digital output and AIN7/GPIO7 is configured as an analog input. The conversion result for AIN7 may be incorrect. There may be an increase in supply current when GPIO6 tries to drive high when the AIN7 voltage is low and vice versa. Device damage may be plausible.	A
			AIN6/GPIO6 is configured as a digital output and AIN7/GPIO7 is configured as a digital input. The readback value of GPI_VALUE[7] depends on the output drive on GPIO6.	B
AIN7/GPIO7	6	AVDD	AIN6/GPIO6 and AIN7/GPIO7 are configured as digital outputs. Increase in supply current when GPIO6 tries to drive low and GPIO7 tries to drive high and vice versa. Device damage may be plausible.	A
			AIN7/GPIO7 is configured as an analog input. The conversion result for AIN7 is close to 0xFFFF.	B
			AIN7/GPIO7 is configured as a digital input: GPIO7 is stuck high. The readback value of GPI_VALUE[7] is 1b.	B
AVDD	7	DECAP	AIN7/GPIO7 is configured as a digital output: GPIO7 is stuck high. Increase in supply current when GPIO7 tries to drive low. Device damage may be plausible.	A
			A voltage higher than the absolute maximum rating is applied to the pin because the minimum supply voltage is higher than the absolute maximum voltage rating of the DECAP pin. Device damage may be plausible.	A
DECAP	8	—	Not considered. Corner pin.	-
GND	9	DVDD	Device unpowered and not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
DVDD	10	ADDR	The I <sup>2</sup> C address is 0x17. If the device is supposed to be configured for a different I <sup>2</sup> C address, then no I <sup>2</sup> C communication with the device is possible.	B
			The I <sup>2</sup> C address is 0x17. If the device is supposed to be configured for I <sup>2</sup> C address 0x17, then normal operation.	D
			Device damage may be plausible if the voltage on the DVDD pin is higher than the absolute maximum rating of the ADDR pin.	A

**Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)**

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
ADDR	11	ALERT	The I <sup>2</sup> C address depends on the voltage on the ADDR pin during device power-up or reset. I <sup>2</sup> C communication with the device may not be possible.	B
ALERT	12	—	Not considered. Corner pin.	-
SCL	13	SDA	No I <sup>2</sup> C communication with the device is possible.	B
SDA	14	AIN0/GPIO0	AIN0/GPIO0 is configured as an analog input. I <sup>2</sup> C communication with device may not be possible depending on the voltage and external impedance connected to the AIN0/GPIO0 pin. The conversion result for AIN0 may be incorrect.	B
			AIN0/GPIO0 is configured as a digital input. I <sup>2</sup> C communication with device may not be possible depending on the voltage and external impedance connected to the AIN0/GPIO0 pin. The readback value of GPI_VALUE[0] may be incorrect.	B
			AIN0/GPIO0 is configured as a digital output. No I <sup>2</sup> C communication with the device is possible. Device damage may be plausible when SDA is driven low and GPIO0 tries to drive high.	A
AIN0/GPIO0	15	AIN1/GPIO1	AIN0/GPIO0 and AIN1/GPIO1 are configured as analog inputs. The conversion results for AIN0 and AIN1 are the same. Depending on the external circuits driving AIN0 and AIN1, the conversion result may be incorrect.	B
			AIN0/GPIO0 is configured as an analog input and AIN1/GPIO1 is configured as a digital input. The conversion result for AIN0 may be incorrect depending on the external circuit driving GPIO1. The readback value of GPI_VALUE[1] may be incorrect.	B
			AIN0/GPIO0 is configured as an analog input and AIN1/GPIO1 is configured as a digital output. The conversion result for AIN0 may be incorrect. There may be an increase in supply current when GPIO1 tries to drive high when the AIN0 voltage is low and vice versa. Device damage may be plausible.	A
			AIN0/GPIO0 is configured as a digital input and AIN1/GPIO1 is configured as an analog input. The conversion result for AIN1 may be incorrect depending on the external circuit driving GPIO0. The readback value of GPI_VALUE[0] may be incorrect.	B
			AIN0/GPIO0 and AIN1/GPIO1 are configured as digital inputs. The readback values of GPI_VALUE[0] and GPI_VALUE[1] are the same. The readback values may be incorrect depending on the external circuits driving these pins.	B
			AIN0/GPIO0 is configured as a digital input and AIN1/GPIO1 is configured as a digital output. The readback value of GPI_VALUE[0] depends on the output drive on GPIO1.	B
			AIN0/GPIO0 is configured as a digital output and AIN1/GPIO1 is configured as an analog input. The conversion result for AIN1 may be incorrect. There may be an increase in supply current when GPIO0 tries to drive high when the AIN1 voltage is low and vice versa. Device damage may be plausible.	A
			AIN0/GPIO0 is configured as a digital output and AIN1/GPIO1 is configured as a digital input. The readback value of GPI_VALUE[1] depends on the output drive on GPIO0.	B
			AIN0/GPIO0 and AIN1/GPIO1 are configured as digital outputs. Increase in supply current when GPIO0 tries to drive low and GPIO1 tries to drive high and vice versa. Device damage may be plausible.	A
AIN1/GPIO1	16	—	Not considered. Corner pin.	-
Thermal Pad	—	—	See the <a href="#">Pin FMA for Device Pins Short-Circuited to Ground</a> condition for respective device pins.	-

**Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply**

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
AIN2/GPIO2	1	AIN2/GPIO2 is configured as an analog input. The conversion result for this channel will be close to 0xFFFF.	B
		AIN2/GPIO2 is configured as a digital input: GPIO2 is stuck high. The readback value of GPI_VALUE[2] will be 1b.	B
		AIN2/GPIO2 is configured as a digital output: GPIO2 is stuck high. Increase in supply current when GPIO2 tries to drive low. Device damage may be plausible.	A
AIN3/GPIO3	2	AIN3/GPIO3 is configured as an analog input. The conversion result for this channel will be close to 0xFFFF.	B
		AIN3/GPIO3 is configured as a digital input: GPIO3 is stuck high. The readback value of GPI_VALUE[3] will be 1b.	B
		AIN3/GPIO3 is configured as a digital output: GPIO3 is stuck high. Increase in supply current when GPIO3 tries to drive low. Device damage may be plausible.	A
AIN4/GPIO4	3	AIN4/GPIO4 is configured as an analog input. The conversion result for this channel will be close to 0xFFFF.	B
		AIN4/GPIO4 is configured as a digital input: GPIO4 is stuck high. The readback value of GPI_VALUE[4] will be 1b.	B
		AIN4/GPIO4 is configured as a digital output: GPIO4 is stuck high. Increase in supply current when GPIO4 tries to drive low. Device damage may be plausible.	A
AIN5/GPIO5	4	AIN5/GPIO5 is configured as an analog input. The conversion result for this channel will be close to 0xFFFF.	B
		AIN5/GPIO5 is configured as a digital input: GPIO5 is stuck high. The readback value of GPI_VALUE[5] will be 1b.	B
		AIN5/GPIO5 is configured as a digital output: GPIO5 is stuck high. Increase in supply current when GPIO5 tries to drive low. Device damage may be plausible.	A
AIN6/GPIO6	5	AIN6/GPIO6 is configured as an analog input. The conversion result for this channel will be close to 0xFFFF.	B
		AIN6/GPIO6 is configured as a digital input: GPIO6 is stuck high. The readback value of GPI_VALUE[6] will be 1b.	B
		AIN6/GPIO6 is configured as a digital output: GPIO6 is stuck high. Increase in supply current when GPIO6 tries to drive low. Device damage may be plausible.	A
AIN7/GPIO7	6	AIN7/GPIO7 is configured as an analog input. The conversion result for this channel will be close to 0xFFFF.	B
		AIN7/GPIO7 is configured as a digital input: GPIO7 is stuck high. The readback value of GPI_VALUE[7] will be 1b.	B
		AIN7/GPIO7 is configured as a digital output: GPIO7 is stuck high. Increase in supply current when GPIO7 tries to drive low. Device damage may be plausible.	A
AVDD	7	No effect. Normal operation.	D
DECAP	8	A voltage higher than the absolute maximum rating is applied to the pin because the minimum supply voltage is higher than the absolute maximum voltage rating of the DECAP pin. Device damage may be plausible.	A
GND	9	Device unpowered and not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
DVDD	10	No effect. Normal operation.	D
ADDR	11	The I <sup>2</sup> C address is 0x17. If the device is supposed to be configured for a different I <sup>2</sup> C address, then no I <sup>2</sup> C communication with the device is possible.	B
		The I <sup>2</sup> C address is 0x17. If the device is supposed to be configured for I <sup>2</sup> C address 0x17, then normal operation.	D

**Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply (continued)**

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
ALERT	12	The ALERT pin is configured as an open-drain output. No alert indication is possible. Increase in supply current when ALERT tries to drive low. Device damage plausible if ALERT drives low for an extended period of time.	A
		The ALERT pin is configured as a push-pull output. No alert indication is possible. Increase in supply current when ALERT tries to drive low. Device damage plausible if ALERT drives low for an extended period of time.	A
SCL	13	No I <sup>2</sup> C communication with the device is possible. Increase in supply current when SCL tries to drive low. Device damage plausible if SCL drives low for an extended period of time.	A
SDA	14	No I <sup>2</sup> C communication with device is possible. Increase in supply current when SDA tries to drive low. Device damage plausible if SDA drives low for extended an period of time.	A
AIN0/GPIO0	15	AIN0/GPIO0 is configured as an analog input. The conversion result for this channel will be close to 0xFFFF.	B
		AIN0/GPIO0 is configured as a digital input: GPIO0 is stuck high. The readback value of GPI_VALUE[0] will be 1b.	B
		AIN0/GPIO0 is configured as a digital output: GPIO0 is stuck high. Increase in supply current when GPIO0 tries to drive low. Device damage may be plausible.	A
AIN1/GPIO1	16	AIN1/GPIO1 is configured as an analog input. The conversion result for this channel will be close to 0xFFFF.	B
		AIN1/GPIO1 is configured as a digital input: GPIO1 is stuck high. The readback value of GPI_VALUE[1] will be 1b.	B
		AIN1/GPIO1 is configured as a digital output: GPIO1 is stuck high. Increase in supply current when GPIO1 tries to drive low. Device damage may be plausible.	A
Thermal Pad	—	Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2022, Texas Instruments Incorporated