TEXAS INSTRUMENTS

Modeling the ADS5500/20/21/22/41/42 series of components through IBIS

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Introduction

This document describes how the output buffers in the ADS5500/20/21/22/41/42 family of devices are modeled using IBIS. These buffers are special in that, the rate of rise and fall at the output is controlled using certain feedback circuits. Therefore, an accurate representation of this buffer through an IBIS model requires multiple models.

The CMOS output buffers for data and clock signals have been modeled. The architecture (and hence model generation method) for both are identical except that the clock buffer has greater drive strength.

Buffer architecture

The output buffer block contains the pull-up, pull-down, power-clamp and the ground clamp circuits (as is present in any normal output buffer) as shown in Fig.1. The pull-up and pull-down circuits are switches operated/controlled by the input to the buffer.

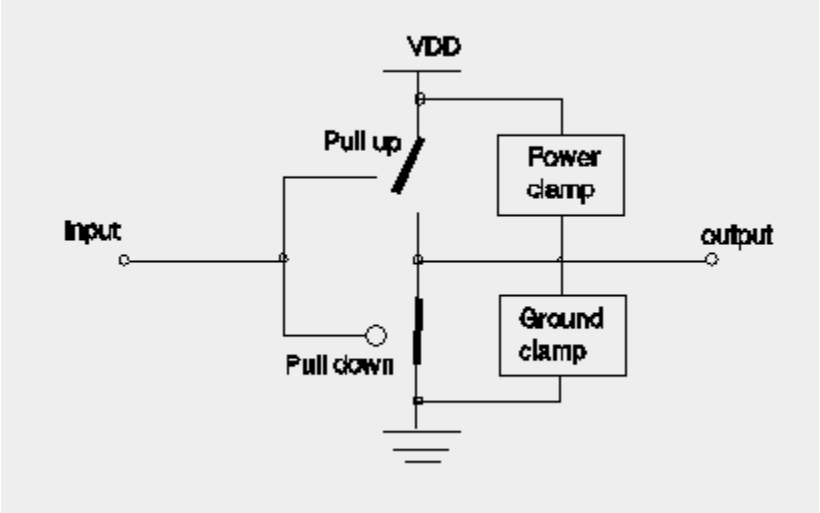

Figure 1. Internal structure of output buffer block

Pull-down and Pull-up V-I tables

Since the output buffer doesn't have a tri-state output, the power clamp and ground clamp data are merged into the pull-up and pull down tables respectively. The setup for extraction of pull-up data is shown in Figure.2. The buffer is non-inverting. So at input a

source of value Vih is connected so that the pull-up switch is on and pull-down switch is off. A voltage source is connected between output and the power supply and is varied from –VDD to +2VDD. The current through the source is measured and tabulated.

The setup for extraction of pull-down data is shown in Figure.3. The pull-up switch is off and pull-down switch is on. A voltage source connected between output and ground is varied from –VDD to +2VDD. The current through the source is measured and tabulated.

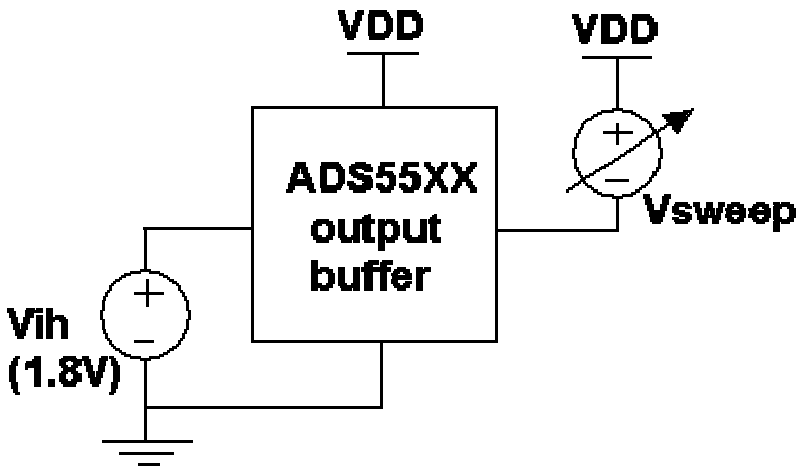

Figure 2. Voltage sweep for Pull-up table

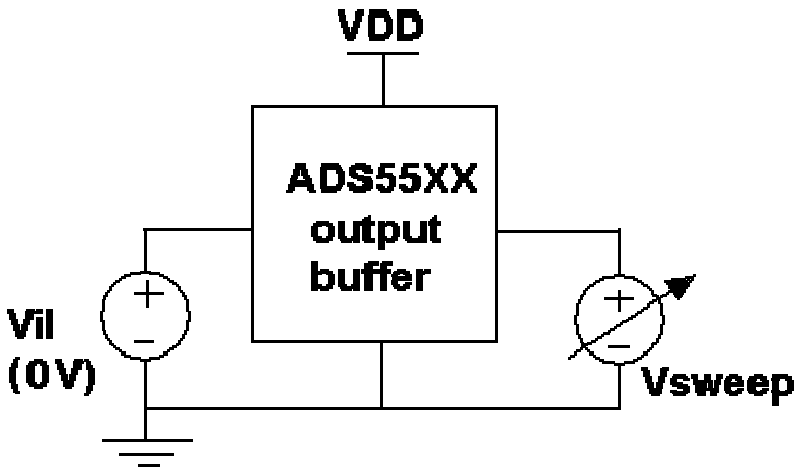

Figure 3. Voltage sweep for Pull-down table

V-t Tables (Rise and Fall curves)

For IBIS modeling, V-t curves are generated with a resistive load attached at the output. (Here a 50 ohms load was used). There are 4 V-t curves generated per model and the circuit setups for each of them are as shown in Figures 4 to 7.

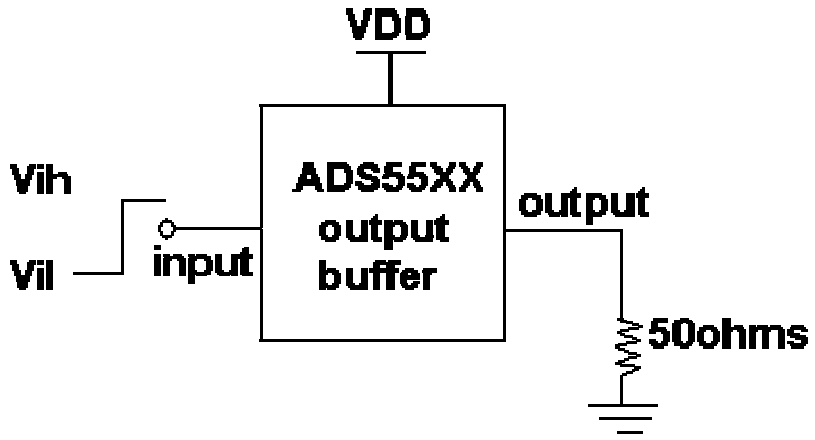

Figure 4. Rising waveform with resistive load connected to pull-down reference (ground).

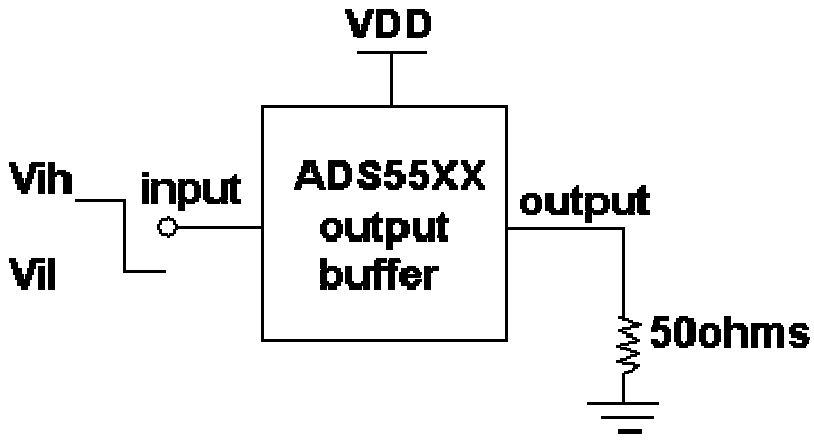

Figure 5. Falling waveform with resistive load connected to pull-down reference (ground).

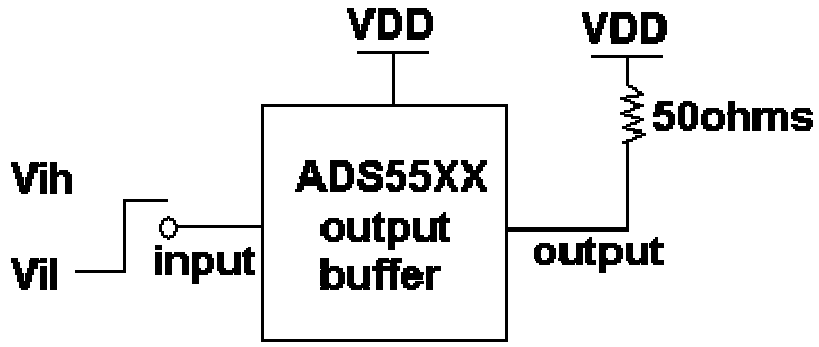

Figure 6. Rising waveform with resistive load connected to pull-up reference (VDD).

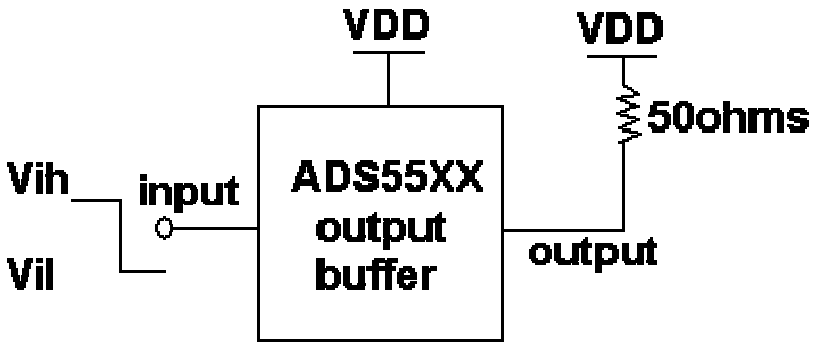

Figure 7. Falling waveform with resistive load connected to pull-up reference (VDD).

Comparison of IBIS model with the actual circuit

The IBIS models generated, are compared with the actual circuit through SPICE simulations. Figure 8 shows the circuit simulation setup for the buffer under nominal conditions driving a transmission line (400 ps delay) terminated by a 4pF capacitor. Two simulations are performed

1. In the 1st simulation the IBIS model of the buffer is used.
2. In the 2nd simulation the actual SPICE netlist of the buffer is used.

The output at load is measured. The results of the 2 simulations are compared in Figure 9.

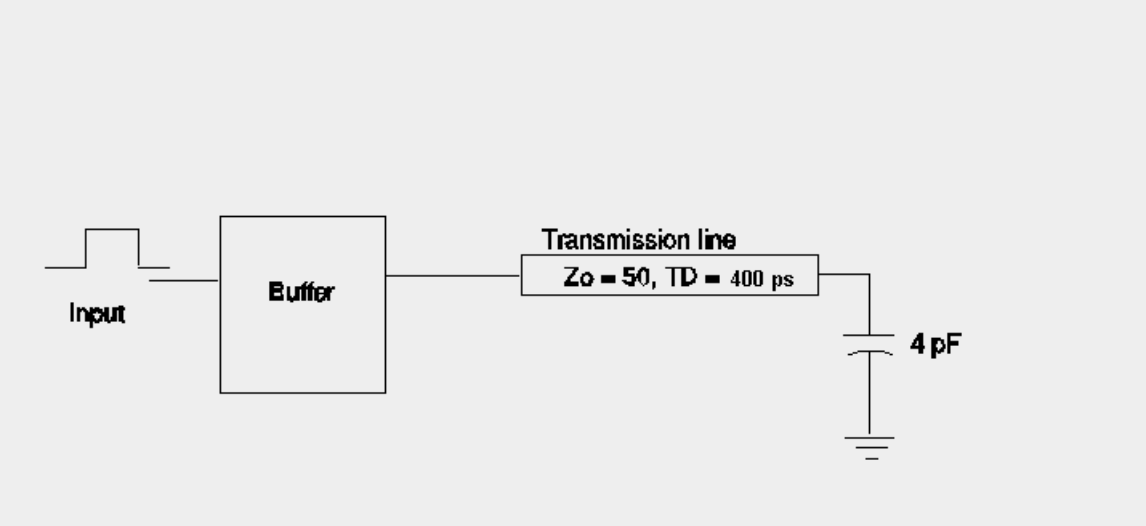

Figure 8. Simulation of buffer driving a transmission line terminated by a 4pF capacitor

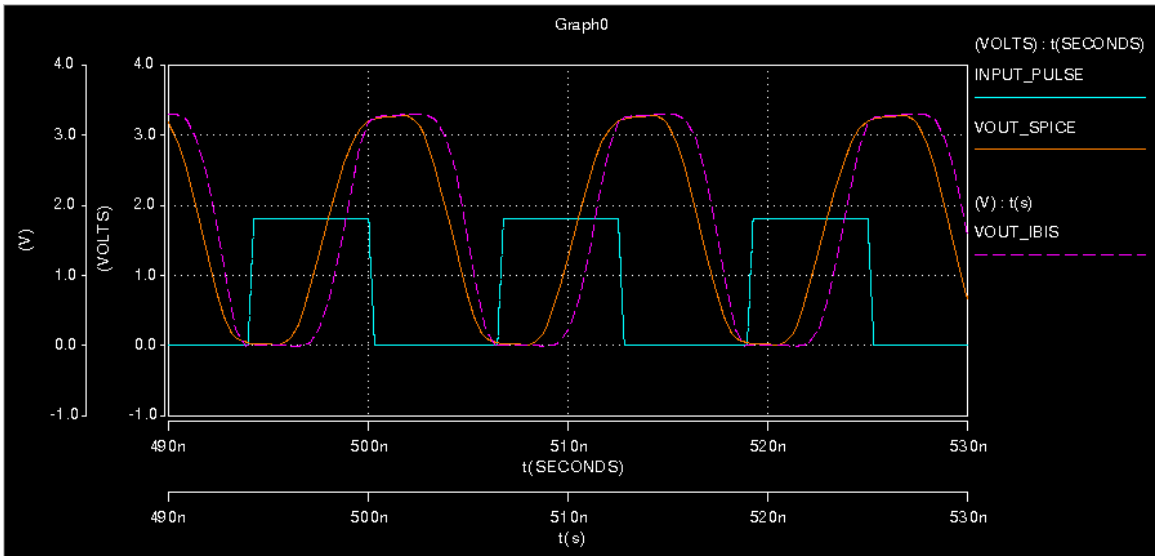

Figure 9. Simulation of buffer driving a transmission line terminated by a 4pF capacitor

Quality Verification:

The created IBIS models were verified as follows:

1. Visual check of each characteristics using the s2iplt tool
2. Syntax check by IBISCHK4
3. Behavior of IBIS models and actual circuit compared using SPICE

MODEL SUMMARY

Buffer name – ADS55XX

Model names – DATAOBUF and CLKOBUF

Model type - Output buffer

Filename - ads55xx.ibs

Modeling conditions:

Condition	Typ/ min/ max
AVDD	3.3 V/ 3.0 V/ 3.6 V
Junction temperature (Tj)	50/ 105/ -20 (degree C)
Process setting	nominal/ weak/ strong

Package Characteristics:

Characteristics	Typ/ min/ max
R_pkg:	0.019 / 0.019 / 0.020 (ohms)
L_pkg	2.580nH / 2.419nH / 2.812nH
C_pkg	482fF / 419fF / 518fF

Note: While using the models for transient simulations, use of both pairs of V-t curves gives better results than just one V-t curve.

Sample instantiation of the IBIS models in TISPICE:

Boutput pu pd d_4 DATA pc gc

+ FILE = ads55xx.ibs

+ MODEL = DATAOBUF_125_400_4

+ TYP=typ

+ ramp_fwf=2

+ ramp_rwf=2

Sample HSPICE deck using the IBIS model

Following deck can be used to simulate the data buffer operating at 125msps driving 400ps delay line terminated by a 4pF capacitance (using HSPICE).

****

* Buffer *

****

Boutput pu pd DATAOUT DATA pc gc

+ FILE = "ads55xx.ibs"

+ MODEL = DATAOBUF_125_400_4

+ ramp_fwf=2

+ ramp_rwf=2

+ TYP=typ

* TRANSMISSION LINE LOAD

T1 DATAOUT 0 op 0 Z0=50 TD = 400ps

* CAPACITANCE AT RECEIVER END

CFIXS2I op 0 4pF

* STIMULUS

VINS2I DATA 0 PULSE(0 1.8 1e-09 3e-10 3e-10 8e-09 16e-09)

.TEMP 50

.TRAN 1e-10 60e-09

.OPTIONS POST

.PLOT TRAN V(DATAOUT) V(data) V(OP)

.END

IBIS Model file (ads55xx.ibs)

The IBIS models for both data and clock buffers have been generated for 48 types of load conditions as described below.

1. There are typically 3 data rates : 80MSPS, 105MSPS and 125MSPS.
2. The transmission line load is assumed to have 400ps, 600ps or 800ps delay. The case of no transmission line also was considered. Hence there are 4 possible types of load.
3. The capacitive load termination considered are 4pF, 8pF, 12pF and 15pF (4 types)

Hence the total no. of models generated are 2 x 3 x 4 x 4 = 96 models.

All the above models are merged into one model file, in which the model data for each model are tabulated under key word [Model] followed by model name. The syntax for model name is as follows :

For data buffer : DATAOBUF_<*speed*>_<*delay of transmission line*>_<*capacitive load*>

For clock buffer CLKOBUF_<*speed*>_<*delay of transmission line*>_<*capacitive load*>

e.g. the name of the model of the data buffer at 125 MSPS, driving a capacitive load of 4pF without any transmission line would be : DATAOBUF_125_0_4.