

## SN74LV125AT 3 ステート出力、クワッド・バス・バッファ・ゲート

### 1 特長

- 入力は TTL 電圧互換
- 4.5V～5.5V の  $V_{CC}$  で動作
- 標準  $t_{pd}$  3.8ns (5V 時)
- 標準  $V_{OLP}$  (出力グランド・バウンス)  $< 0.8V$  ( $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ )
- 標準  $V_{OHV}$  (出力  $V_{OH}$  アンダーシュート)  $> 2.3V$  ( $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ )
- すべてのポートで混在モード電圧動作をサポート
- $I_{off}$  により部分的パワーダウン・モード動作をサポート
- JESD 17 準拠で 250mA 超のラッチアップ性能

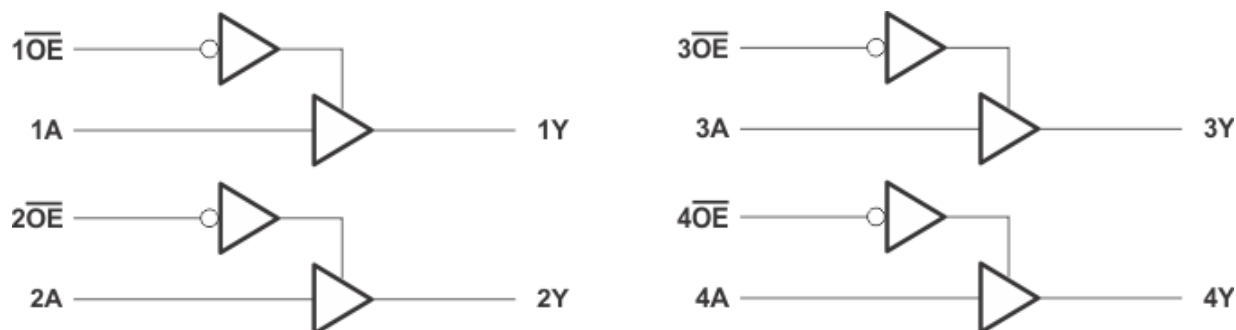
### 2 概要

SN74LV125AT はクワッド・バス・バッファ・ゲートです。このデバイスは、3 ステート出力の独立ライン・ドライバを備えています。各出力は、対応する出力イネーブル ( $\overline{OE}$ ) 入力が High のときディセーブルになります。

#### パッケージ情報

| 部品番号        | パッケージ <sup>1</sup> | パッケージ・サイズ <sup>2</sup> |
|-------------|--------------------|------------------------|
| SN74LV125AT | RGY (VQFN, 14)     | 3.50mm × 3.50mm        |
|             | D (SOIC, 14)       | 8.65mm × 6mm           |
|             | NS (SO, 14)        | 10.20mm × 7.8mm        |
|             | DB (SSOP, 14)      | 6.20mm × 7.8mm         |
|             | PW (TSSOP, 14)     | 5.00mm × 6.4mm         |

- (1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
- (2) パッケージ・サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



概略回路図



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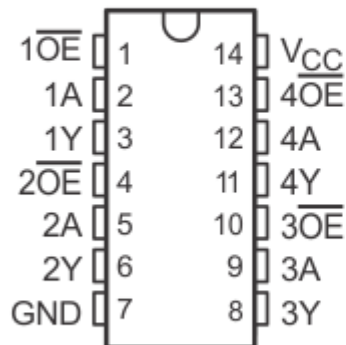
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## 3 Revision History

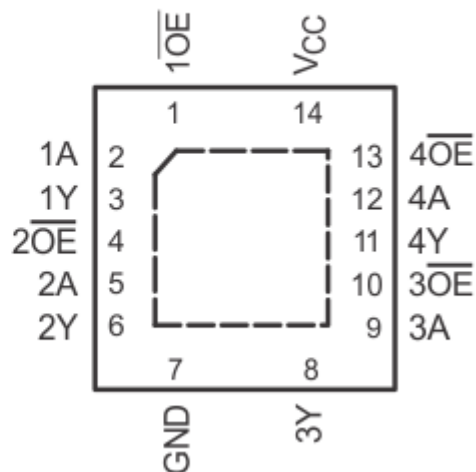
| Changes from Revision A (May 2023) to Revision B (July 2023)                                                                                                               | Page |
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| <ul style="list-style-type: none"> <li>「パッケージ情報」表、「ピンの機能」表、「ESD 定格」表、「熱に関する情報」表、「デバイスの機能モード」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 .....</li> </ul> | 1    |

## 4 Pin Configuration and Functions

SN74LV125A . . . D, DB, DGV, N, NS,  
OR PW PACKAGE  
(TOP VIEW)



SN74LV125A . . . RGY PACKAGE  
(TOP VIEW)



| PIN |      | TYPE <sup>(1)</sup> | DESCRIPTION                 |
|-----|------|---------------------|-----------------------------|
| NO. | NAME |                     |                             |
| 1   | 1OE  | I                   | Output Enable 1, Active Low |
| 2   | 1A   | I                   | 1A Input                    |
| 3   | 1Y   | O                   | 1Y Output                   |
| 4   | 2OE  | I                   | Output Enable 2, Active Low |
| 5   | 2A   | I                   | 2A Input                    |
| 6   | 2Y   | O                   | 2Y Output                   |
| 7   | GND  | —                   | Ground Pin                  |
| 8   | 3Y   | O                   | 3Y Output                   |
| 9   | 3A   | I                   | 3A Input                    |
| 10  | 3OE  | I                   | Output Enable 3, Active Low |
| 11  | 4Y   | O                   | 4Y Output                   |
| 12  | 4A   | I                   | 4A Input                    |
| 13  | 4OE  | I                   | Output Enable 4, Active Low |
| 14  | VCC  | —                   | Power Pin                   |

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                  |                                                                                             | MIN                                   | MAX                   | UNIT   |
|------------------|---------------------------------------------------------------------------------------------|---------------------------------------|-----------------------|--------|
| V <sub>CC</sub>  | Supply voltage                                                                              | −0.5                                  | 7                     | V      |
| V <sub>I</sub>   | Input voltage range <sup>(2)</sup>                                                          | −0.5                                  | 7                     | V      |
| V <sub>O</sub>   | Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup> | −0.5                                  | 7                     | V      |
| V <sub>O</sub>   | Output voltage range <sup>(2) (3)</sup>                                                     | −0.5                                  | V <sub>CC</sub> + 0.5 | V      |
| I <sub>IK</sub>  | Input clamp current                                                                         | V <sub>I</sub> < 0                    |                       | −20 mA |
| I <sub>OK</sub>  | Output clamp current                                                                        | V <sub>O</sub> < 0                    |                       | ±50 mA |
| I <sub>O</sub>   | Continuous output current                                                                   | V <sub>O</sub> = 0 to V <sub>CC</sub> |                       | ±35 mA |
|                  | Continuous current through V <sub>CC</sub> or GND                                           |                                       |                       | ±70 mA |
| T <sub>stg</sub> | Storage temperature                                                                         | −65                                   | 150                   | °C     |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [セクション 5.3](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 5.5-V maximum.

### 5.2 ESD Ratings

|                    |                         | MAX                                                                                      | UNIT  |
|--------------------|-------------------------|------------------------------------------------------------------------------------------|-------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>              | ±2000 |
|                    |                         | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup> | ±1000 |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                 |                                    |                                  | SN74LV125AT |                 | UNIT |
|-----------------|------------------------------------|----------------------------------|-------------|-----------------|------|
|                 |                                    |                                  | MIN         | MAX             |      |
| V <sub>CC</sub> | Supply voltage                     |                                  | 4.5         | 5.5             | V    |
| V <sub>IH</sub> | High-level input voltage           | V <sub>CC</sub> = 4.5 V to 5.5 V | 2           |                 | V    |
| V <sub>IL</sub> | Low-level input voltage            | V <sub>CC</sub> = 4.5 V to 5.5 V |             | 0.8             | V    |
| V <sub>I</sub>  | Input voltage                      |                                  | 0           | 5.5             | V    |
| V <sub>O</sub>  | Output voltage                     | High or low state                | 0           | V <sub>CC</sub> | V    |
|                 |                                    | 3-state                          | 0           | 5.5             |      |
| I <sub>OH</sub> | High-level output current          | V <sub>CC</sub> = 4.5 V to 5.5 V |             | –16             | mA   |
| I <sub>OL</sub> | Low-level output current           | V <sub>CC</sub> = 4.5 V to 5.5 V |             | 16              | mA   |
| Δt/Δv           | Input transition rise or fall rate | V <sub>CC</sub> = 4.5 V to 5.5 V |             | 20              | ns/V |
| T <sub>A</sub>  | Operating free-air temperature     |                                  | –40         | 125             | °C   |

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

## 5.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                        | SN74LV125AT |    |    |     |     | UNIT |
|-------------------------------|----------------------------------------|-------------|----|----|-----|-----|------|
|                               |                                        | D           | DB | NS | PW  | RGY |      |
|                               |                                        | 14 PINS     |    |    |     |     |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance | 86          | 96 | 76 | 113 | 47  | °C/W |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

## 5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                                                        | TEST CONDITIONS                                             | V <sub>CC</sub> | T <sub>A</sub> = 25°C |     |       | –40°C to 85°C |      | –40°C to 125°C |      | UNIT |
|------------------------------------------------------------------|-------------------------------------------------------------|-----------------|-----------------------|-----|-------|---------------|------|----------------|------|------|
|                                                                  |                                                             |                 | MIN                   | TYP | MAX   | MIN           | MAX  | MIN            | MAX  |      |
| V <sub>OH</sub> High-level output voltage                        | I <sub>OH</sub> = –50 µA                                    | 4.5 V           | 4.4                   | 4.5 |       | 4.4           |      | 4.4            |      | V    |
|                                                                  | I <sub>OH</sub> = –16 mA                                    | 4.5 V           | 3.8                   |     |       | 3.8           |      | 3.8            |      |      |
| V <sub>OL</sub> Low-level output voltage                         | I <sub>OL</sub> = 50 µA                                     | 4.5 V           |                       | 0   | 0.1   |               | 0.1  |                | 0.1  | V    |
|                                                                  | I <sub>OL</sub> = 16 mA                                     | 4.5 V           |                       |     | 0.55  |               | 0.55 |                | 0.55 |      |
| I <sub>I</sub> Input leakage current                             | V <sub>I</sub> = 5.5 V or GND                               | 0 to 5.5 V      |                       |     | ±1    |               | ±1   |                | ±1   | µA   |
| I <sub>OZ</sub> Off-State (High-Impedance State) Output Current  | V <sub>O</sub> = V <sub>CC</sub> or GND                     | 5.5 V           |                       |     | ±0.25 |               | ±2.5 |                | ±2.5 | µA   |
| I <sub>CC</sub> Static supply current                            | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0 | 5.5 V           |                       |     | 2     |               | 20   |                | 20   | µA   |
| ΔI <sub>CC</sub> <sup>(1)</sup> Additional static supply current | One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND  | 5.5 V           |                       |     | 1.35  |               | 1.5  |                | 1.5  |      |
| I <sub>off</sub> Input/Output Power-Off Leakage Current          | V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V               | 0               |                       |     | 0.5   |               | 5    |                | 5    | µA   |
| C <sub>i</sub> Input capacitance                                 | V <sub>I</sub> = V <sub>CC</sub> or GND                     |                 |                       |     | 2     |               |      |                |      | pF   |

(1) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

## 5.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit And Voltage Waveforms](#))

| PARAMETER          | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE       | T <sub>A</sub> = 25°C |     |     | –40°C to 85°C |     | –40°C to 125°C |      | UNIT |
|--------------------|--------------|-------------|------------------------|-----------------------|-----|-----|---------------|-----|----------------|------|------|
|                    |              |             |                        | MIN                   | TYP | MAX | MIN           | MAX | MIN            | MAX  |      |
| t <sub>pd</sub>    | A            | Y           | C <sub>L</sub> = 15 pF | 1.9                   | 3.8 | 5.5 | 1             | 6.5 | 1              | 8.5  | ns   |
| t <sub>en</sub>    | OE           | Y           |                        | 2                     | 3.6 | 5.1 | 1             | 6   | 1              | 7.5  |      |
| t <sub>dis</sub>   | OE           | Y           |                        | 1.5                   | 3.2 | 6.8 | 1             | 8   | 1              | 10   |      |
| t <sub>pd</sub>    | A            | Y           | C <sub>L</sub> = 50 pF | 2.9                   | 5.3 | 7.5 | 1             | 8.5 | 1              | 10.5 | ns   |
| t <sub>en</sub>    | OE           | Y           |                        | 2.8                   | 5.1 | 7.1 | 1             | 8   | 1              | 9.5  |      |
| t <sub>dis</sub>   | OE           | Y           |                        | 2.8                   | 6.1 | 8.8 | 1             | 10  | 1              | 10   |      |
| t <sub>sk(o)</sub> |              |             |                        |                       |     | 1   |               | 1   |                | 1    |      |

## 5.7 Noise Characteristics

V<sub>CC</sub> = 5 V, C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C

| PARAMETER <sup>(1)</sup> |                                               | SN74LV125AT |      |      | UNIT |
|--------------------------|-----------------------------------------------|-------------|------|------|------|
|                          |                                               | MIN         | TYP  | MAX  |      |
| V <sub>OL(P)</sub>       | Quiet output, maximum dynamic V <sub>OL</sub> |             | 1.1  | 1.5  | V    |
| V <sub>OL(V)</sub>       | Quiet output, minimum dynamic V <sub>OL</sub> |             | –0.3 | –0.8 | V    |
| V <sub>OH(V)</sub>       | Quiet output, minimum dynamic V <sub>OH</sub> |             | 3    |      | V    |
| V <sub>IH(D)</sub>       | High-level dynamic input voltage              | 2           |      |      | V    |
| V <sub>IL(D)</sub>       | Low-level dynamic input voltage               |             |      | 0.8  | V    |

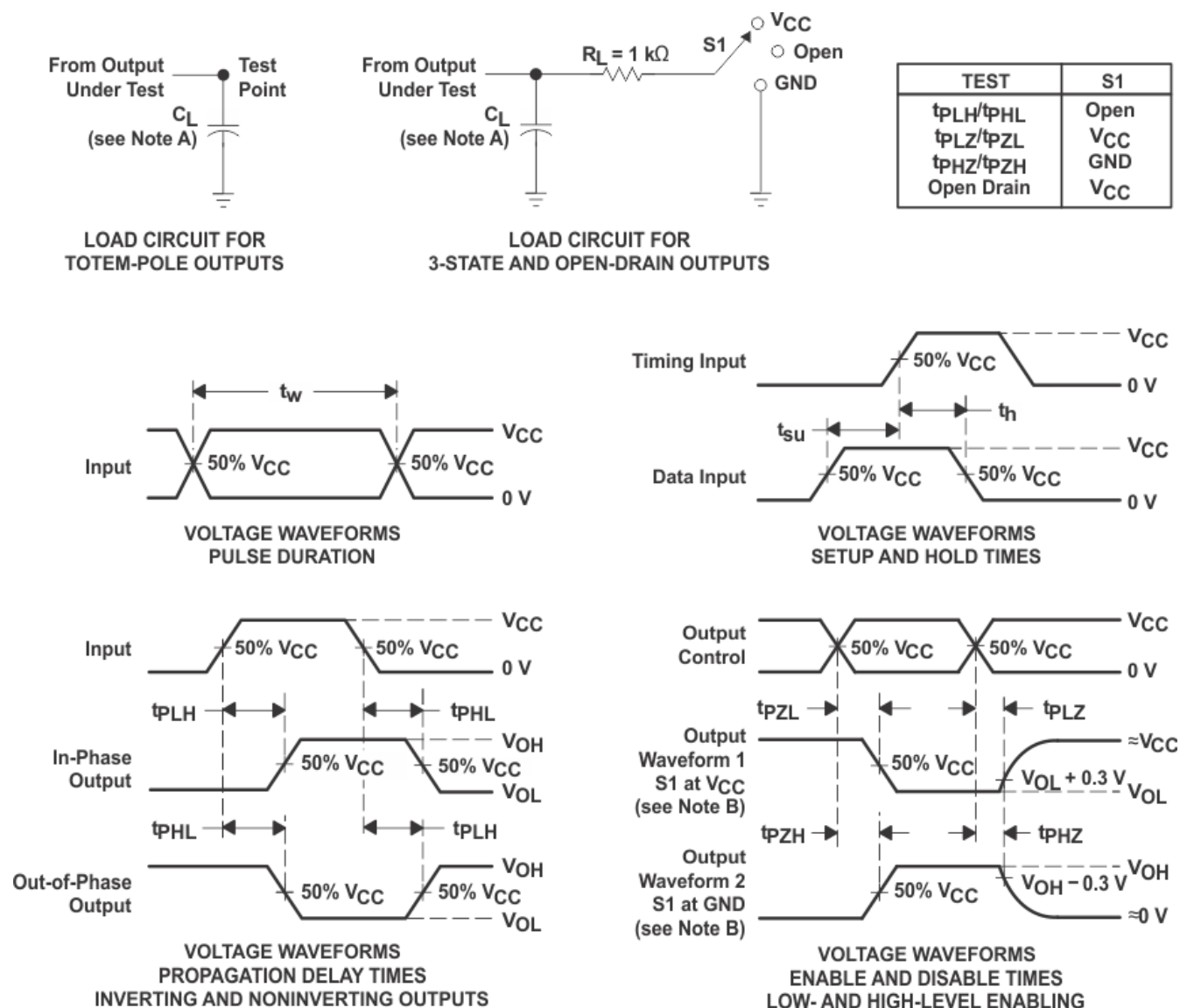
(1) Characteristics are for surface-mount packages only.

## 5.8 Operating Characteristics

$V_{CC} = 5\text{ V}$ ,  $T_A = -25^\circ\text{C}$

| PARAMETER |                               |                 | TEST CONDITIONS                               | TYP | UNIT |
|-----------|-------------------------------|-----------------|-----------------------------------------------|-----|------|
| $C_{pd}$  | Power dissipation capacitance | Outputs enabled | $C_L = 50\text{ pF}$ ,<br>$f = 10\text{ MHz}$ | 16  | pF   |

## 6 Parameter Measurement Information



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
  - D. The outputs are measured one at a time, with one input transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .
  - H. All parameters and waveforms are not applicable to all devices.

**6-1. Load Circuit And Voltage Waveforms**

## 7 Detailed Description

### 7.1 Overview

The SN74LV125AT is a quadruple bus buffer gate. This device features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable ( $\overline{OE}$ ) input is high.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

### 7.2 Functional Block Diagram

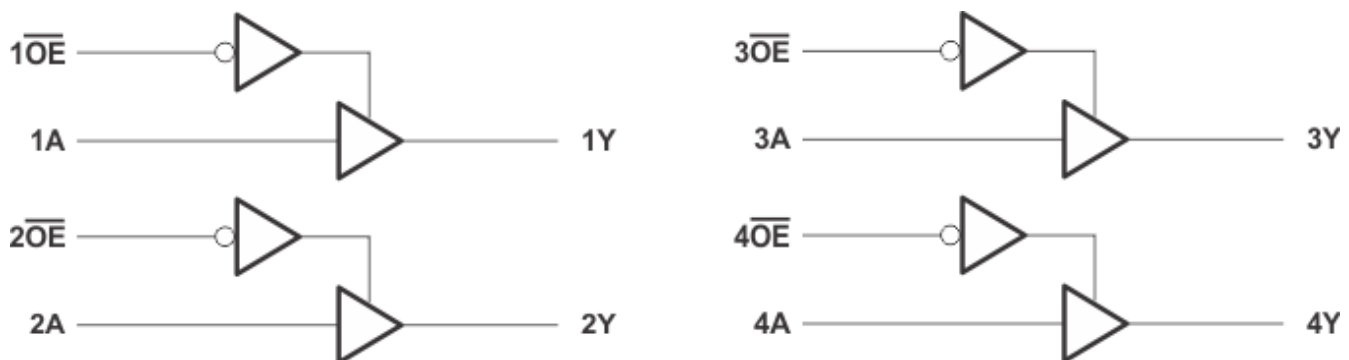


图 7-1. Logic Diagram (Positive Logic)

### 7.3 Device Functional Modes

表 7-1. Function Table  
(Each Buffer)

| INPUTS <sup>(1)</sup> |   | OUTPUT <sup>(2)</sup> |
|-----------------------|---|-----------------------|
| $\overline{OE}$       | A | Y                     |
| L                     | H | H                     |
| L                     | L | L                     |
| H                     | X | Z                     |

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

(2) H = Driving High, L = Driving Low, Z = High Impedance State

## 8 Device and Documentation Support

### 8.1 Documentation Support

#### 8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 8-1. Related Links

| PARTS       | PRODUCT FOLDER             | SAMPLE & BUY               | TECHNICAL DOCUMENTS        | TOOLS & SOFTWARE           | SUPPORT & COMMUNITY        |
|-------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| SN74LV125AT | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

#### 8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](http://ti.com) のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

#### 8.3 サポート・リソース

**TI E2E™ サポート・フォーラム**は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の[使用条件](#)を参照してください。

#### 8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

#### 8.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

#### 8.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74LV125ATDBR   | ACTIVE        | SSOP         | DB              | 14   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | LV125AT                 | <a href="#">Samples</a> |
| SN74LV125ATDR    | ACTIVE        | SOIC         | D               | 14   | 2500        | RoHS & Green    | NIPDAU   SN                          | Level-1-260C-UNLIM   | -40 to 85    | LV125AT                 | <a href="#">Samples</a> |
| SN74LV125ATNSR   | ACTIVE        | SO           | NS              | 14   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | LV125AT                 | <a href="#">Samples</a> |
| SN74LV125ATPWR   | ACTIVE        | TSSOP        | PW              | 14   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | LV125AT                 | <a href="#">Samples</a> |
| SN74LV125ATRGYR  | ACTIVE        | VQFN         | RGY             | 14   | 3000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | VV125                   | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LV125ATDBR  | SSOP         | DB              | 14   | 2000 | 330.0              | 16.4               | 8.35    | 6.6     | 2.4     | 12.0    | 16.0   | Q1            |
| SN74LV125ATDR   | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74LV125ATDR   | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.6     | 9.3     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74LV125ATDR   | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74LV125ATNSR  | SO           | NS              | 14   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |
| SN74LV125ATPWR  | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LV125ATRGYR | VQFN         | RGY             | 14   | 3000 | 330.0              | 12.4               | 3.75    | 3.75    | 1.15    | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS

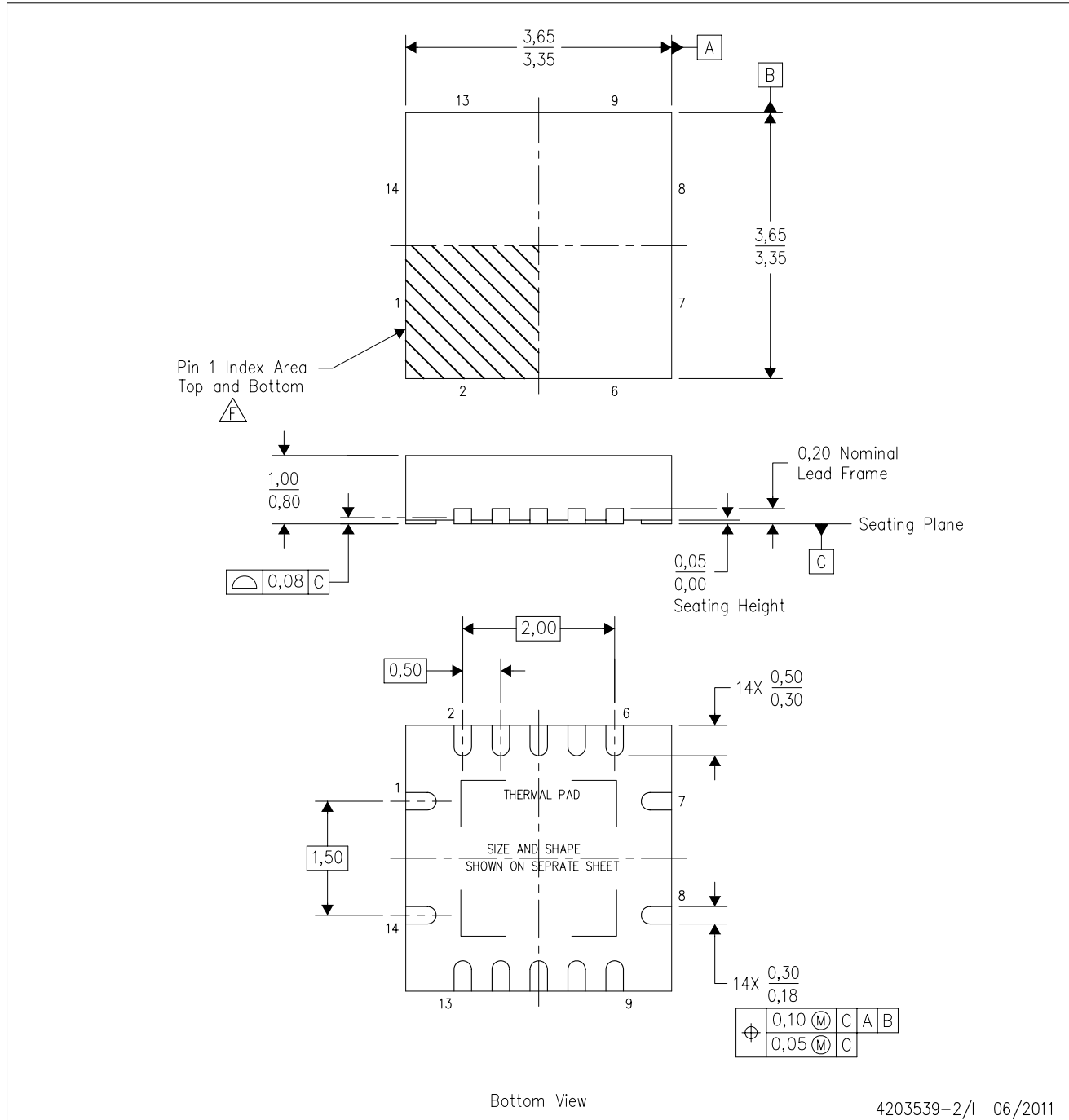


\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LV125ATDBR  | SSOP         | DB              | 14   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74LV125ATDR   | SOIC         | D               | 14   | 2500 | 356.0       | 356.0      | 35.0        |
| SN74LV125ATDR   | SOIC         | D               | 14   | 2500 | 366.0       | 364.0      | 50.0        |
| SN74LV125ATDR   | SOIC         | D               | 14   | 2500 | 356.0       | 356.0      | 35.0        |
| SN74LV125ATNSR  | SO           | NS              | 14   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74LV125ATPWR  | TSSOP        | PW              | 14   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74LV125ATRGYR | VQFN         | RGY             | 14   | 3000 | 360.0       | 360.0      | 36.0        |

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



4203539-2/I 06/2011

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - QFN (Quad Flatpack No-Lead) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - Package complies to JEDEC MO-241 variation BA.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
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