

## SN74AHC245-Q1 車載対応、3 ステート出力オクタール・バス・トランシーバ

### 1 特長

- 車載アプリケーション用に AEC-Q100 認定済み :
  - デバイス温度グレード 1 : -40°C ~ +125°C、 $T_A$
  - デバイス HBM ESD 分類レベル 2
  - デバイス CDM ESD 分類レベル C6
- 2V ~ 5.5V の  $V_{CC}$  で動作
- JESD 17 準拠で 250mA 超のラッチアップ性能

### 2 アプリケーション

- デジタル信号のイネーブルまたはディセーブル
- コントローラ・リセット時の信号保持
- スイッチのデバウンス

### 3 概要

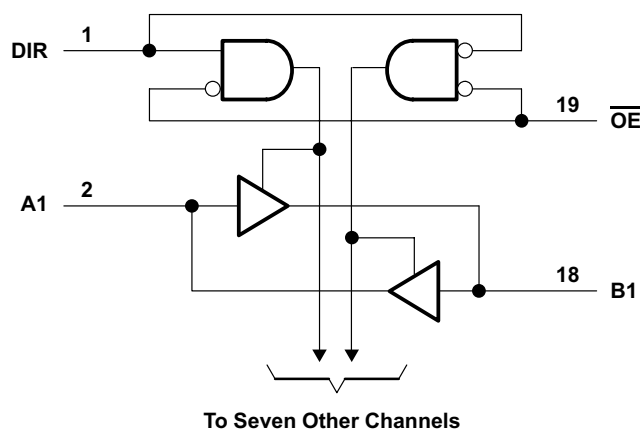
SN74AHC245-Q1 オクタール・バス・トランシーバは、データ・バス間の非同期双方向通信用に設計されています。制御機能を実装することで、外部のタイミング要件を最小化しています。このデバイスを使うと、方向制御 (DIR) 入力の論理レベルに応じて、A バスから B バス、または B バスから A バスへデータを転送できます。出力イネーブル ( $\overline{OE}$ ) 入力を使うと、本デバイスを無効化してバスを実質的に絶縁できます。

電源オンまたは電源オフ時に高インピーダンス状態を確保するため、 $\overline{OE}$  はプルアップ抵抗経由で  $V_{CC}$  に接続されます。この抵抗の最小値は、ドライバの電流シンク能力によって決定されます。

#### パッケージ情報<sup>(1)</sup>

部品番号	パッケージ	本体サイズ (公称)
SN74AHC245-Q1	PW (TSSOP, 20)	6.50mm × 4.40mm
	WRKS (WQFN, 20)	4.50mm × 2.50mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



簡略回路図



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## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

<b>Changes from Revision C (February 2023) to Revision D (June 2023)</b>	<b>Page</b>
• Updated RθJA values: PW = 83 to 122.3, all values in °C/W.....	<b>5</b>
<b>Changes from Revision B (November 2022) to Revision C (February 2023)</b>	<b>Page</b>
• データシートのステータスを「事前情報」から：「量産データ」に変更.....	<b>1</b>

## 5 Pin Configuration and Functions

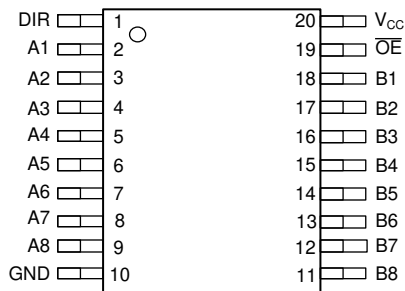


図 5-1. SN74AHC245-Q1 PW Package, 20-Pin TSSOP (Top View)

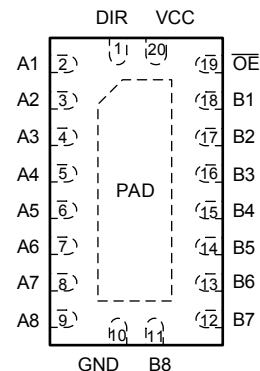


図 5-2. SN74AHC245-Q1 WRKS Package, 20-Pin WQFN (Top View)

表 5-1. Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NO.	NAME		
1	DIR	I/O	Direction control input (L = B → A, H = A → B)
2	A1	I/O	Channel 1 output/input A
3	A2	I/O	Channel 2 output/input A
4	A3	I/O	Channel 3 output/input A
5	A4	I/O	Channel 4 output/input A
6	A5	I/O	Channel 5 output/input A
7	A6	I/O	Channel 6 output/input A
8	A7	I/O	Channel 7 output/input A
9	A8	I/O	Channel 8 output/input A
10	GND	G	Ground
11	B8	I/O	Channel 8 input/output B
12	B7	I/O	Channel 7 input/output B
13	B6	I/O	Channel 6 input/output B
14	B5	I/O	Channel 5 input/output B
15	B4	I/O	Channel 4 input/output B
16	B3	I/O	Channel 3 input/output B
17	B2	I/O	Channel 2 input/output B
18	B1	I/O	Channel 1 input/output B
19	OE	I/O	Output enable, active low
20	V <sub>CC</sub>	P	Positive supply
Thermal Pad		—	Thermal Pad <sup>(2)</sup>

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

(2) WRKS Package Only

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage range		−0.5	7	V
$V_I$	Input voltage range <sup>(2)</sup>	Control inputs	−0.5	7	V
$V_O$	I/O, Output voltage range		−0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$ Control inputs		−20	mA
$I_{OK}$	I/O, Output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
$I_O$	Continuous output current	$V_O = 0$ to $V_{CC}$		±25	mA
	Continuous current through $V_{CC}$ or GND			±75	mA

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

### 6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2 <sup>(1)</sup>	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C6	±1000	

- (1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage		2	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V	1.5		V
		$V_{CC} = 3$ V	2.1		
		$V_{CC} = 5.5$ V	3.85		
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V		0.5	V
		$V_{CC} = 3$ V		0.9	
		$V_{CC} = 5.5$ V		1.65	
$V_I$	Input voltage	OE or DIR	0	5.5	V
$V_O$	Output voltage	A or B	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2$ V		−50	μA
		$V_{CC} = 3.3$ V ± 0.3 V		−4	mA
		$V_{CC} = 5$ V ± 0.5 V		−8	
$I_{OL}$	Low-level output current	$V_{CC} = 2$ V		50	μA
		$V_{CC} = 3.3$ V ± 0.3 V		4	mA
		$V_{CC} = 5$ V ± 0.5 V		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3$ V ± 0.3 V		100	ns/V
		$V_{CC} = 5$ V ± 0.5 V		20	
$T_A$	Operating free-air temperature		−40	125	°C

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*.

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		PW	RKS	UNIT
		20 PINS	20 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	122.3	67.7	°C/W

(1) For more information about traditional and new thermal metrics, see the [IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
V <sub>OH</sub>		I <sub>OH</sub> = -50 μA	2 V	1.9	2		1.9		V
			3 V	2.9	3		2.9		
			4.5 V	4.4	4.5		4.4		
		I <sub>OH</sub> = -4 mA	3 V	2.58			2.48		
			4.5 V	3.94			3.8		
V <sub>OL</sub>		I <sub>OL</sub> = 50 μA	2 V			0.1		0.1	V
			3 V			0.1		0.1	
			4.5 V			0.1		0.1	
		I <sub>OL</sub> = 4 mA	3 V			0.36		0.44	
			4.5 V			0.36		0.44	
I <sub>I</sub>	A or B inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			±0.1		±1	μA
	$\overline{\text{OE}}$ or DIR		0 V to 5.5 V			±0.1		±1	
I <sub>OZ</sub> <sup>(1)</sup>		V <sub>O</sub> = V <sub>CC</sub> or GND, V <sub>I</sub> ( $\overline{\text{OE}}$ ) = V <sub>IL</sub> or V <sub>IH</sub>	5.5 V			±0.25		±2.5	μA
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			4		40	μA
C <sub>i</sub>	$\overline{\text{OE}}$ or DIR	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		2.5	10		10	pF
C <sub>io</sub>	A or B inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		4				pF

(1) The parameter I<sub>OZ</sub> includes the input leakage current.

## 6.6 Switching Characteristics, V<sub>CC</sub> = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see [FIG 7-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t <sub>PLH</sub>	A or B	B or A	C <sub>L</sub> = 15 pF		5.8	8.4	1	10	ns
t <sub>PHL</sub>					5.8	8.4	1	10	
t <sub>PZH</sub>	$\overline{\text{OE}}$	A or B	C <sub>L</sub> = 15 pF		8.5	13.2	1	15.5	ns
t <sub>PZL</sub>					8.5	13.2	1	15.5	
t <sub>PHZ</sub>	$\overline{\text{OE}}$	A or B	C <sub>L</sub> = 15 pF		8.9	12.5	1	15.5	ns
t <sub>PLZ</sub>					8.9	12.5	1	15.5	
t <sub>PLH</sub>	A or B	B or A	C <sub>L</sub> = 50 pF		8.3	11.9	1	13.5	ns
t <sub>PHL</sub>					8.3	11.9	1	13.5	
t <sub>PZH</sub>	$\overline{\text{OE}}$	A or B	C <sub>L</sub> = 50 pF		11	16.7	1	19	ns
t <sub>PZL</sub>					11	16.7	1	19	
t <sub>PHZ</sub>	$\overline{\text{OE}}$	A or B	C <sub>L</sub> = 50 pF		11.5	15.8	1	18	ns
t <sub>PLZ</sub>					11.5	15.8	1	18	

## 6.7 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 7-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } 125^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{PLH}$	A or B	B or A	$C_L = 15\text{ pF}$		4	5.5	1	6.5	ns
$t_{PHL}$					4	5.5	1	6.5	
$t_{PZH}$	$\overline{OE}$	A or B	$C_L = 15\text{ pF}$		5.8	8.5	1	10	ns
$t_{PZL}$					5.8	8.5	1	10	
$t_{PHZ}$	$\overline{OE}$	A or B	$C_L = 15\text{ pF}$		5.6	7.8	1	9.2	ns
$t_{PLZ}$					5.6	7.8	1	9.2	
$t_{PLH}$	A or B	B or A	$C_L = 50\text{ pF}$		5.5	7.5	1	8.5	ns
$t_{PHL}$					5.5	7.5	1	8.5	
$t_{PZH}$	$\overline{OE}$	A or B	$C_L = 50\text{ pF}$		7.3	10.6	1	12	ns
$t_{PZL}$					7.3	10.6	1	12	
$t_{PHZ}$	$\overline{OE}$	A or B	$C_L = 50\text{ pF}$		7	9.7	1	11	ns
$t_{PLZ}$					7	9.7	1	11	

## 6.8 Noise Characteristics

$V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  <sup>(1)</sup>

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.9		V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		-0.9		V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$		4.3		V
$V_{IH(D)}$	High-level dynamic input voltage		3.5		V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

(1) Characteristics are for surface-mount packages only.

## 6.9 Operating Characteristics

$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		TYP	UNIT
$C_{pd}$	Power dissipation capacitance	No load	$f = 1\text{ MHz}$	14	pF

## 6.10 Typical Characteristics

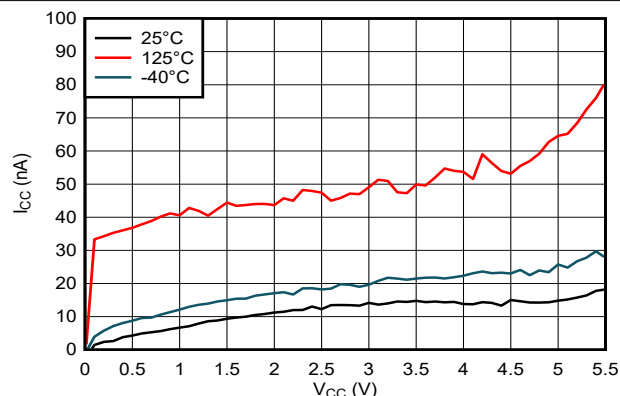


图 6-1. Supply Current Across Voltage Supply Voltage

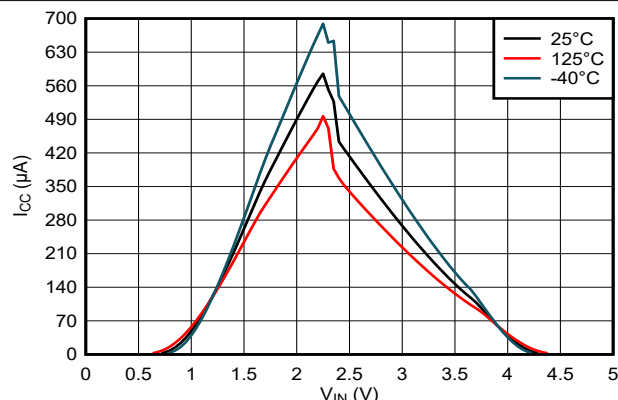


图 6-2. Supply Current Across Input Voltage; 5-V Supply

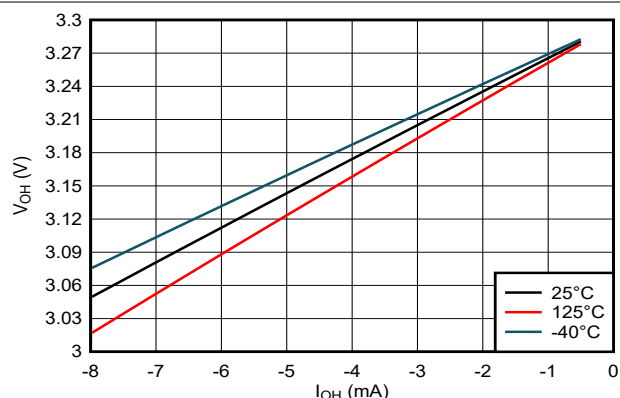


图 6-3. Output Voltage vs Current in HIGH State; 3.3-V Supply

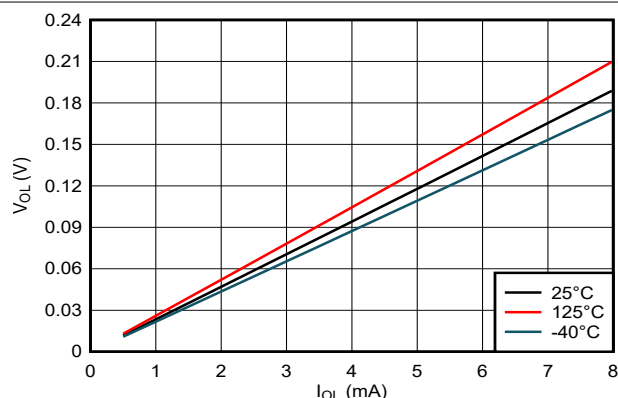


图 6-4. Output Voltage vs Current in LOW State; 3.3-V Supply

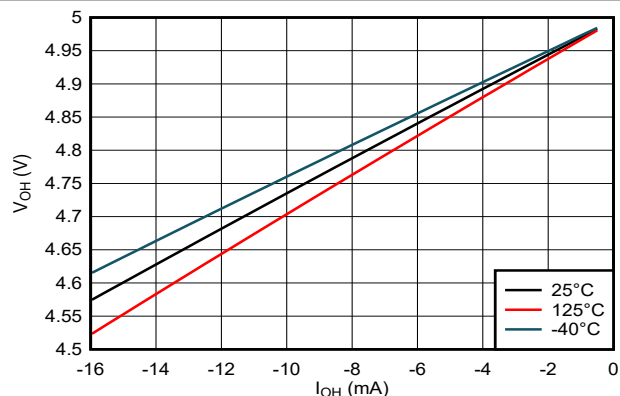


图 6-5. Output Voltage vs Current in HIGH State; 5-V Supply

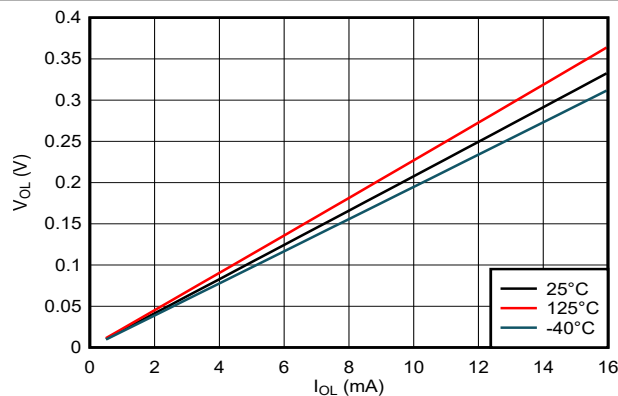
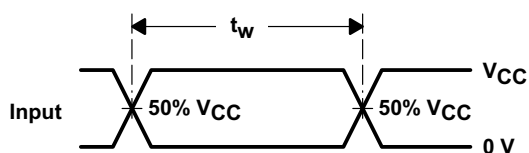
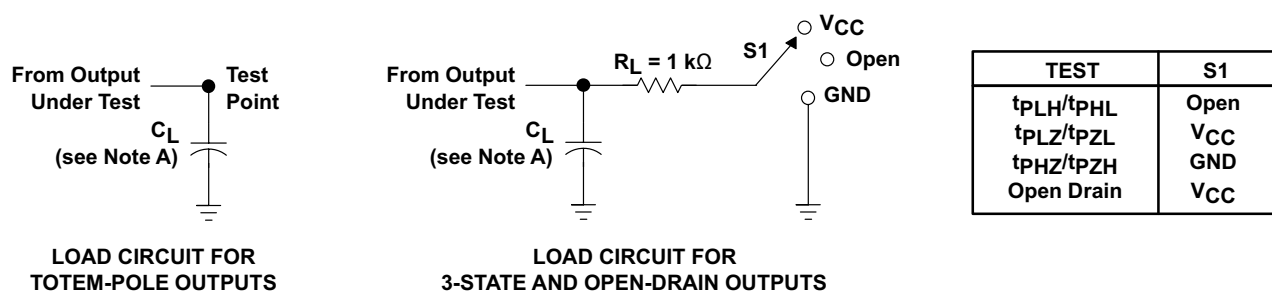
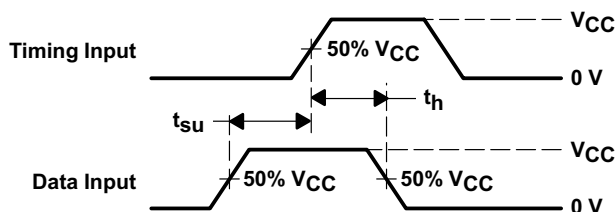


图 6-6. Output Voltage vs Current in LOW State; 5-V Supply

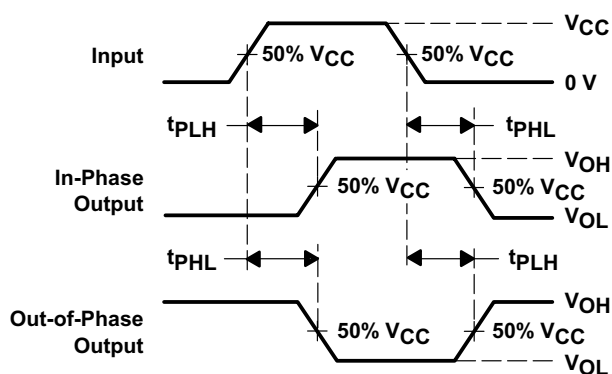
## 7 Parameter Measurement Information



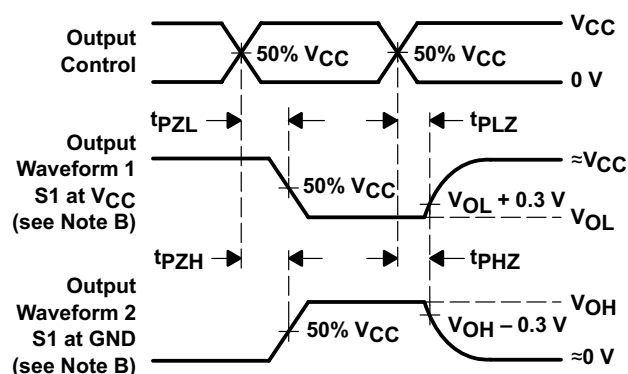
**VOLTAGE WAVEFORMS  
PULSE DURATION**



**VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 3$  ns,  $t_f \leq 3$  ns.  
 D. The outputs are measured one at a time with one input transition per measurement.  
 E. All parameters and waveforms are not applicable to all devices.

**7-1. Load Circuit and Voltage Waveforms**

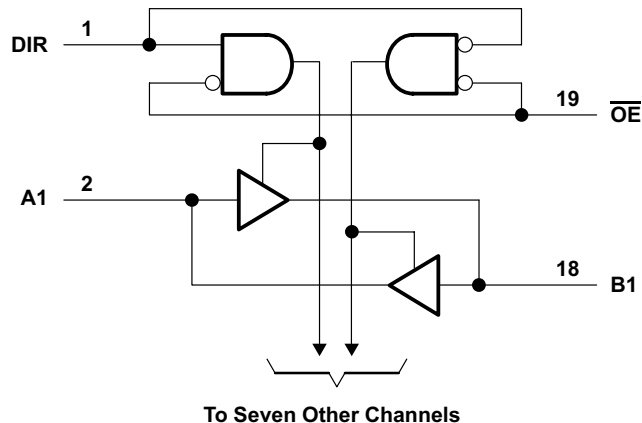


## 8 Detailed Description

### 8.1 Overview

The SN74AHC245-Q1 is designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements. The SN74AHC245-Q1 allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so that the buses are effectively isolated. To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law ( $R = V \div I$ ).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in [Implications of Slow or Floating CMOS Inputs](#).

Do not leave standard CMOS inputs floating at any time during operation. Unused inputs must be terminated at  $V_{CC}$  or GND. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; a 10-k $\Omega$  resistor, however, is recommended and will typically meet all requirements.

#### 8.3.2 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs. Driving high, driving low, and high impedance are the three states that these outputs can be in. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device can drive larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance mode, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor

can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10-k $\Omega$  resistor can be used to meet these requirements.

Unused 3-state CMOS outputs should be left disconnected.

### 8.3.3 Wettable Flanks

This device includes wettable flanks for at least one package. See the *Features* section on the front page of the data sheet for which packages include this feature.

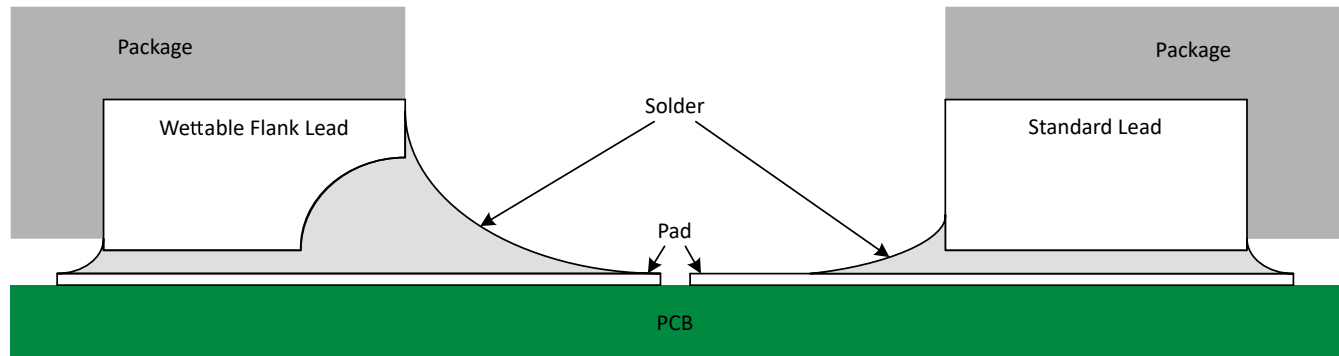


图 8-1. Simplified Cutaway View of Wettable-Flank QFN Package and Standard QFN Package After Soldering

Wettable flanks help improve side wetting after soldering, which makes QFN packages easier to inspect with automatic optical inspection (AOI). As shown in 图 8-1, a wettable flank can be dimpled or step-cut to provide additional surface area for solder adhesion which assists in reliably creating a side fillet. See the mechanical drawing for additional details.

### 8.3.4 Clamp Diode Structure

As 图 8-2 shows, the outputs to this device have both positive and negative clamping diodes, and the inputs to this device have negative clamping diodes only.

**注意**

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

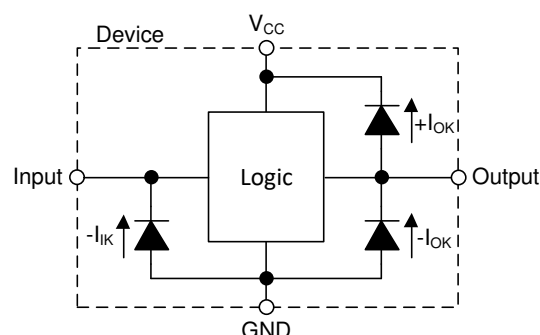


图 8-2. Electrical Placement of Clamping Diodes for Each Input and Output

## 8.4 Device Functional Modes

表 8-1 lists the functional modes of the SN74AHC245-Q1.

**表 8-1. Function Table**

INPUTS <sup>(1)</sup>		OUTPUTS <sup>(2)</sup>	
$\overline{OE}$	DIR	A	B
L	L	B	Z
L	H	Z	A
H	X	Z	Z

(1) H = High voltage level, L = Low voltage level, X = Do not care

(2) A = Logic value at 'A' input, B = Logic value at 'B' input, Z = High impedance

## 9 Application and Implementation

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

The SN74AHC245-Q1 can be used to drive signals over relatively long traces or transmission lines. In order to reduce ringing caused by impedance mismatches between the driver, transmission line, and receiver, a series damping resistor placed in series with the transmitter's output can be used. The figure in the *Application Curve* section shows the received signal with three separate resistor values. Just a small amount of resistance can make a significant impact on signal integrity in this type of application.

### 9.2 Typical Application

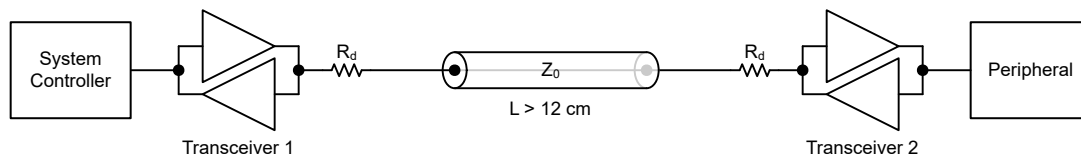


图 9-1. Application Block Diagram

#### 9.2.1 Design Requirements

##### 9.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74AHC245-Q1 plus the maximum static supply current,  $I_{CC}$ , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Be sure to not exceed the maximum total current through  $V_{CC}$  listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74AHC245-Q1 plus the maximum supply current,  $I_{CC}$ , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Be sure to not exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74AHC245-Q1 can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50 pF.

The SN74AHC245-Q1 can drive a load with total resistance described by  $R_L \geq V_O / I_O$ , with the output voltage and current defined in the *Electrical Characteristics* table with  $V_{OH}$  and  $V_{OL}$ . When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the  $V_{CC}$  pin.

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and Cpd Calculation](#).

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

**注意**

The maximum junction temperature,  $T_{J(max)}$  listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

### 9.2.1.2 Input Considerations

Input signals must cross  $V_{IL(max)}$  to be considered a logic LOW, and  $V_{IH(min)}$  to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either  $V_{CC}$  or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74AHC245-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10-k $\Omega$  resistor value is often used due to these factors.

The SN74AHC245-Q1 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

### 9.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the  $V_{OH}$  specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the  $V_{OL}$  specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to  $V_{CC}$  or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

### 9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from  $V_{CC}$  to GND. The capacitor needs to be placed physically close to the device and electrically close to both the  $V_{CC}$  and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is  $\leq 50$  pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74AHC245-Q1 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than  $(V_{CC} / I_{O(max)}) \Omega$ . Doing this will prevent the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in  $M\Omega$ ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#).

### 9.2.3 Application Curves

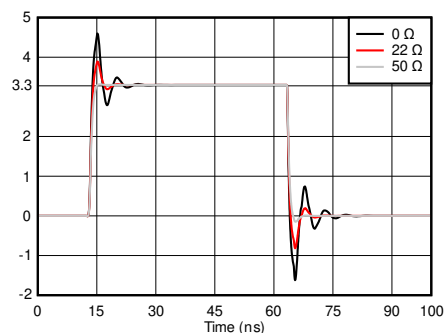


FIG 9-2. Simulated Signal Integrity at the Receiver With Different Damping Resistor ( $R_d$ ) Values

## 9.3 Power Supply Recommendations

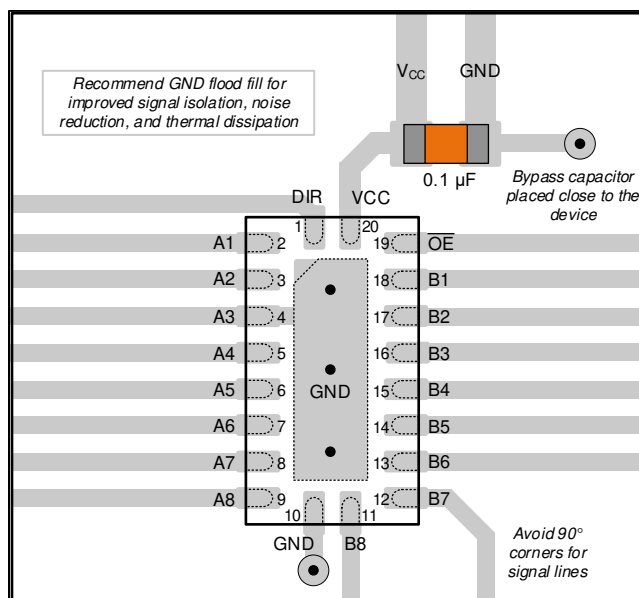
The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Absolute Maximum Ratings* section. Each  $V_{CC}$  terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1- $\mu$ F capacitor; if there are multiple  $V_{CC}$  terminals, then TI recommends a 0.01- $\mu$ F or 0.022- $\mu$ F capacitor for each power terminal. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. Frequencies of 0.1  $\mu$ F and 1  $\mu$ F are commonly used in parallel. The bypass capacitor must be installed as close as possible to the power terminal for best results.

## 9.4 Layout

### 9.4.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

### 9.4.2 Layout Example



✎ 9-3. Example Layout for the SN74AHC245-Q1 in the RKS Package

## 10 Device and Documentation Support

### 10.1 ドキュメントの更新通知を受け取る方法

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 10.5 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHC245QPWRG4Q1	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC245Q1	<a href="#">Samples</a>
SN74AHC245QPWRQ1	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC245Q1	<a href="#">Samples</a>
SN74AHC245QWRKSRQ1	ACTIVE	VQFN	RKS	20	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA245Q	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN74AHC245-Q1 :**

- Catalog : [SN74AHC245](#)
- Enhanced Product : [SN74AHC245-EP](#)
- Military : [SN54AHC245](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC245QPWRG4Q1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74AHC245QPWRQ1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74AHC245QPWRQ1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74AHC245QWRKSRQ1	VQFN	RKS	20	3000	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC245QPWRG4Q1	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74AHC245QPWRQ1	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74AHC245QPWRQ1	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74AHC245QWRKSRQ1	VQFN	RKS	20	3000	210.0	185.0	35.0

## GENERIC PACKAGE VIEW

**RKS 20**

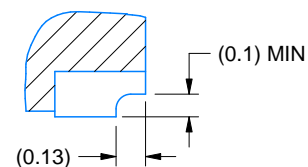
**VQFN - 1 mm max height**

2.5 x 4.5, 0.5 mm pitch

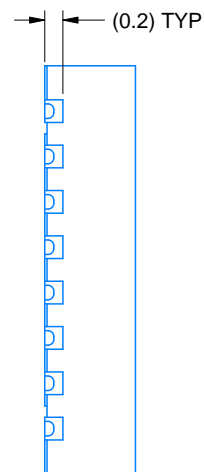
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.





The drawing shows a 12-pin connector assembly. The top view (left) shows a rectangular footprint with dimensions 10 by 11. It features 12 pins arranged in two rows of six. Dimensions include 1.05, 0.95, 1.0, 0.8, 0.05, 0.00, 14X 0.5, 2X 3.5, 9, 10, 11, 12, 3.05, 2.95, 2, 19, 20X 0.45, 0.35, 20X 0.3, 0.2, and 20X 0.1. Callouts include 'PIN 1 ID (OPTIONAL)', 'EXPOSED THERMAL PAD', and 'SEATING PLANE'. The side view (right) shows the profile of the connector with dimensions 1.0, 0.8, 0.05, 0.00, and 0.08. It includes a callout 'C' and a circular feature with a diameter of 0.08.



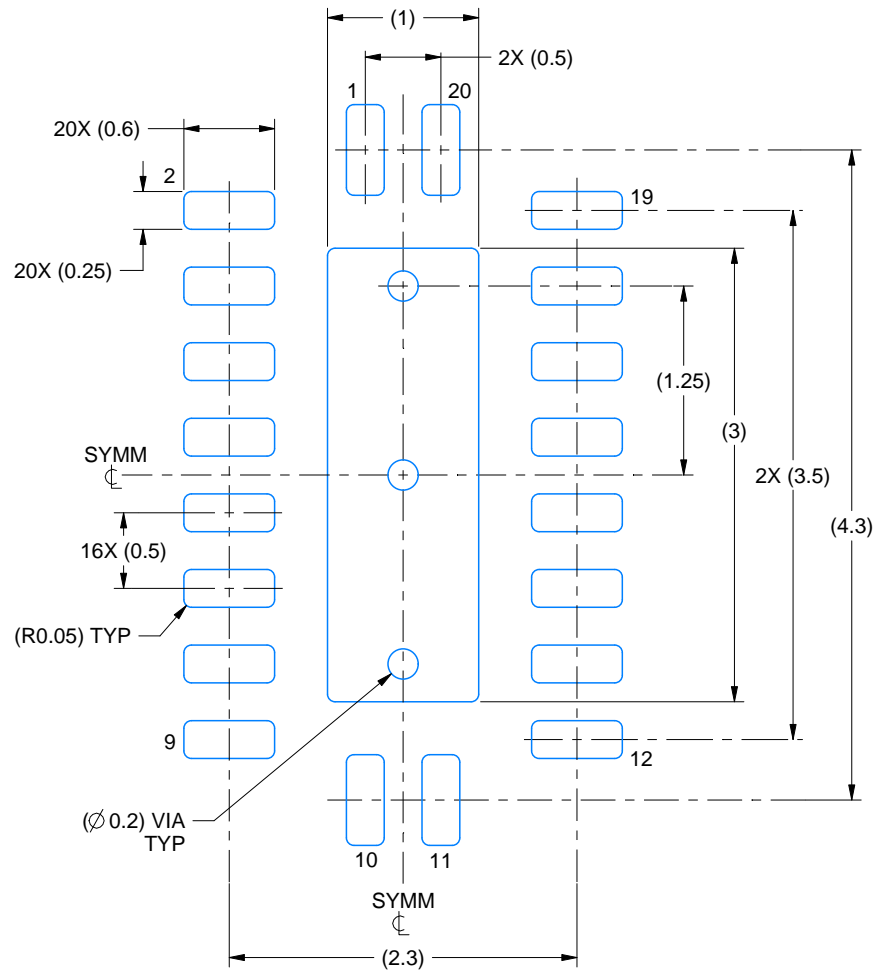
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

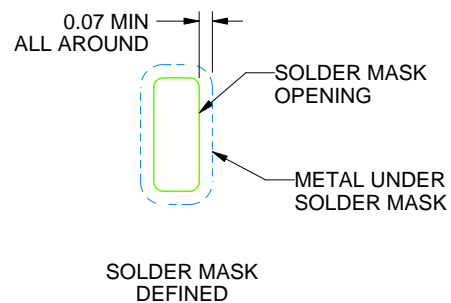
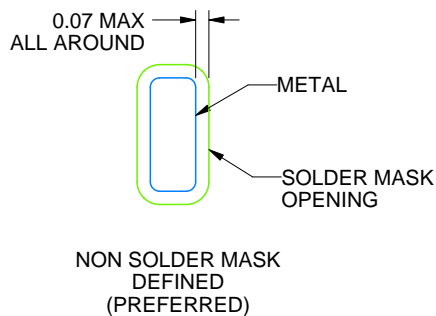
RKS0020B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:20X



SOLDER MASK DETAILS

4226762/B 06/2022

NOTES: (continued)

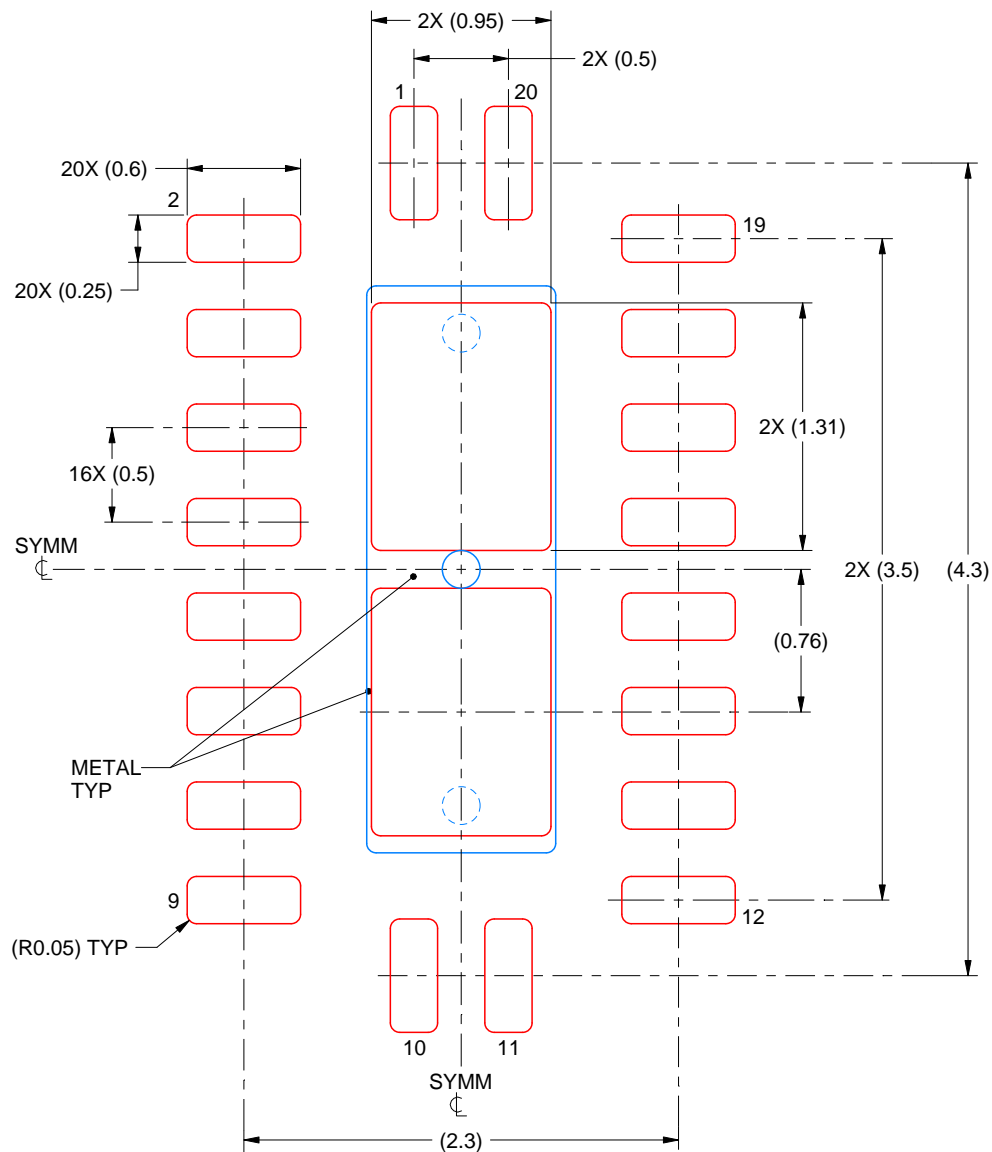
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

# EXAMPLE STENCIL DESIGN

RKS0020B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
83% PRINTED SOLDER COVERAGE BY AREA  
SCALE:25X

4226762/B 06/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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