OPA928 36V 対応、フェムトアンペア入力バイアス、高精度、レール ツー レール I/O、e-trim™ オペアンプ

1 特長

- 超低入力バイアス電流:
  - 25℃、V_S = 16V で 20fA (テスト時の最大値)
  - 85℃、V_S = 16V で 20fA (テスト時の最大値)
  - 85℃、V_S = 36V で 75fA (テスト時の最大値)
- 超低ノイズ:
  - 0.1Hz で 0.07fA/√Hz
  - 1kHz で 15nV/√Hz
- 高い DC 精度:
  - ±5μV の入力オフセット電圧
  - ±0.1μV/℃のオフセット電圧ドリフト
- 高精度ガード バッファを内蔵
- 広い帯域幅:2.5MHz GBW
- 低い静止電流:275μA
- 広い電源範囲:±2.25V～±18V (4.5V～36V)
- レール ツー レール入出力
- 動作温度範囲:-40℃～+125℃
- 低リーケージのピン配置を採用した業界標準の SOIC パッケージ

2 アプリケーション

- 電気化学メーター、pH メーター
- 実験室およびフィールド用計測機器
- 質量分光器
- イオン クロマトグラフィー (IC) 装置
- 分光光度計
- 電位計
- クーロン カウント

3 概要

OPA928 は、新世代の 36V、フェムトアンペア入力バイアスの e-trim™ オペアンプです。このデバイスは、-40℃～+85℃ の産業用温度範囲全体にわたって 20fA (最大値) の超低入力バイアス電流を実現します。OPA928 の入力バイアス性能は、両方の温度で製造時にテストされています。

入力バイアスがゼロに近いほか、レール ツー レール入出力、低いオフセット電圧 (代表値 ±5μV)、低いオフセット ドリフト (代表値 ±0.1μV/℃)、超低電流ノイズ (0.1Hz で 0.07fA/√Hz) など、優れた DC 精度と AC 性能を備えています。これらの特長から、OPA928 は低光フォトダイオードおよび高ソース インピーダンスのアプリケーションに最適です。

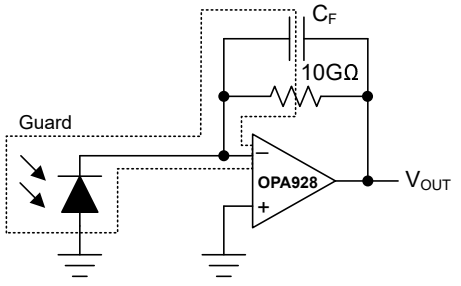
OPA928 には高精度のガード バッファが内蔵されており、高インピーダンスの入力パターンを、感受性が高いアプリケーションでの望ましくない電流リークから保護します。OPA928 のパッケージとピン配置は、低リークの回路設計をサポートするように設計されています。

OPA928 は次世代 OPA128 です。

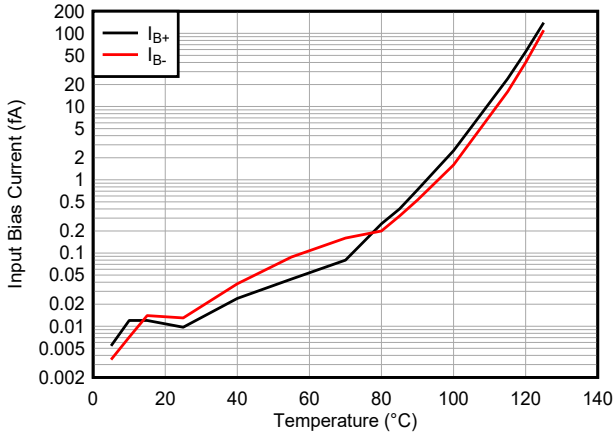
パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
OPA928	D (SOIC、8)	4.9mm × 6mm

(1) 詳細については、セクション 10 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



高ゲイン トランスインピーダンス アンプ



入力バイアス電流と温度との関係
(V_S = 16V、V_{CM} = 中電力)、RH = 10%

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4 Pin Configuration and Functions

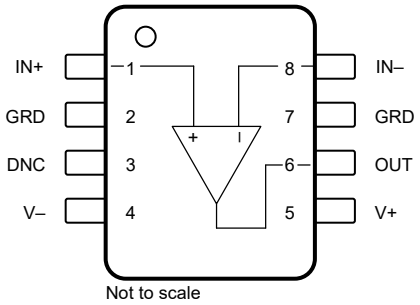


図 4-1. D Package, 8-Pin SOIC (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
GRD	2, 7	—	Guard buffer
IN+	1	Input	Noninverting input
IN–	8	Input	Inverting input
DNC	3	—	Do not connect, leave floating
OUT	6	Output	Output
V+	5	Power	Positive (highest) power supply
V–	4	Power	Negative (lowest) power supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage	Dual supply		±20	V
		Single supply		40	
	Signal input pin voltage	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential(2)		±0.5	
	Signal input pin current			±10	mA
	Guard pin to signal input pin voltage			±0.5	V
I_{SC}	Output short circuit(3)		Continuous		
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input pins are diode-clamped to the power-supply rails. Current limit input signals that can swing more than 0.5V beyond the supply rails to 10mA or less.
(3) Short-circuit to ground.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	Dual supply	±2.25		±18	V
		Single supply	4.5		36	
T_A	Ambient temperature		–40		125	°C

5.4 Thermal Information

THERMAL METRIC(1)		OPA928 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	113.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	51.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	58.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	57.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	°C/W

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics: 4.5V ≤ V_S < 8V

at T_A = 25°C, 4.5V ≤ V_S < 8V, V_{GRD} = V_{CM} = (V+) – 3V, V_{OUT} = V_S / 2, and R_L = 10kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT BIAS CURRENT							
I_B	Input bias current	RH < 50%(1)			±1	±20	fA
			T_A = –40°C to +85°C			±20	
I_{OS}	Input offset current	RH < 50% (1) (2)			±1	±20	fA
			T_A = –40°C to +85°C			±20	
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±5	±25	µV
		T_A = –40°C to +125°C			±20	±105	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C			±0.1	±0.8	µV/°C
PSRR	Power-supply rejection ratio	4.5V < V_S < 36V, V_{CM} = V_S / 2 – 0.75V	T_A = –40°C to +125°C		±0.3	±1.0	µV/V
NOISE							
	Input voltage noise	(V–) – 0.1V < V_{CM} < (V+) – 3V	f = 0.1Hz to 10Hz		1.4		$µV_{PP}$
e_n	Input voltage noise density	(V–) – 0.1V < V_{CM} < (V+) – 3V	f = 100Hz		18		nV/√Hz
			f = 1kHz		15		
i_n	Input current noise density	f = 0.1Hz			0.07		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage			(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	(V–) – 0.1V < V_{CM} < (V+) – 3V		96	120		dB
			T_A = –40°C to +125°C	90	104		
		(V+) – 3V < V_{CM} < (V+) + 0.1V		See *Typical Characteristics*			
INPUT IMPEDANCE							
Z_{ID}	Differential				750 || 3		GΩ || pF
Z_{IC}	Common-mode				1000 || 6		TΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 0.6V < V_O < (V+) – 0.6V, R_L = 2kΩ		110	120		dB
			T_A = –40°C to +125°C	100	114		
		(V–) + 0.3V < V_O < (V+) – 0.3V, R_L = 10kΩ		110	126		
			T_A = –40°C to +125°C	106	120		

5.5 Electrical Characteristics: 4.5V ≤ V_S < 8V (続き)

at T_A = 25°C, 4.5V ≤ V_S < 8V, V_{GRD} = V_{CM} = (V+) – 3V, V_{OUT} = V_S / 2, and R_L = 10kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
GBW	Unity gain bandwidth				2.5		MHz
SR	Slew rate	Gain = 1, 1V step	Falling		4.5		V/µs
			Rising		3.5		
t_s	Settling time	Gain = 1, 2V step, C_L = 20pF	To 0.01%,		2		µs
			To 0.001%		7		
t_{OR}	Overload recovery time	V_{IN} × gain = V_S	From overload to negative rail		0.8		µs
			From overload to positive rail		1.2		
THD+N	Total harmonic distortion + noise	Gain = 1, f = 1kHz, V_O = 0.5V_{RMS}			0.01%		
OUTPUT							
V_O	Voltage output swing from rail	No load			5	15	mV
		R_L = 10kΩ			50	110	
		R_L = 2kΩ			200	500	
I_{SC}	Short-circuit current				±30		mA
C_L	Capacitive load drive				See *Typical Characteristics*		
Z_O	Open-loop output impedance	f = 1MHz, I_O = 0A			800		Ω
POWER SUPPLY							
I_Q	Quiescent current	I_O = 0A			275	400	µA
			T_A = –40°C to +125°C			500	
TEMPERATURE							
	Thermal protection				180		°C
	Thermal hysteresis				30		°C
INTERNAL GUARD BUFFER							
V_{OSG}	Guard buffer input offset voltage	(V–) + 0.1V < V_{CM} < (V+) – 3V			±8	±50	µV
			T_A = –40°C to +125°C		±25	±150	
dV_{OSG}/dT	Guard buffer input offset voltage drift	T_A = –40°C to +125°C			±0.2	±1.2	µV/°C
V_{OGB}	Guard buffer output swing from rail(3)	No load			5	15	mV
	Guard buffer output impedance	I_O = 0A			1		kΩ
BW_{GB}	Guard buffer bandwidth				4.5		MHz

(1) RH = relative humidity.
(2) Specification established from device population bench system measurements across multiple lots.
(3) The guard pin voltage (V_{GRD}) is limited by the guard buffer output swing unless overdriven by an external source; see also セクション 7.1.3.

5.6 Electrical Characteristics: 8V ≤ V_S ≤ 16V

at T_A = 25°C, 8V ≤ V_S ≤ 16V, V_{GRD} = V_{CM} = V_{OUT} = V_S / 2, and R_L = 10kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT BIAS CURRENT							
I_B	Input bias current	RH < 50%(1)			±1	±20	fA
			T_A = –40°C to +85°C			±20	
I_{OS}	Input offset current	RH < 50%(1) (2)			±1	±20	fA
			T_A = –40°C to +85°C			±20	
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±5	±25	µV
		T_A = –40°C to +125°C			±20	±105	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C			±0.1	±0.8	µV/°C
PSRR	Power-supply rejection ratio	4.5V < V_S < 36V, V_{CM} = V_S / 2 – 0.75V	T_A = –40°C to +125°C		±0.3	±1.0	µV/V
NOISE							
	Input voltage noise	f = 0.1Hz to 10Hz	(V–) – 0.1V < V_{CM} < (V+) – 3V		1.4		$µV_{PP}$
e_n	Input voltage noise density	(V–) – 0.1V < V_{CM} < (V+) – 3V	f = 100Hz		18		nV/√Hz
			f = 1kHz		15		
i_n	Input current noise density	f = 0.1Hz			0.07		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage			(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	(V–) – 0.1V < V_{CM} < (V+) – 3V		108	124		dB
			T_A = –40°C to +125°C	104	120		
		(V+) – 3V < V_{CM} < (V+) + 0.1V		See *Typical Characteristics*			
INPUT IMPEDANCE							
Z_{ID}	Differential				750 || 3		GΩ || pF
Z_{IC}	Common-mode				1000 || 6		TΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 0.6V < V_O < (V+) – 0.6V, R_L = 2kΩ		116	132		dB
			T_A = –40°C to +125°C	110	126		
		(V–) + 0.3V < V_O < (V+) – 0.3V, R_L = 10kΩ		126	140		
			T_A = –40°C to +125°C	114	130		

5.6 Electrical Characteristics: 8V ≤ V_S ≤ 16V (続き)

at T_A = 25°C, 8V ≤ V_S ≤ 16V, V_{GRD} = V_{CM} = V_{OUT} = V_S / 2, and R_L = 10kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
GBW	Unity gain bandwidth				2.5		MHz
SR	Slew rate	Gain = 1, 10V step	Falling		6		V/µs
			Rising		5		
t_s	Settling time	To 0.01%, C_L = 20pF, gain = 1	2V step		2		µs
			10V step		2.5		
		To 0.001%, C_L = 20pF, gain = 1	2V step		7		
			10V step		16		
t_{OR}	Overload recovery time	V_{IN} × gain = V_S	From overload to negative rail		0.4		µs
			From overload to positive rail		1		
THD+N	Total harmonic distortion + noise	Gain = 1, f = 1kHz, V_O = 3.5V_{RMS}			0.0012%		
OUTPUT							
V_O	Voltage output swing from rail	No load			5	15	mV
		R_L = 10kΩ			50	110	
		R_L = 2kΩ			200	500	
I_{SC}	Short-circuit current	V_S = 16V			±65		mA
C_L	Capacitive load drive				See *Typical Characteristics*		
Z_O	Open-loop output impedance	f = 1MHz, I_O = 0A			800		Ω
POWER SUPPLY							
I_Q	Quiescent current	I_O = 0A			275	400	µA
			T_A = –40°C to +125°C			500	
TEMPERATURE							
	Thermal protection				180		°C
	Thermal hysteresis				30		°C
INTERNAL GUARD BUFFER							
V_{OSG}	Guard buffer input offset voltage	(V–) + 0.1V < V_{CM} < (V+) – 3V			±8	±50	µV
			T_A = –40°C to +125°C		±25	±150	
dV_{OSG}/dT	Guard buffer input offset voltage drift	T_A = –40°C to +125°C			±0.2	±1.2	µV/°C
V_{OG}	Guard buffer output swing from rail(3)	No load			5	15	mV
	Guard buffer output impedance	I_O = 0A			1		kΩ
BW_{GB}	Guard buffer bandwidth				4.5		MHz

(1) RH = relative humidity.
(2) Specification established from device population bench system measurements across multiple lots.
(3) The guard pin voltage (V_{GRD}) is limited by the guard buffer output swing unless overdriven by an external source; see also セクション 7.1.3.

5.7 Electrical Characteristics: 16V < V_S ≤ 36V

at T_A = 25°C, 16V < V_S ≤ 36V, V_{GRD} = V_{CM} = V_{OUT} = V_S / 2, and R_L = 10kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT BIAS CURRENT							
I_B	Input bias current(1)	RH < 50%(2)			±1	±75	fA
			T_A = –40°C to +85°C			±75	
I_{OS}	Input offset current	RH < 50%(2) (3)			±1	±75	fA
			T_A = –40°C to +85°C			±75	
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±5	±25	µV
		T_A = –40°C to +125°C			±20	±105	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C			±0.1	±0.8	µV/°C
PSRR	Power-supply rejection ratio	4.5V < V_S < 36V, V_{CM} = V_S / 2 – 0.75V	T_A = –40°C to +125°C		±0.3	±1.0	µV/V
NOISE							
	Input voltage noise	f = 0.1Hz to 10Hz	(V–) – 0.1V < V_{CM} < (V+) – 3V		1.4		$µV_{PP}$
e_n	Input voltage noise density	(V–) – 0.1V < V_{CM} < (V+) – 3V	f = 100Hz		18		nV/√Hz
			f = 1kHz		15		
i_n	Input current noise density	f = 0.1Hz			0.07		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage			(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	(V–) – 0.1V < V_{CM} < (V+) – 3V		114	130		dB
			T_A = –40°C to +125°C	112	128		
		(V+) – 3V < V_{CM} < (V+) + 0.1V		See *Typical Characteristics*			
INPUT IMPEDANCE							
Z_{ID}	Differential				750 || 3		GΩ || pF
Z_{IC}	Common-mode				1000 || 6		TΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 1V < V_O < (V+) – 1V, R_L = 2kΩ		124	138		dB
			T_A = –40°C to +125°C	116	130		
		(V–) + 0.3V < V_O < (V+) – 0.3V, R_L = 10kΩ		126	140		
			T_A = –40°C to +125°C	118	134		

5.7 Electrical Characteristics: 16V < V_S ≤ 36V (続き)

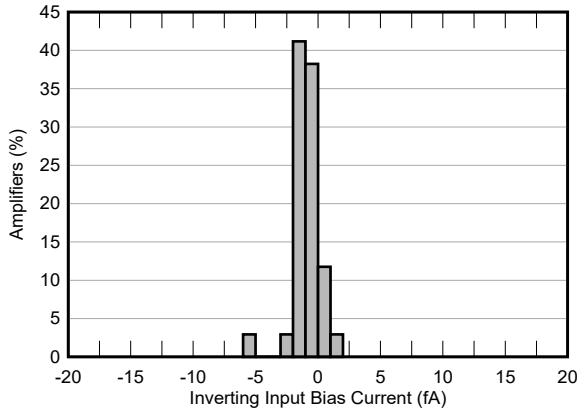
at T_A = 25°C, 16V < V_S ≤ 36V, V_{GRD} = V_{CM} = V_{OUT} = V_S / 2, and R_L = 10kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
GBW	Unity gain bandwidth				2.5		MHz
SR	Slew rate	Gain = 1, 10V step	Falling		6		V/µs
			Rising		5		
t_s	Settling time	To 0.01%, C_L = 20pF, gain = 1,	2V step		2		µs
			10V step		2.5		
		To 0.001%, C_L = 20pF, gain = 1	2V step		7		
			10V step		16		
t_{OR}	Overload recovery time	V_{IN} × gain = V_S	From overload to negative rail		0.4		µs
			From overload to positive rail		1		
THD+N	Total harmonic distortion + noise	Gain = 1, f = 1kHz, V_O = 3.5V_{RMS}			0.0012%		
OUTPUT							
V_O	Voltage output swing from rail	No load			0.05	0.1	V
		R_L = 10kΩ			0.1	0.5	
		R_L = 2kΩ			0.5	1	
I_{SC}	Short-circuit current	V_S = 36V			±65		mA
C_L	Capacitive load drive				See *Typical Characteristics*		
Z_O	Open-loop output impedance	f = 1MHz, I_O = 0A			800		Ω
POWER SUPPLY							
I_Q	Quiescent current	I_O = 0A			275	400	µA
			T_A = –40°C to +125°C			500	
TEMPERATURE							
	Thermal protection				180		°C
	Thermal hysteresis				30		°C
INTERNAL GUARD BUFFER							
V_{OSGB}	Guard buffer input offset voltage				±8	±50	µV
		T_A = –40°C to +125°C			±25	±150	
dV_{OSGB}/dT	Guard buffer input offset voltage drift	T_A = –40°C to +125°C			±0.2	±1.2	µV/°C
V_{OGB}	Guard buffer output swing from rail(4)	No load			5	15	mV
	Guard buffer output impedance	I_O = 0A			1		kΩ
BW_{GB}	Guard buffer bandwidth				4.5		MHz

(1) For input common-mode voltage greater than (V–) + 20V, see *Typical Characteristics*.
(2) RH = relative humidity.
(3) Specification established from device population bench system measurements across multiple lots.
(4) The guard pin voltage (V_{GRD}) is limited by the guard buffer output swing unless overdriven by an external source; see also セクション 7.1.3.

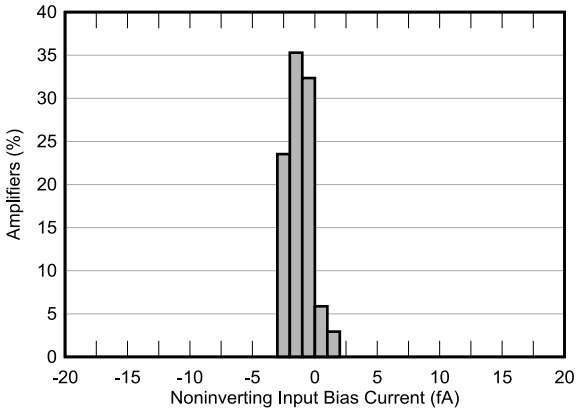
5.8 Typical Characteristics

at T_A = 25°C, V_S = 16V, V_{GRD} = V_{CM} = V_S / 2, R_L = 10kΩ connected to V_S / 2, and C_L = 100pF (unless otherwise noted)



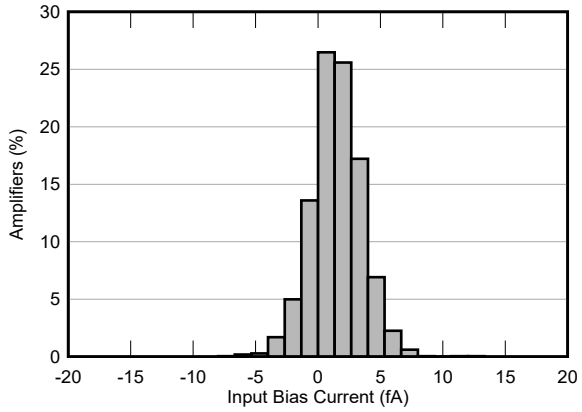
V_S = 4.5V, T_A = 85°C, I_{BN}

図 5-1. Input Bias Current Production Distribution



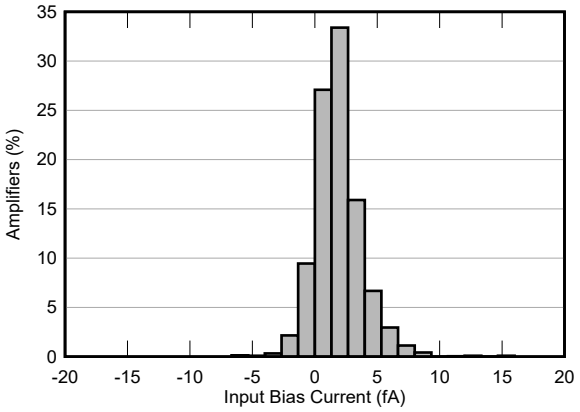
V_S = 4.5V, T_A = 85°C, I_{BP}

図 5-2. Input Bias Current Production Distribution



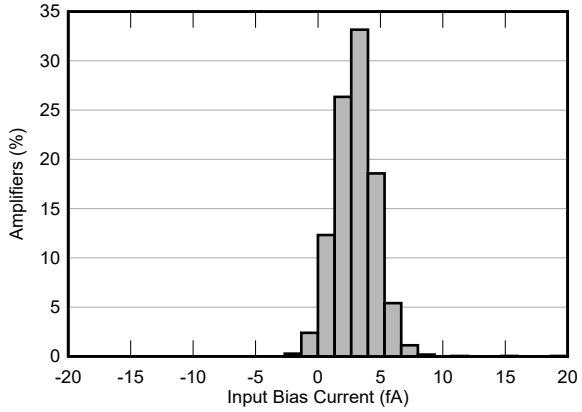
V_S = 16V, T_A = 85°C, I_{BN}, 2126 units

図 5-3. Input Bias Current Production Distribution



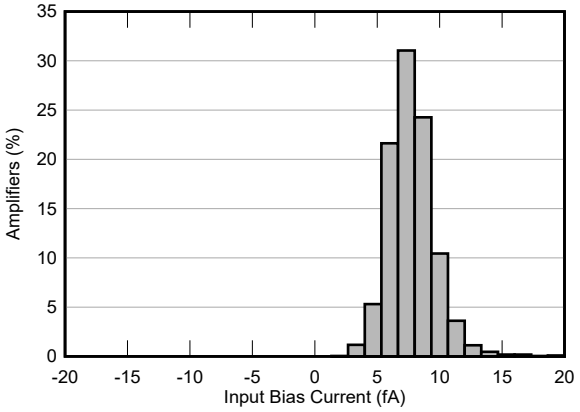
V_S = 16V, T_A = 85°C, I_{BP}, 2126 units

図 5-4. Input Bias Current Production Distribution



V_S = 36V, T_A = 85°C, I_{BN}, 2126 units

図 5-5. Input Bias Current Production Distribution

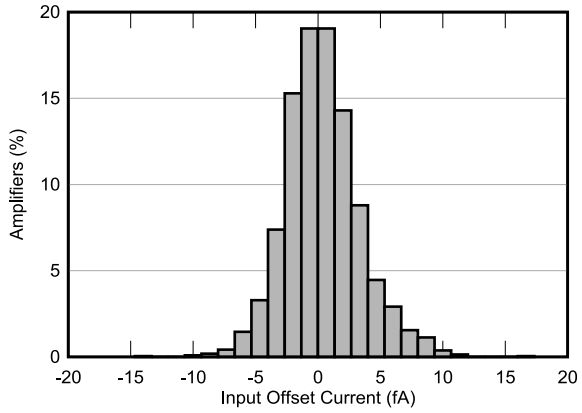


V_S = 36V, T_A = 85°C, I_{BP}, 2126 units

図 5-6. Input Bias Current Production Distribution

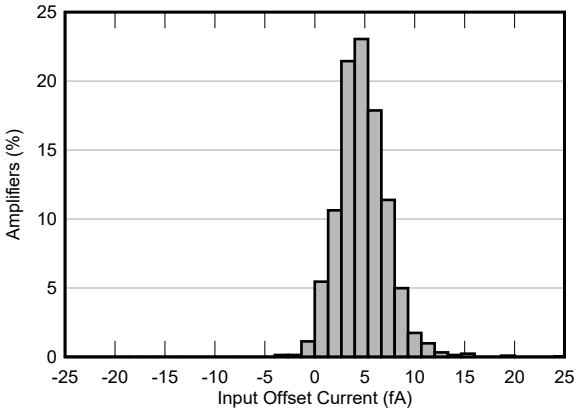
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 16V, V_{GRD} = V_{CM} = V_S / 2, R_L = 10kΩ connected to V_S / 2, and C_L = 100pF (unless otherwise noted)



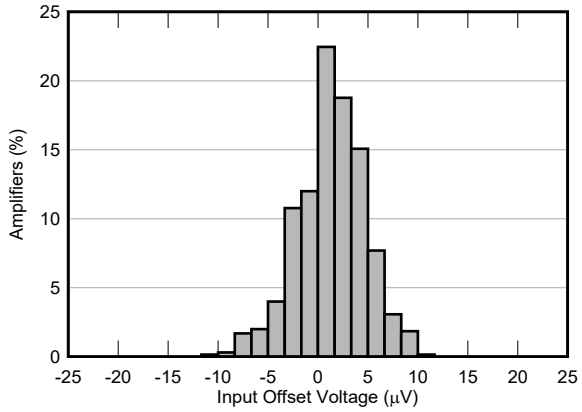
V_S = 16V, T_A = 85°C, 2126 units

図 5-7. Input Bias Offset Current Production Distribution



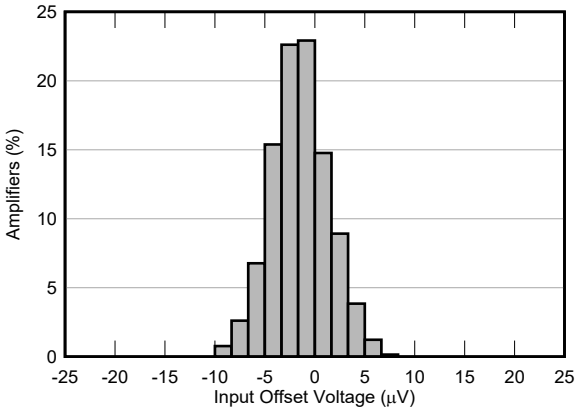
V_S = 36V, T_A = 85°C, 2126 units

図 5-8. Input Bias Offset Current Production Distribution



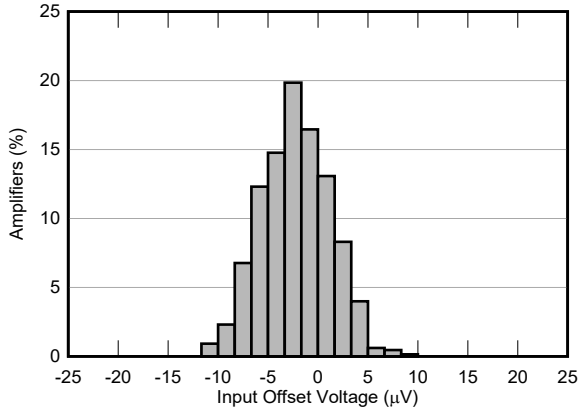
V_S = 4.5V, 650 units

図 5-9. Offset Voltage Production Distribution



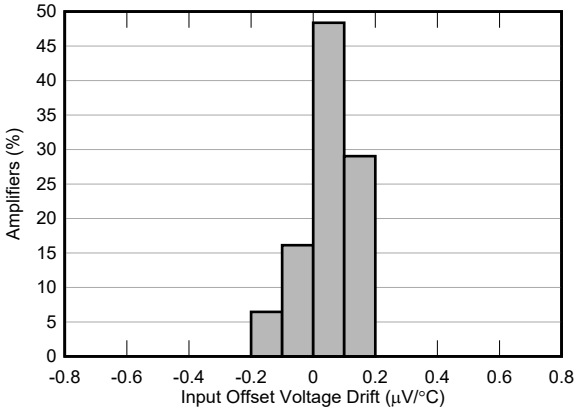
V_S = 16V, 650 units

図 5-10. Offset Voltage Production Distribution



V_S = 36V, 650 units

図 5-11. Offset Voltage Production Distribution

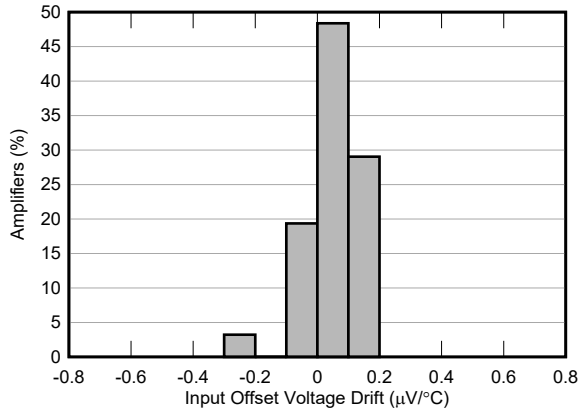


V_S = 4.5V, T_A = –40°C to +125°C, 34 units

図 5-12. Offset Voltage Drift Distribution

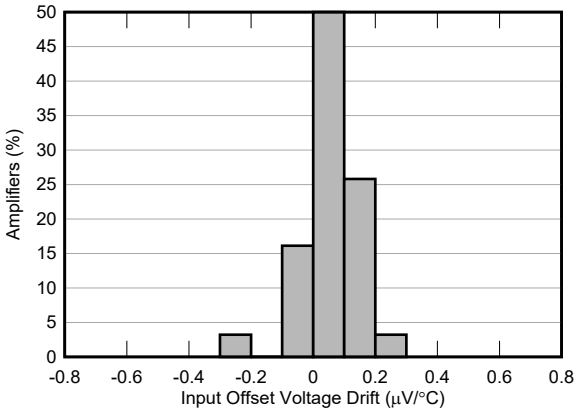
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 16V, V_{GRD} = V_{CM} = V_S / 2, R_L = 10kΩ connected to V_S / 2, and C_L = 100pF (unless otherwise noted)



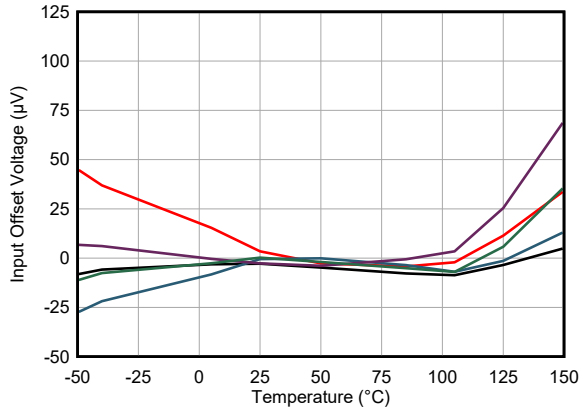
V_S = 16V, T_A = –40°C to +125°C, 34 units

図 5-13. Offset Voltage Drift Distribution



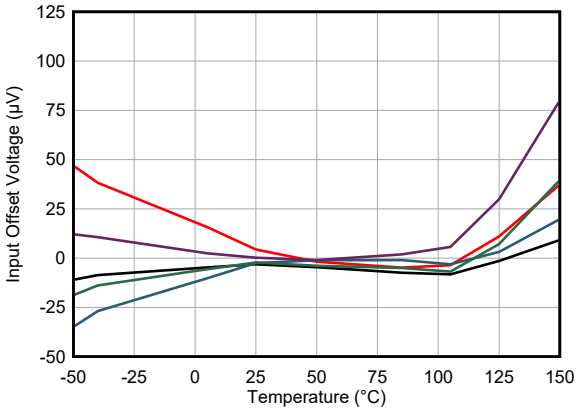
V_S = 36V, T_A = –40°C to +125°C, 34 units

図 5-14. Offset Voltage Drift Distribution



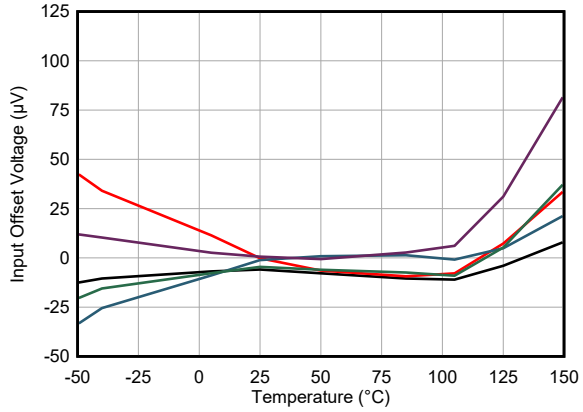
V_S = 4.5V, 5 typical units

図 5-15. Offset Voltage vs Temperature



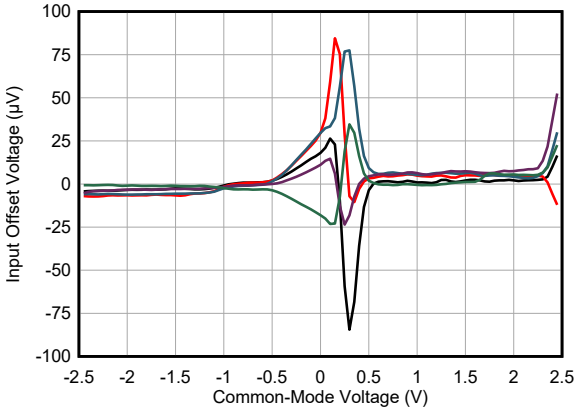
V_S = 16V, 5 typical units

図 5-16. Offset Voltage vs Temperature



V_S = 36V, 5 typical units

図 5-17. Offset Voltage vs Temperature

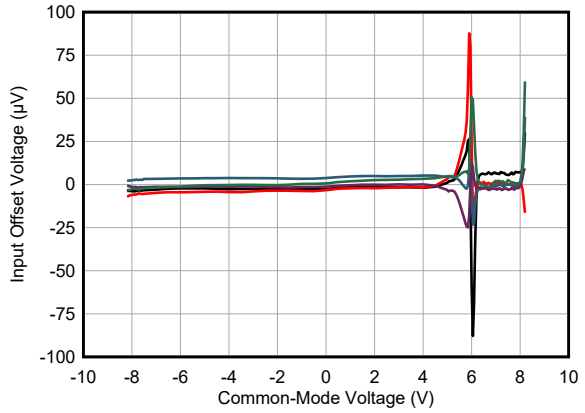


V_S = 4.5V, 5 typical units

図 5-18. Offset Voltage vs Common-Mode Voltage

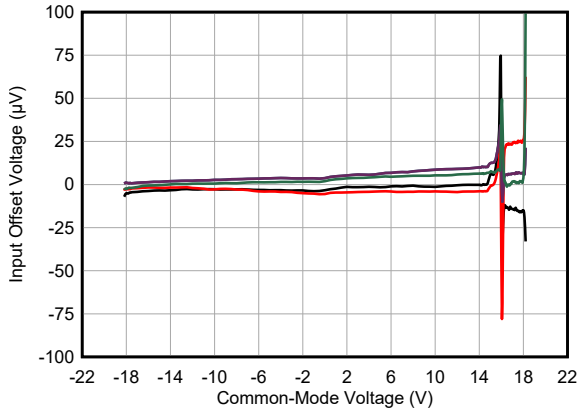
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 16V, V_{GRD} = V_{CM} = V_S / 2, R_L = 10kΩ connected to V_S / 2, and C_L = 100pF (unless otherwise noted)



V_S = 16V, 5 typical units

図 5-19. Offset Voltage vs Common-Mode Voltage in Transition Region



V_S = 36V, 5 typical units

図 5-20. Offset Voltage vs Common-Mode Voltage in Transition Region

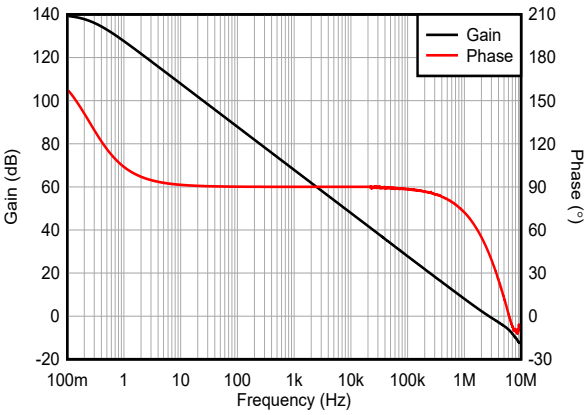


図 5-21. Open-Loop Gain and Phase vs Frequency

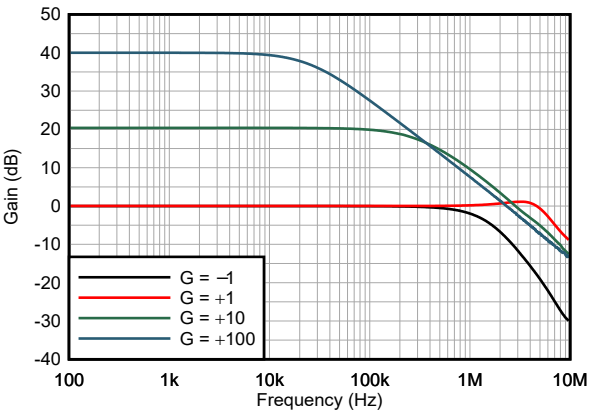
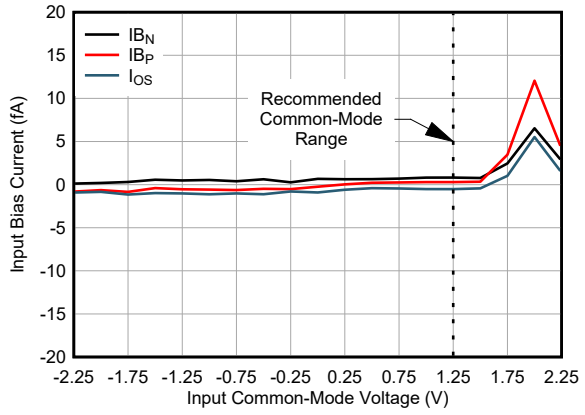
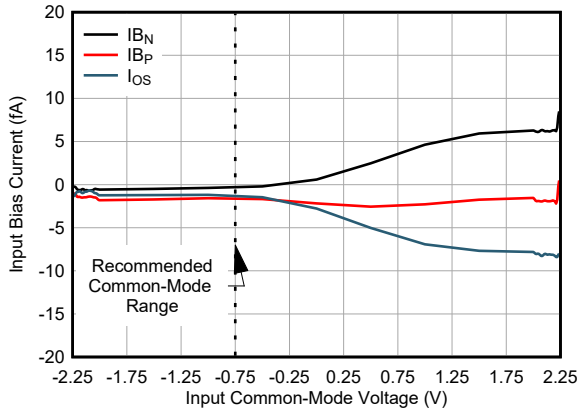


図 5-22. Closed-Loop Gain vs Frequency



V_S = 4.5V, T_A = 25°C

図 5-23. Input Bias Current vs Common-Mode Voltage

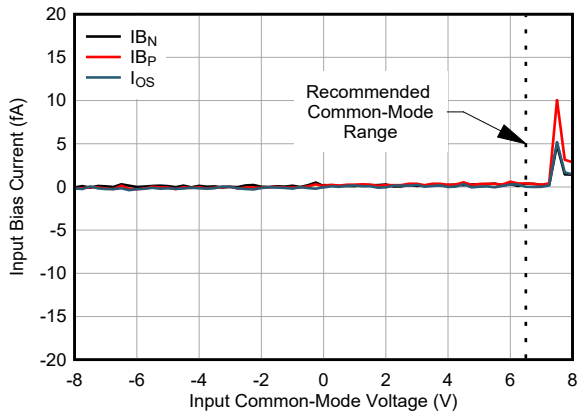


V_S = 4.5V, T_A = 85°C

図 5-24. Input Bias Current vs Common-Mode Voltage

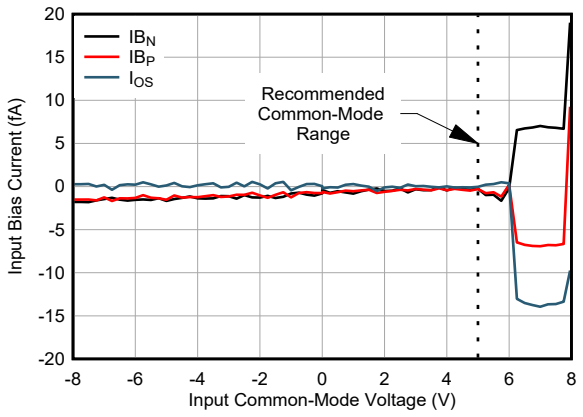
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 16V, V_{GRD} = V_{CM} = V_S / 2, R_L = 10kΩ connected to V_S / 2, and C_L = 100pF (unless otherwise noted)



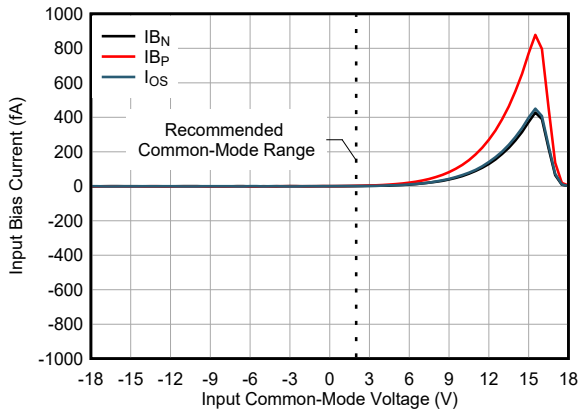
V_S = 16V, T_A = 25°C

図 5-25. Input Bias Current vs Common-Mode Voltage



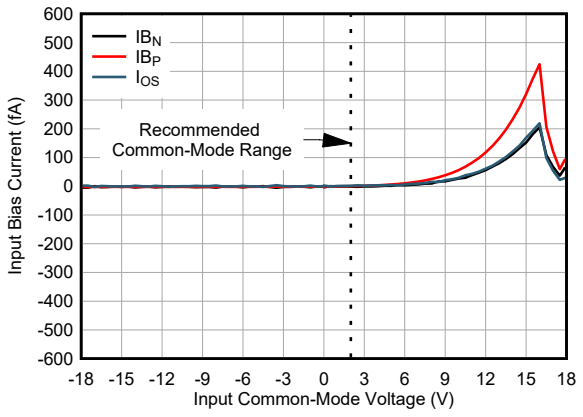
V_S = 16V, T_A = 85°C

図 5-26. Input Bias Current vs Common-Mode Voltage



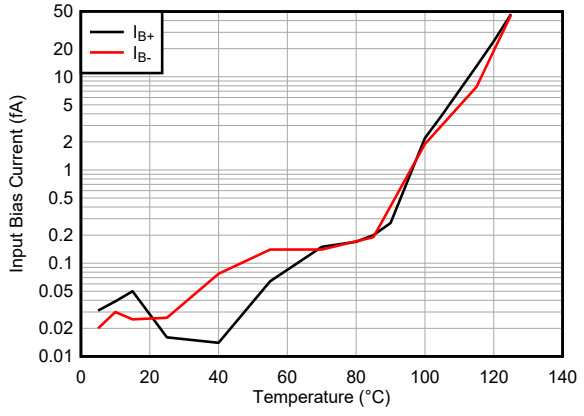
V_S = 36V, T_A = 25°C

図 5-27. Input Bias Current vs Common-Mode Voltage



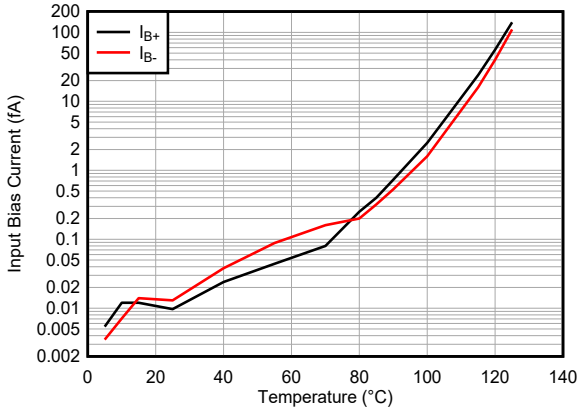
V_S = 36V, T_A = 85°C

図 5-28. Input Bias Current vs Common-Mode Voltage



V_S = 4.5V, RH = 10%

図 5-29. Input Bias Current vs Temperature

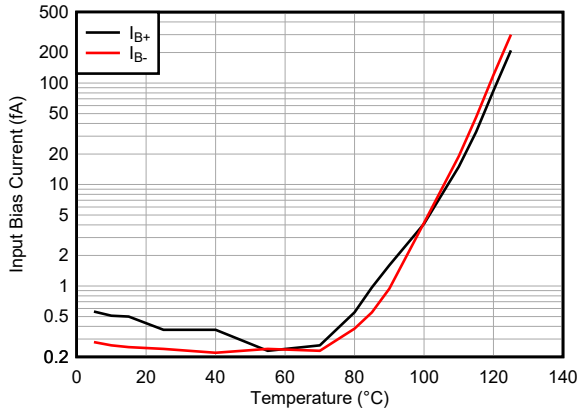


V_S = 16V, RH = 10%

図 5-30. Input Bias Current vs Temperature

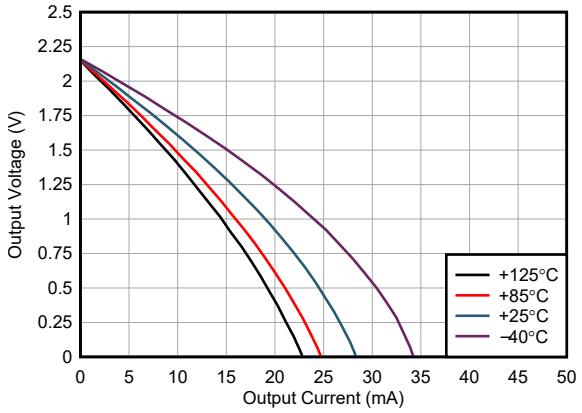
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 16V, V_{GRD} = V_{CM} = V_S / 2, R_L = 10kΩ connected to V_S / 2, and C_L = 100pF (unless otherwise noted)



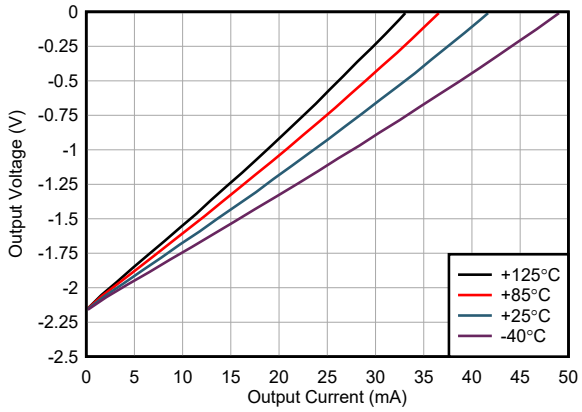
V_S = 36V, RH = 10%

図 5-31. Input Bias Current vs Temperature



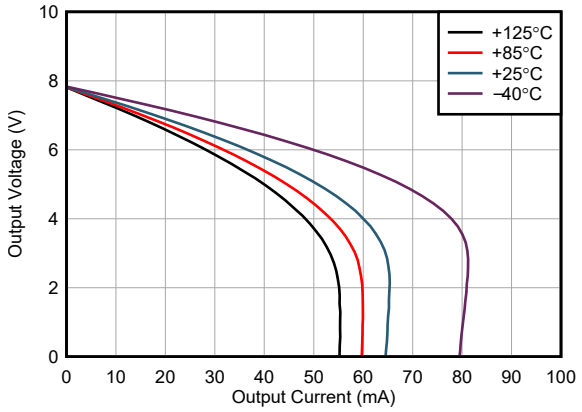
V_S = 4.5V, sourcing

図 5-32. Output Voltage Swing vs Output Current



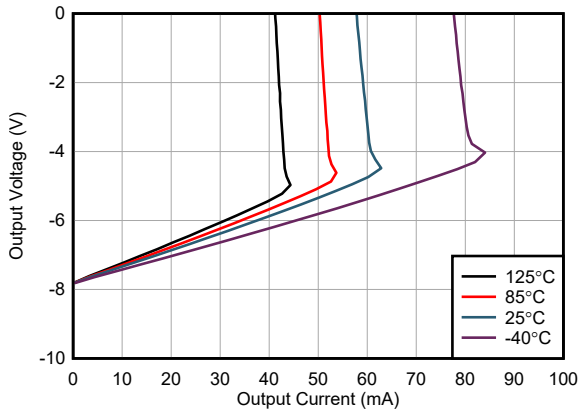
V_S = 4.5V, sinking

図 5-33. Output Voltage Swing vs Output Current



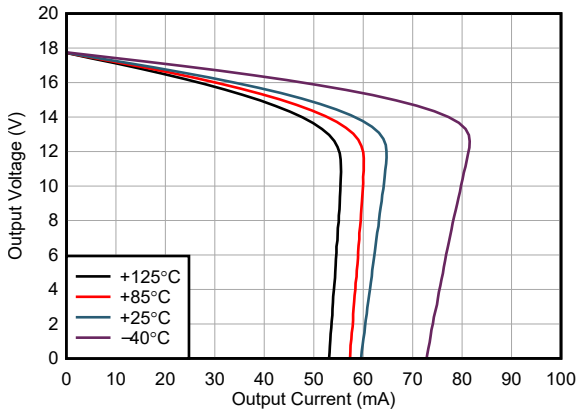
V_S = 16V, sourcing

図 5-34. Output Voltage Swing vs Output Current



V_S = 16V, sinking

図 5-35. Output Voltage Swing vs Output Current

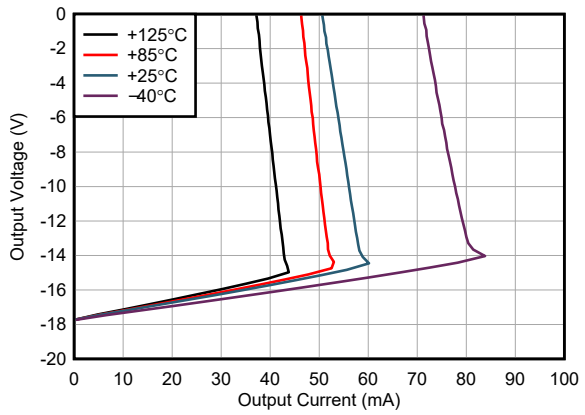


V_S = 36V, sourcing

図 5-36. Output Voltage Swing vs Output Current

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 16V, V_{GRD} = V_{CM} = V_S / 2, R_L = 10kΩ connected to V_S / 2, and C_L = 100pF (unless otherwise noted)



V_S = 36V, sinking

図 5-37. Output Voltage Swing vs Output Current

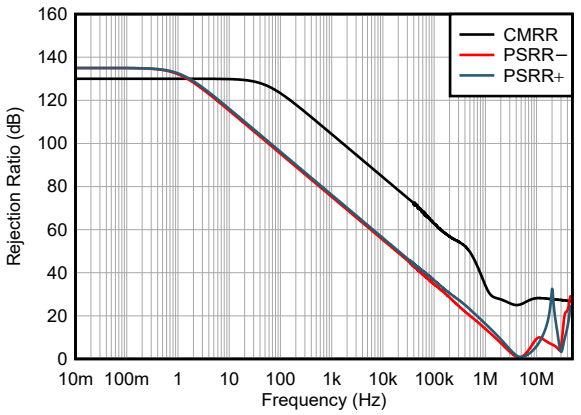


図 5-38. CMRR and PSRR vs Frequency

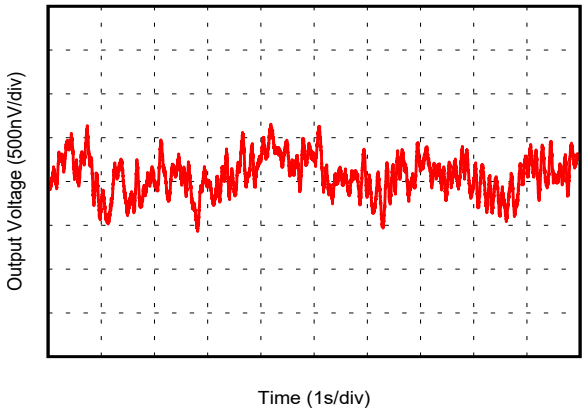


図 5-39. 0.1Hz to 10Hz Noise

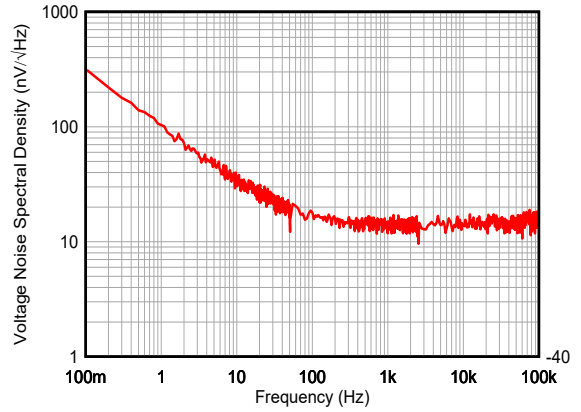


図 5-40. Input Voltage Noise Spectral Density vs Frequency

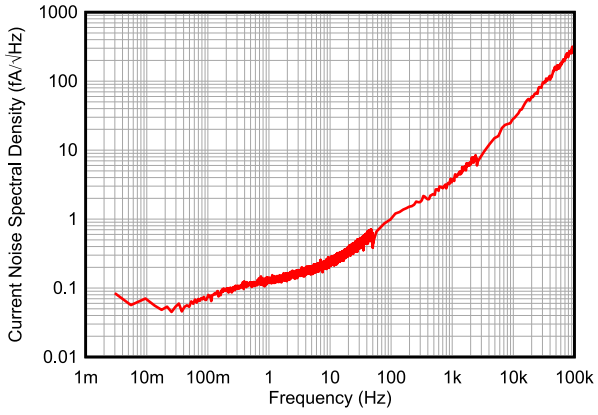
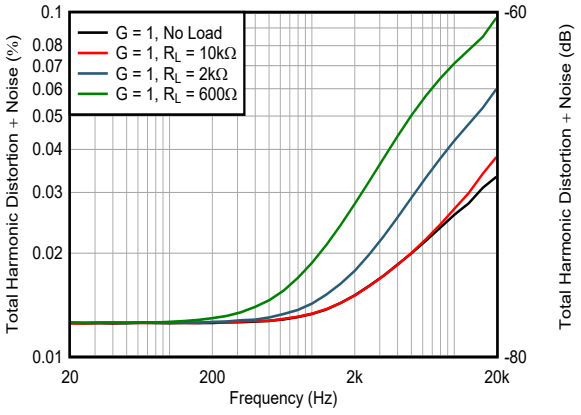


図 5-41. Input Current Noise Spectral Density vs Frequency

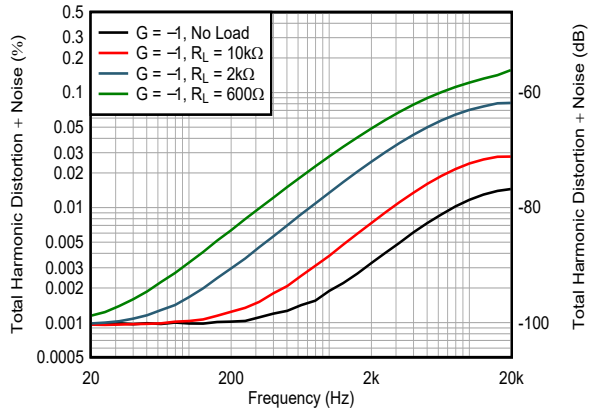


V_S = 4.5V

図 5-42. THD+N vs Frequency

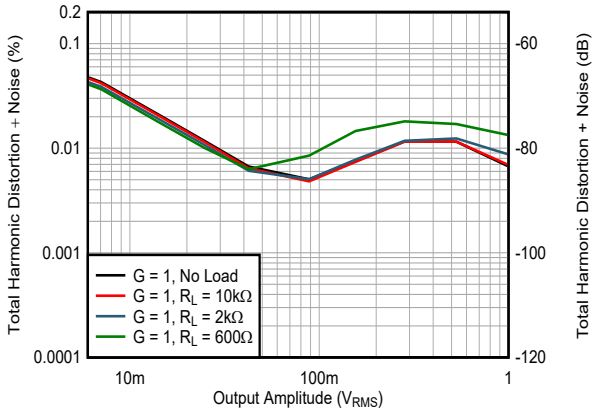
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 16V, V_{GRD} = V_{CM} = V_S / 2, R_L = 10kΩ connected to V_S / 2, and C_L = 100pF (unless otherwise noted)



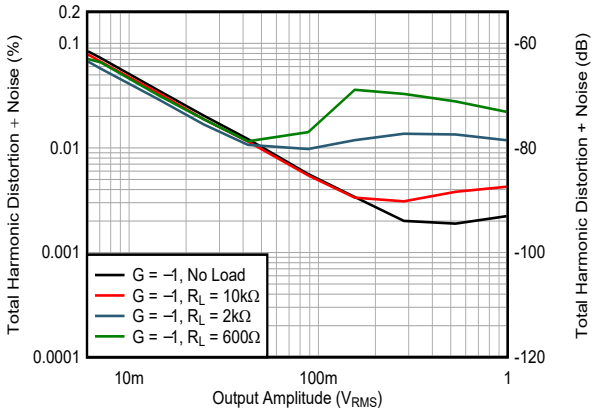
V_S = 4.5V

図 5-43. THD+N vs Frequency



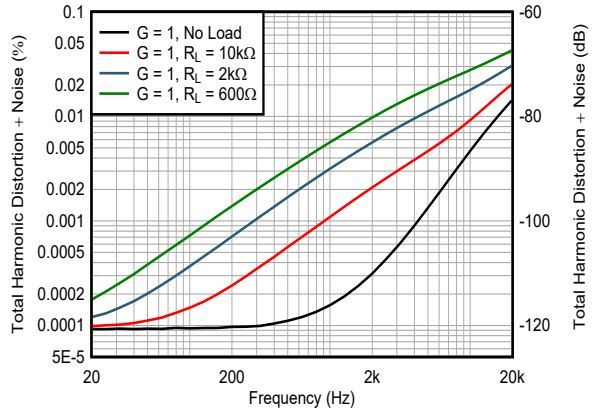
V_S = 4.5V

図 5-44. THD+N vs Output Amplitude



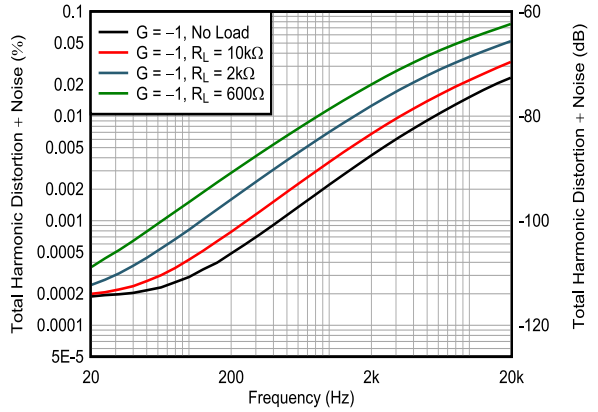
V_S = 4.5V

図 5-45. THD+N vs Output Amplitude



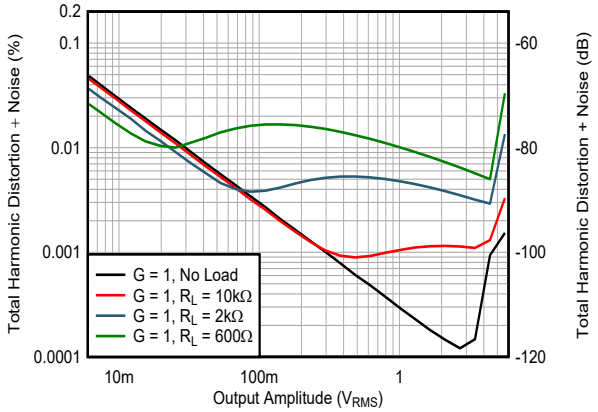
V_S = 16V

図 5-46. THD+N vs Frequency



V_S = 16V

図 5-47. THD+N vs Frequency



V_S = 16V

図 5-48. THD+N vs Output Amplitude

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 16V, V_{GRD} = V_{CM} = V_S / 2, R_L = 10kΩ connected to V_S / 2, and C_L = 100pF (unless otherwise noted)

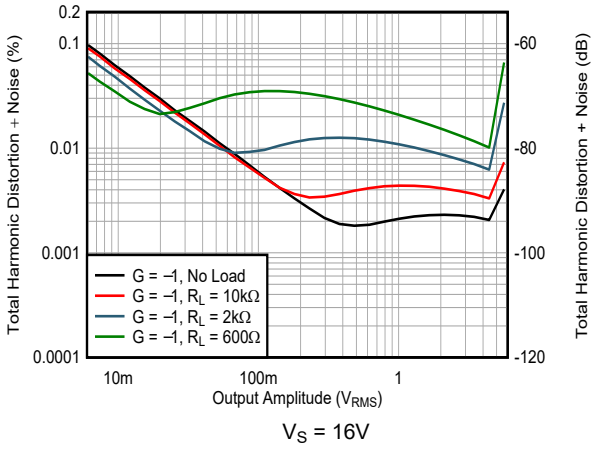


図 5-49. THD+N vs Output Amplitude

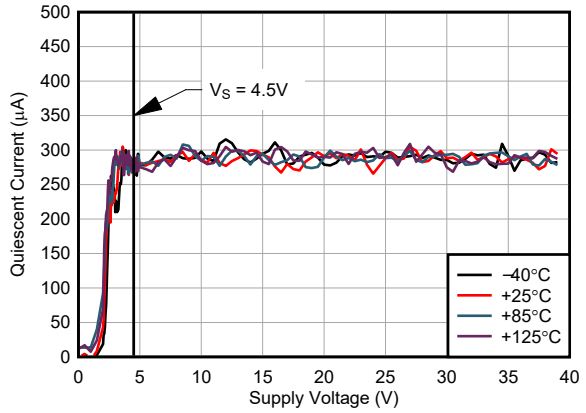


図 5-50. Quiescent Current vs Supply Voltage

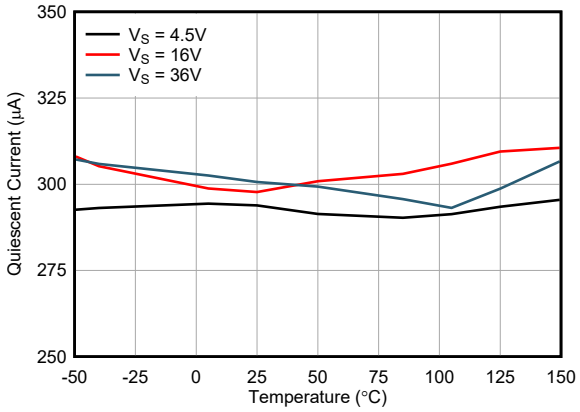


図 5-51. Quiescent Current vs Temperature

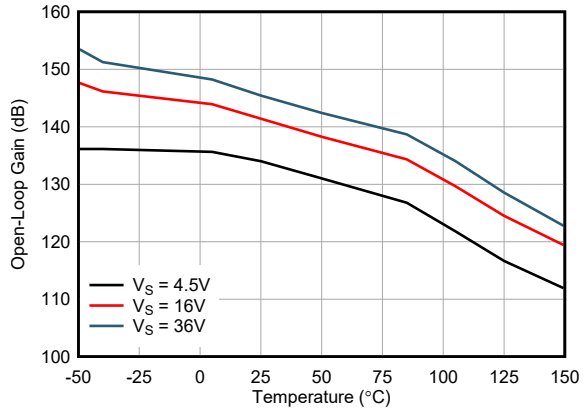


図 5-52. Open-Loop Gain vs Temperature

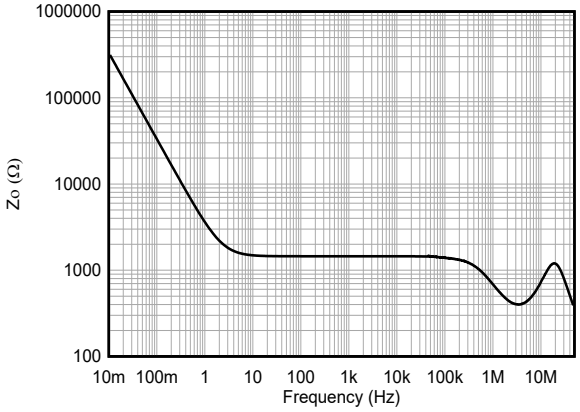


図 5-53. Open-Loop Output Impedance vs Frequency

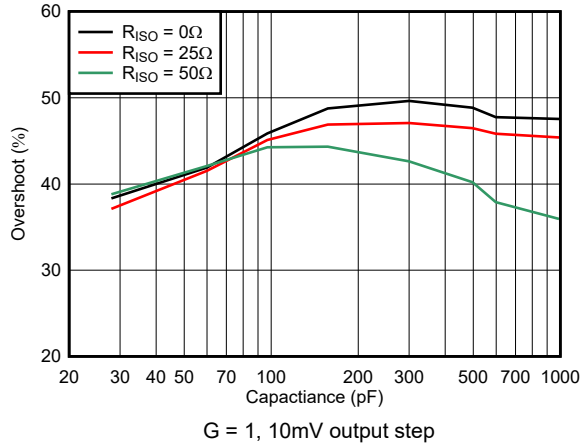
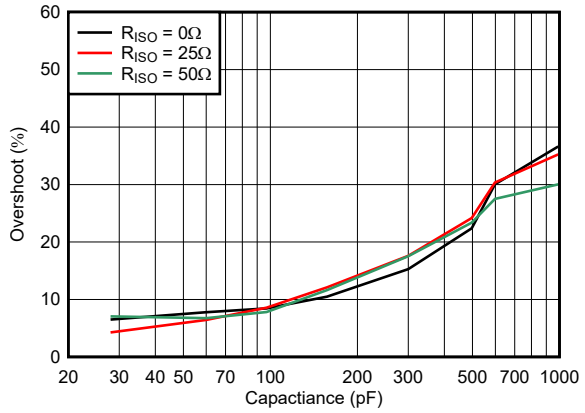


図 5-54. Small-Signal Overshoot vs Capacitive Load

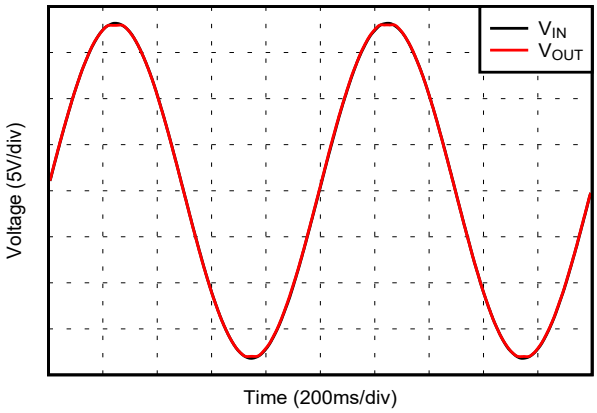
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 16V, V_{GRD} = V_{CM} = V_S / 2, R_L = 10kΩ connected to V_S / 2, and C_L = 100pF (unless otherwise noted)



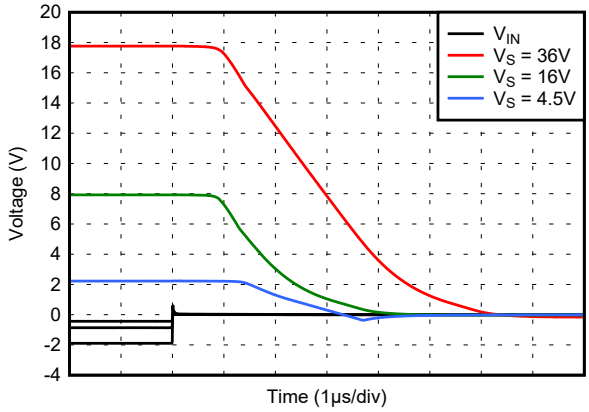
G = −1, 10mV output step

図 5-55. Small-Signal Overshoot vs Capacitive Load



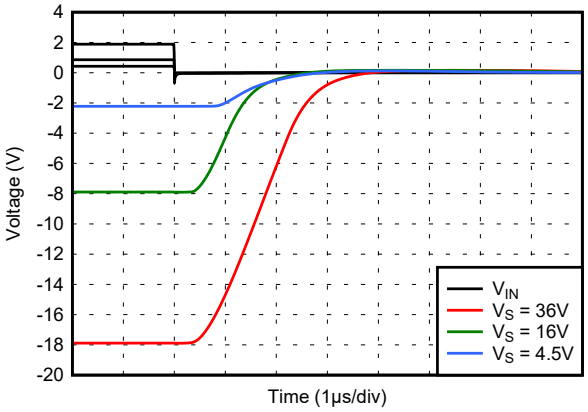
V_S = 36V

図 5-56. No Phase Reversal



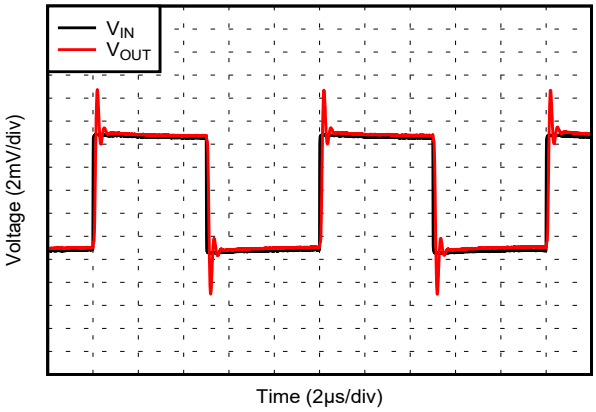
G = –10V/V

図 5-57. Positive Overload Recovery



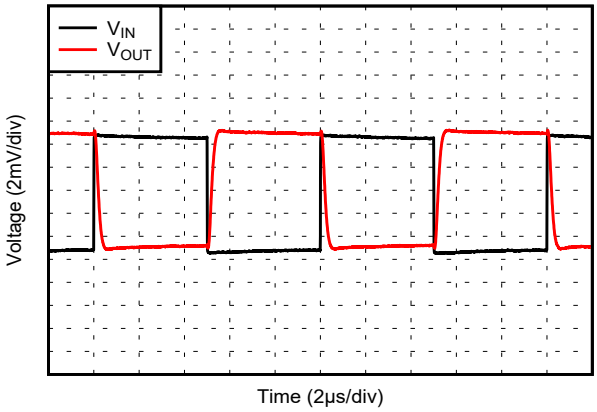
G = –10V/V

図 5-58. Negative Overload Recovery



G = 1, C_L = 10pF, 10mV step

図 5-59. Small-Signal Step Response

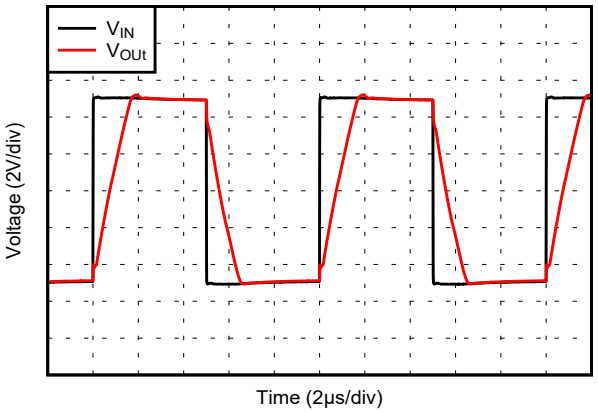


G = −1, C_L = 10pF, 10mV step

図 5-60. Small-Signal Step Response

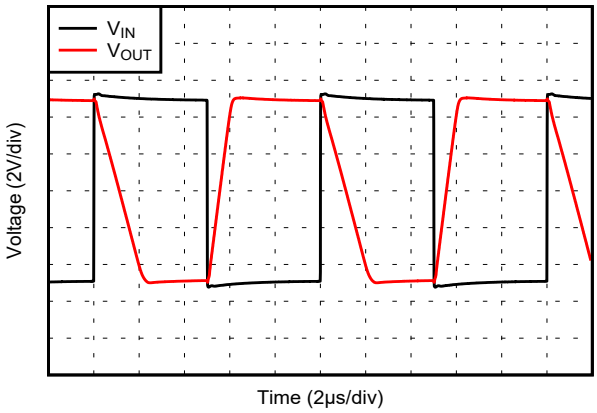
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 16V, V_{GRD} = V_{CM} = V_S / 2, R_L = 10kΩ connected to V_S / 2, and C_L = 100pF (unless otherwise noted)



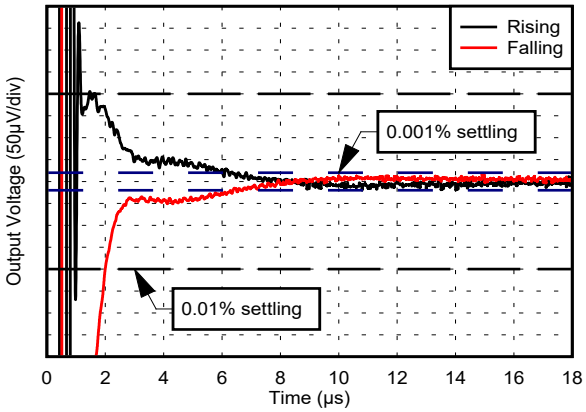
G = 1, C_L = 10pF, 10mV step

図 5-61. Large-Signal Step Response



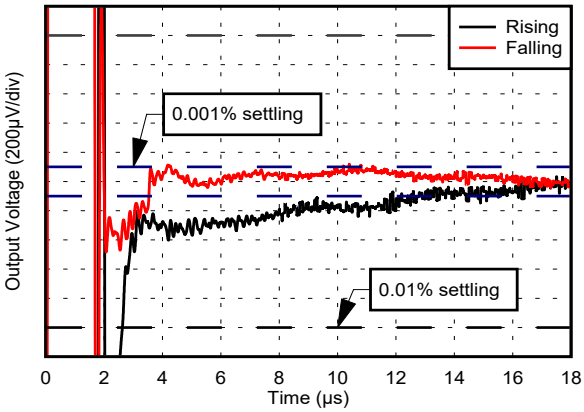
G = −1, C_L = 10pF, 10mV step

図 5-62. Large-Signal Step Response



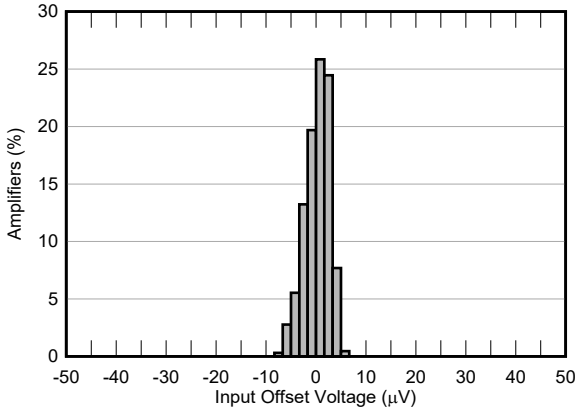
Gain = 1, C_L = 10pF, 2V step applied at t = 0µs

図 5-63. Settling Time



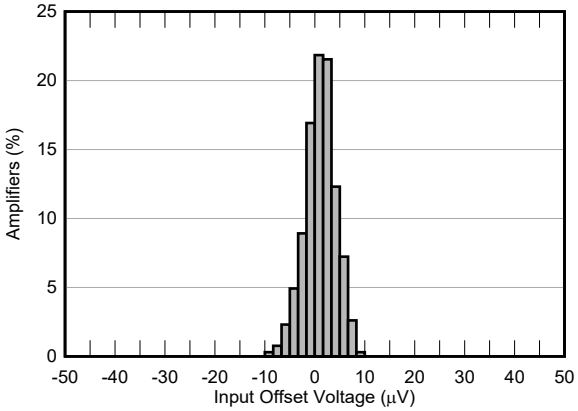
Gain = 1, C_L = 10pF, 10V step applied at t = 0µs

図 5-64. Settling Time



V_S = 4.5V, 650 units

図 5-65. Guard Buffer Offset Distribution

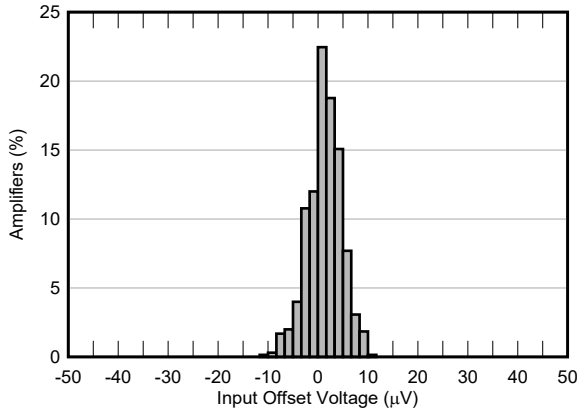


V_S = 16V, 650 units

図 5-66. Guard Buffer Offset Distribution

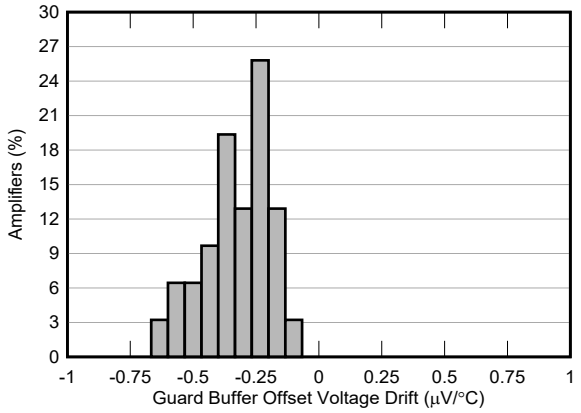
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 16V, V_{GRD} = V_{CM} = V_S / 2, R_L = 10kΩ connected to V_S / 2, and C_L = 100pF (unless otherwise noted)



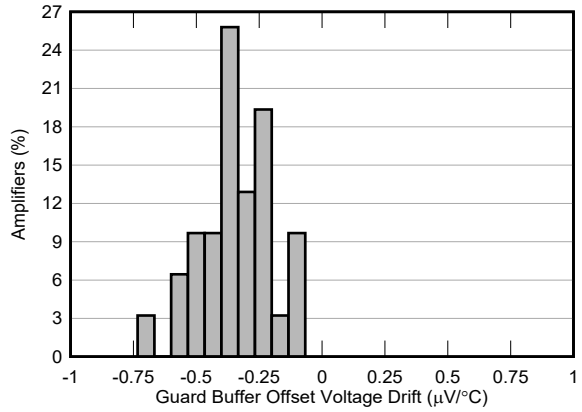
V_S = 36V, 650 units

図 5-67. Guard Buffer Offset Distribution



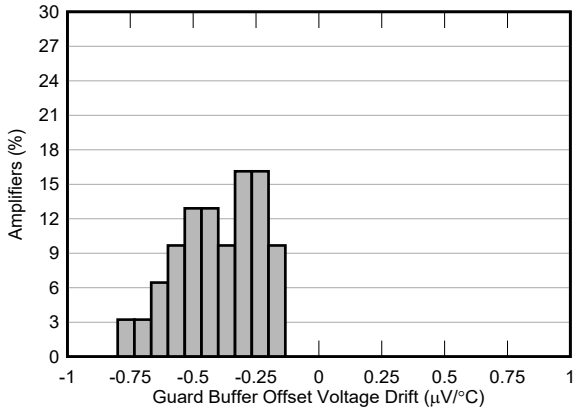
V_S = 4.5V, 34 units

図 5-68. Guard Buffer Offset Drift Distribution



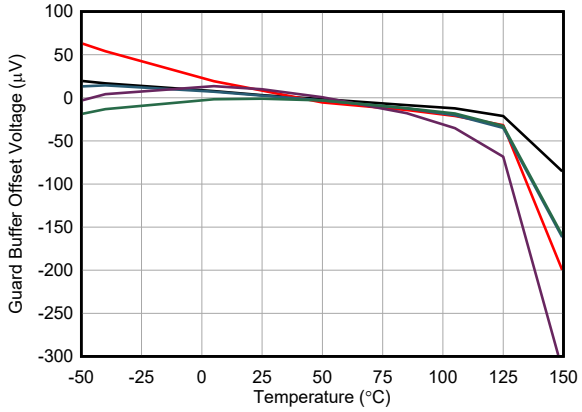
V_S = 16V, 34 units

図 5-69. Guard Buffer Offset Drift Distribution



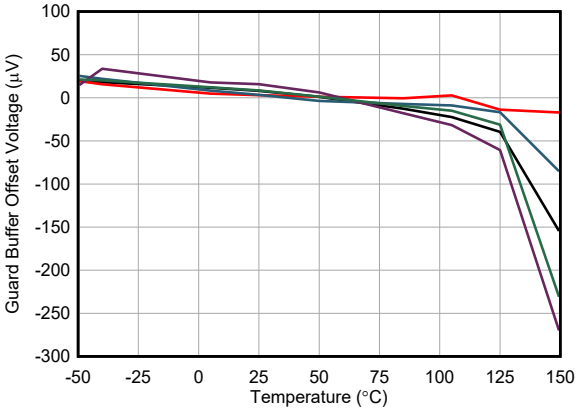
V_S = 36V, 34 units

図 5-70. Guard Buffer Offset Drift Distribution



V_S = 4.5V, 5 typical units

図 5-71. Guard Buffer Offset Voltage vs Temperature

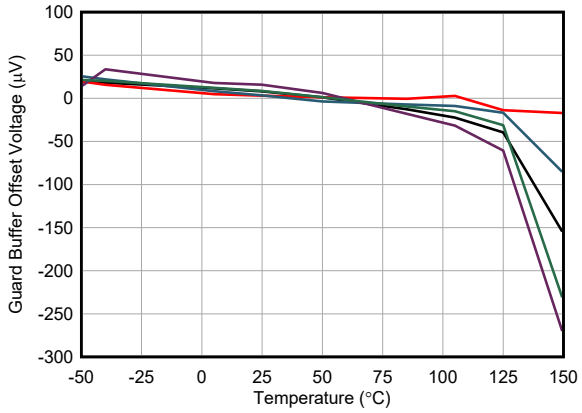


V_S = 4.5V, 5 typical units

図 5-72. Guard Buffer Offset Voltage vs Temperature

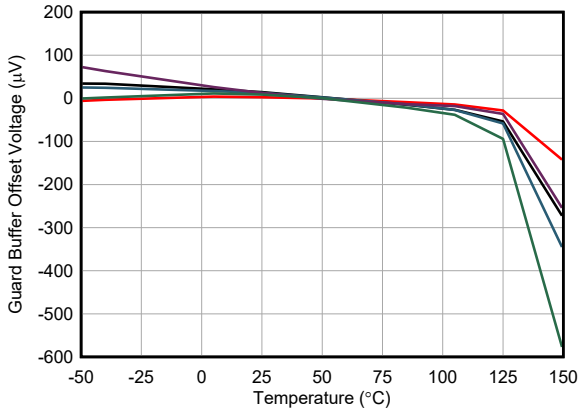
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 16V, V_{GRD} = V_{CM} = V_S / 2, R_L = 10kΩ connected to V_S / 2, and C_L = 100pF (unless otherwise noted)



V_S = 16V, 5 typical units

図 5-73. Guard Buffer Offset Voltage vs Temperature



V_S = 36V, 5 typical units

図 5-74. Guard Buffer Offset Voltage vs Temperature

6 Detailed Description

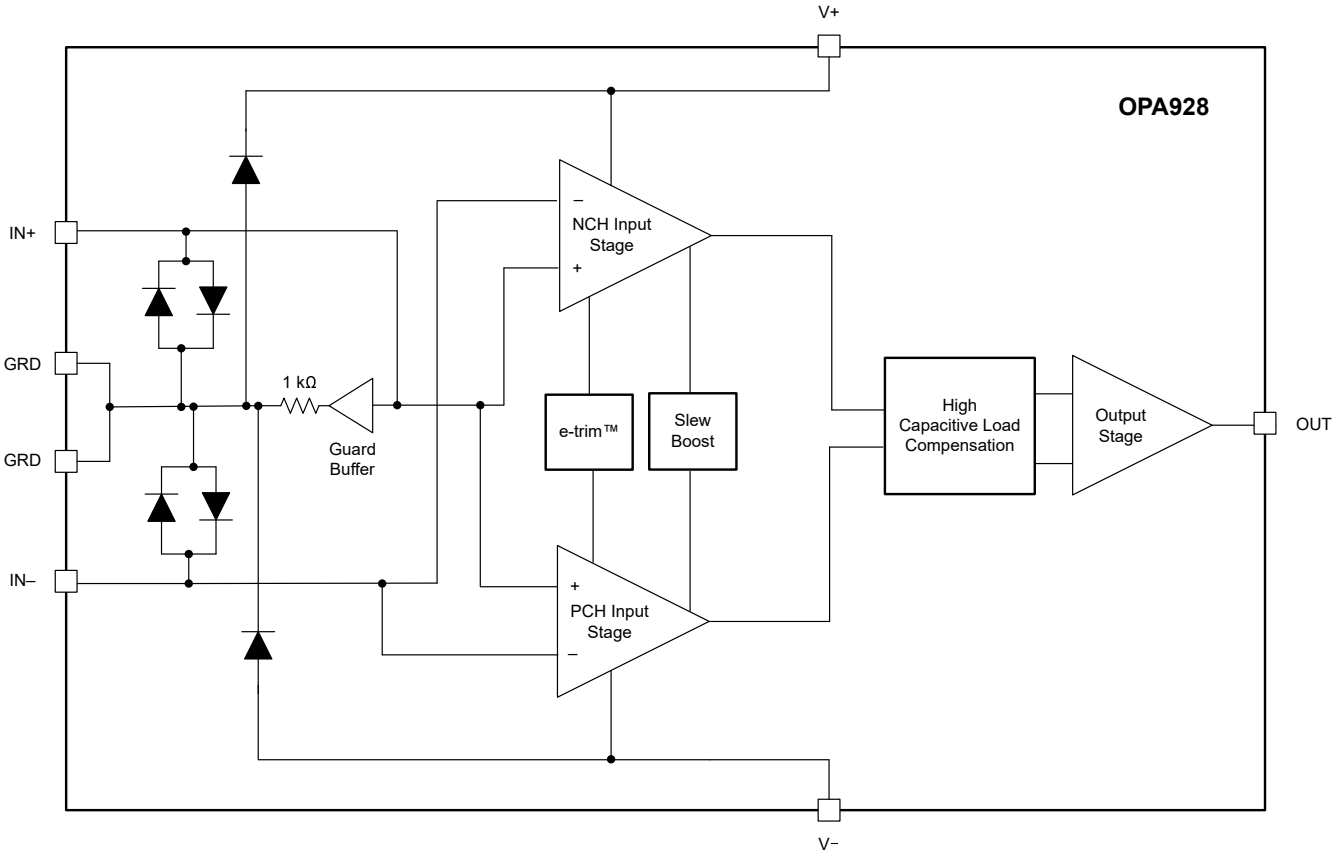
6.1 Overview

The OPA928 is an ultra-low input bias current, low-power, high-precision, e-trim operational amplifier (op amp). This op amp features state-of-the art CMOS technology and advanced design techniques to provide extremely low input bias current (< 20fA) performance across the entire industrial temperature range of −40ºC to +85ºC. In addition, the OPA928 operates from 4.5V to 36V, is unity-gain stable, and post-package trimmed to achieve very low offset and offset drift performance.

To facilitate the design of guard rings around high-impedance traces, the OPA928 features an integrated, high-precision guard buffer. Access to the internal guard buffer output is provided by using two pins of the low-leakage friendly pin out of the amplifier.

The excellent dc performance and unique features combined with stellar ac performance like ultra-low current noise, low voltage noise, and wide bandwidth, make the OPA928 an excellent choice for interfacing very high impedance sensors, and photodiodes.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Guard Buffer

To achieve a femtoampere-level input bias current, the OPA928 uses an internal, high-precision, rail-to-rail guard buffer connected to the noninverting input. The guard buffer follows the voltage at the input of the OPA928 to generate a near zero differential voltage across the internal antiparallel diodes (detailed in セクション 6.3.2), nearly eliminating the leakage current though the diodes. The guard buffer output can be accessed through the guard pins (2 and 7). Use the guard pins to protect external components and input traces from possible current leakage paths. The guard buffer is isolated from large capacitive loads that can be present at the guard pins by a nominal 1kΩ resistor. For more on guarding, see セクション 7.1.2.

The guard buffer is a rail-to-rail input and output amplifier with the same complementary input stage as the OPA928. Like all rail-to-rail amplifiers, the guard buffer output cannot swing all the way to the rail by a few millivolts. This is particularly important in some special single-supply cases because the input bias performance of the OPA928 is sensitive to small differential voltages across the internal antiparallel diodes; see also セクション 7.1.3.

6.3.2 Input Protection

The OPA928 uses back-to-back, or antiparallel, input protection diodes to limit the input differential voltage and protect the device against transient currents. In most circuit applications, the input protection circuitry, illustrated in セクション 6.2, has no consequence. However, the antiparallel diodes can be forward biased by fast transient step responses as the amplifier cannot respond fast enough to the input signal. The aforementioned condition can cause relatively large amounts of current to flow through the inputs. Buffer configurations can be susceptible to this behavior in particular. If the input signal current is not inherently limited, an input series or feedback resistor can be used to limit the input current to below the absolute maximum. This additional resistor can degrade the low-noise performance of the OPA928.

6.3.3 Thermal Protection

The internal power dissipation of any amplifier causes the junction temperature (T_J) to rise. This phenomenon is called *self heating*. To prevent damage from overheating, the OPA928 has a thermal protection feature.

This thermal protection works by monitoring the temperature of the output stage and turning off the op amp output drive for temperatures above approximately 180°C. Thermal protection forces the output to a high-impedance state. The OPA928 is also designed with approximately 30°C of thermal hysteresis. The OPA928 returns to normal operation when the output stage temperature reaches a safe operating temperature of approximately 150°C.

6.3.4 Capacitive Load and Stability

The OPA928 features a patented output stage capable of driving large capacitive loads. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads. The particular op-amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier can be stable in operation.

For additional drive capability, insert a small isolation resistor (R_{ISO}) in series with the output; 図 6-1 shows this resistor. This resistor significantly reduces ringing while maintaining dc performance for purely capacitive loads. However, if there is a resistive load in parallel with the capacitive load, a voltage divider is created, introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_{ISO} / R_L, and is generally negligible at low output levels. R_{ISO} modifies the open-loop gain of the system for increased phase margin.

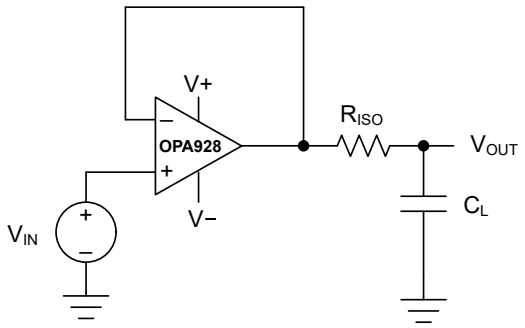


図 6-1. Extending Capacitive Load Drive With the OPA928

6.3.5 EMI Rejection

The OPA928 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. The OPA928 features improved design techniques to enhance EMI immunity.図 6-2 shows the tests results of the OPA928 over a broad frequency spectrum. Additional shielding further reduces the effects of EMI; see also セクション 7.1.6.

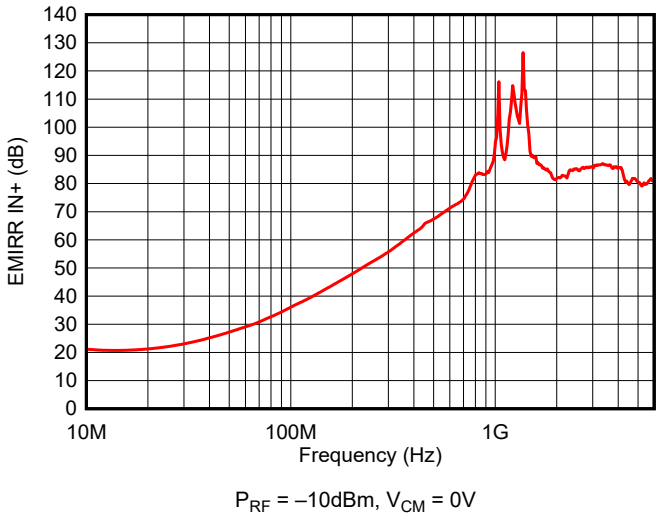


図 6-2. EMIRR Testing

For more information on EMI, see the *EMI Rejection Ratio of Operational Amplifiers* application report.

6.3.6 Common-Mode Voltage Range

The OPA928 is a 36V, rail-to-rail input and output op amp with an input common-mode range that extends 100mV beyond either supply rail. This wide range is achieved with paralleled complementary N-channel and P-channel differential input pairs. There is a small transition region, typically (V+) –3V to (V+) – 1.5V in which both input pairs are active and offset voltage and distortion performance can be degraded. The input bias performance is virtually unaffected in this region, but is subject to temperature variation. In inverting configurations, such as transimpedance applications, the input common-mode voltage is fixed and the transition region is easily avoided. In a buffer application, the small degradation of input offset performance in the transition region presents a negligible effect on the signal. In high, noninverting gain configurations, the common-mode voltage is limited to a small range and typically away from the transition region.

While the transition region is unlikely to affect most applications, there is an input common-mode limitation that directly affects the input bias current performance of the OPA928. Large input common-mode voltages can significantly degrade input bias current performance. If operating the device with a supply voltage greater than 20V, limit the input common-mode voltage to less than (V–) + 20V. See 図 5-23 to 図 5-28 for the recommended common-mode voltage range across different supply conditions.

6.4 Device Functional Modes

The OPA928 has a single functional mode and is operational when the power-supply voltage is greater than 4.5V (±2.25V). The operating power supply voltage for the OPA928 is 4.5V (±2.25V) to 36V (±18V).

The OPA928 provides an integrated buffer for guarding high impedance traces. Designers can choose to use the integrated guard buffer to drive guard traces or an external guard buffer. When an external guard driver is used, the internal guard buffer can be overdriven or left floating. For more details on guarding, see also セクション 7.1.2.

7 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Application Information

The OPA928 offers femtoampere level input bias current, and excellent dc precision and ac performance. This device provides 2.5MHz bandwidth and very low noise, 15nV/√Hz and 0.07fA/√Hz. The OPA928 can operate with a 36V supply and provides a wider linear output voltage swing than comparable op amps. The ultra-low input bias, low noise and wide output voltage swing capability make this device an excellent choice for high impedance buffer and transimpedance amplifier applications.

7.1.1 Contamination Considerations

Applications requiring femtoampere-level performance are extremely sensitive to contamination. Contaminants in the form of solder flux, salts, oils, organic acids, and more can form conductive paths over printed circuit board (PCB) traces and allow small currents to leak into input traces or other sensitive nodes, severely degrading performance. Proper handling and cleaning is required to achieve femtoampere level input bias performance in a PCB featuring the OPA928.

The following list of best practices helps prevent a PCB from contamination:

- Always wear a pair of clean, powder-free gloves or finger cots when handling the PCB.
- Always hold the PCB by the edges when handling is required.
- Avoid touching the surface of the PCB and other component packages, especially near sensitive nodes or input traces.
- Be cautious when breathing, speaking, and sneezing to prevent moisture or saliva from contacting the PCB.
- Do not allow direct airflow onto the board. Moving air can blow dust and moisture onto sensitive nodes. Airflow also introduces moving charges that manifest as a small current at the input.
- When not in use, place the PCB in an ESD bag or other enclosure to prevent dust and other contaminants from settling on the board.
- If configuring through-hole components in sensitive nodes, handle the components by the wire leads only.

A rigorous cleaning protocol is required after PCB assembly to remove all contaminants that can degrade input bias performance of the OPA928. Repeat the cleaning procedure any time the board is soldered or modified near sensitive nodes, or if contamination of these nodes is suspected.

7.1.2 Guarding Considerations

This section explores considerations for driving the printed circuit board (PCB) guard with the OPA928 internal guard buffer, an external guard driver, or by connecting the guard copper directly to the analog ground. For details on how to implement a guard in PCB layout, see also セクション 7.4.1

図 7-1 shows the equivalent schematic of the OPA928 internal guard buffer driving the PCB guard, including the PCB parasitic leakage paths. The guard presents a low-impedance path of near equal potential to the high-impedance input. Parasitic leakage currents that can flow into the high-impedance traces are rerouted through the low-impedance guard. The near equal potential between the input and guard traces makes the current flowing between the two nodes insignificant and the input trace is protected from the undesired leakage current. For a noninverting configuration, the input common-mode voltage changes with the input signal and the guard must be actively driven by a voltage follower that tracks the input signal. The OPA928 features a high-performance internal guard buffer that can be accessed at pin 2 and pin 7 to drive the PCB guard copper; see the *Electrical Characteristics* for specified guard buffer performance. The internal guard buffer tracks the voltage of the OPA928 input signal and is isolated from capacitive loads through a 1kΩ isolation resistor, R_{ISO}.

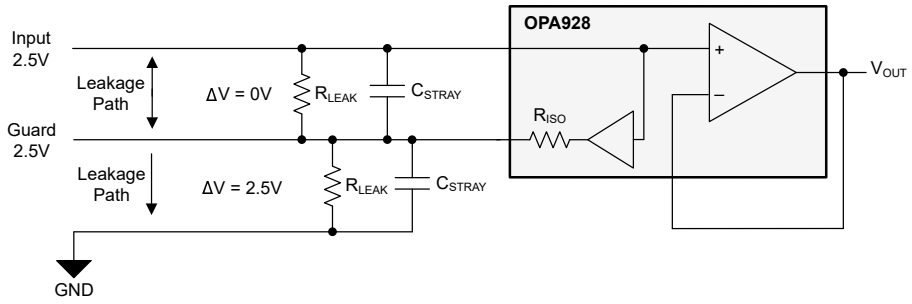


図 7-1. Driving the Guard, Internal Guard Buffer

図 7-2 shows how the PCB guard is driven with an external guard driver instead of the OPA928 internal guard buffer. To prevent the input bias current of the external guard driver from degrading the input signal, track the low-impedance input of the OPA928. If an external guard driver is used, the OPA928 guard pins can be left unconnected or can be overdriven by the external guard driver. Choose a low-offset, low-noise amplifier for the guard driver because any voltage potential between guard and input traces causes current to leak through the high-impedance trace. Include an isolation resistor at the output of the guard driver to prevent gain peaking due to capacitive loading and to provide short-circuit protection. Confirm that the guard driver is stable and capable of driving the capacitive load presented by the guard, including long cable lengths, if applicable.

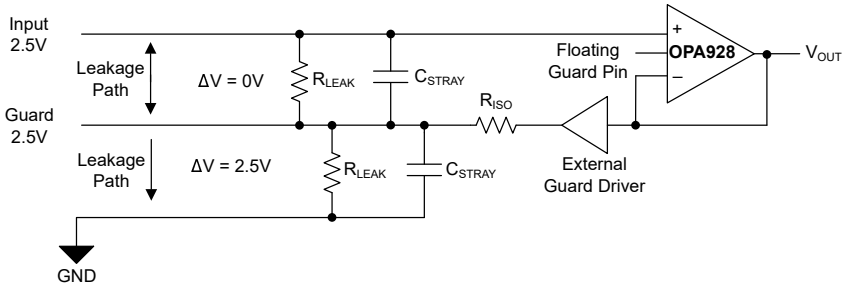


図 7-2. Driving the Guard, External Guard Driver

For inverting configurations, the input common-mode voltage is fixed to the analog ground or some dc reference voltage applied to the noninverting input. In this case, the PCB guard can be tied directly to ground or low-impedance reference of the signal amplifier. Connecting the PCB guard to a low-impedance reference or ground makes sure that the guard potential is always equal to the input common-mode voltage, without the additional offset and noise of an active guard driver. If the PCB guard is connected to the analog ground of the circuit,

make sure that current return paths do not cross through the guard area. Keep power and digital grounds separate from the guard and prevent ground loops from occurring.

7.1.3 Single-Supply Considerations

Some applications require consideration of the limitations of the guard buffer output swing. One such application is the single-supply inverting amplifier with a common-mode voltage equal to the rail, most commonly ground. The guard buffer cannot drive the guard all the way to the rail. The internal guard buffer features a rail-to-rail output stage and is capable of driving the guard to within 15mV of the rail. The small voltage difference manifests as a differential voltage across the antiparallel diodes as shown in 図 7-3. Even a small differential voltage of 15mV can cause a significant amount of leakage through the diodes at high temperatures.

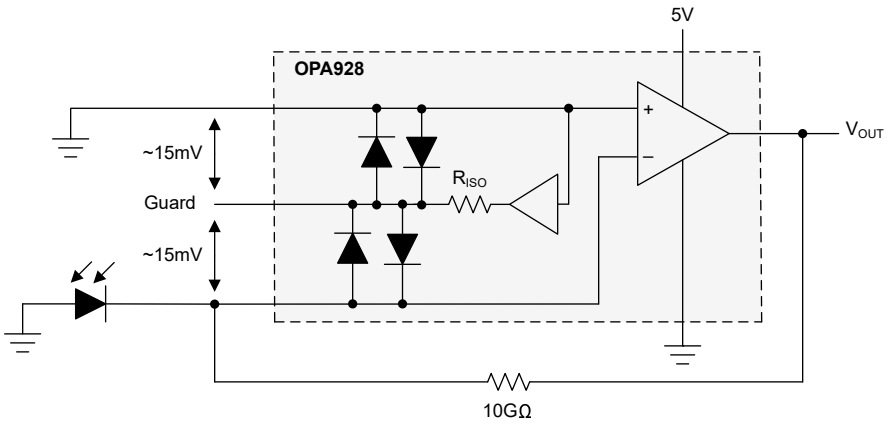


図 7-3. Single-Supply Transimpedance Amplifier

To avoid the input common-mode limitation of the guard buffer in inverting configurations with zero-common mode voltage, connect the guard pins directly to ground as done in 図 7-4.

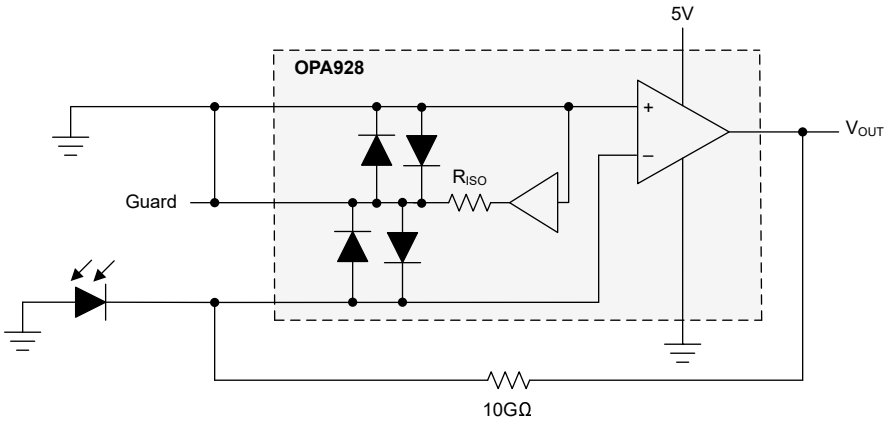


図 7-4. Single-Supply Transimpedance Amplifier With Grounded Guard Pin

図 7-5 shows the input bias current performance of the OPA928 near the negative rail when the guard pins are left floating compared to when the guard pins are tied to ground.

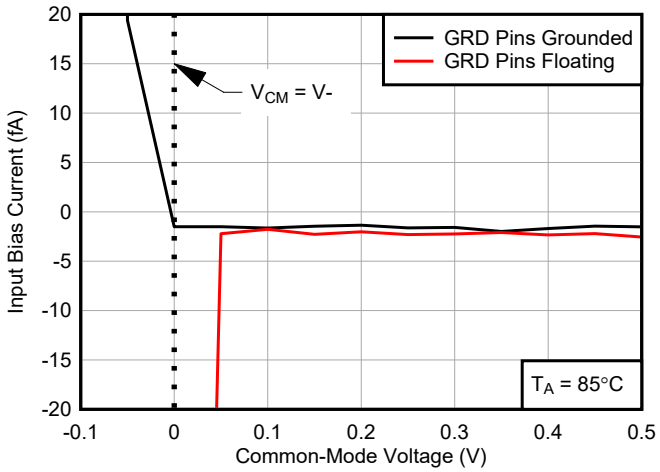


図 7-5. Input Bias Current Near the Negative Rail in Single Supply Applications

Noninverting, high-gain configurations can be susceptible to similar limitations. The limitation occurs when the input signal is less than the specified output swing of the guard buffer. To circumvent this issue, consider using dual supplies.

7.1.4 Humidity Considerations

The resistance of insulators is substantially affected by both temperature and humidity. Humidity can significantly lower the effective resistance of insulators and cause an increase in leakage current around the affected material. When water molecules settle on the surface of a given material, such as the plastic packaging and PCB, a parallel conductive path is created. Effective guarding techniques can help mitigate this behavior in sensitive applications.

In some cases, water molecules can also penetrate the surface of a given material. The water molecules in the material increase the conductivity of the body of the material and a reduction of resistance is established across all adjacent nodes. Contrary to surface level leakage paths, leakage through the material cannot be mitigated with guarding techniques. Use PCB materials with low humidity absorption properties to reduce moisture related errors.

図 7-6 shows the input bias performance of the OPA928 across temperature under different levels of humidity. Relative humidity is inversely proportional to temperature. The temperature range for high relative humidity levels is limited to maintain reliable measurements.

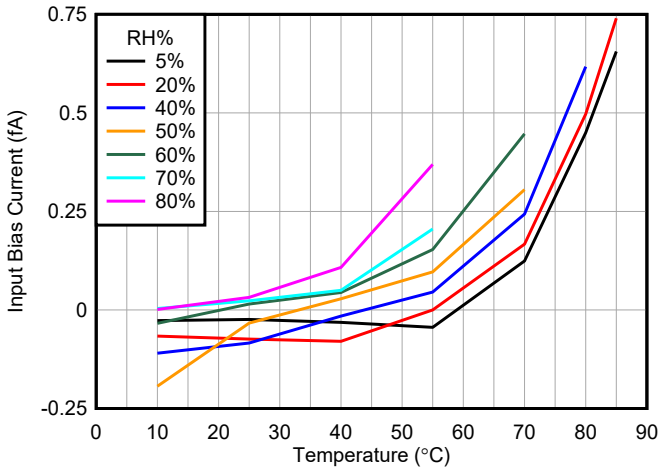


図 7-6. Input Bias Current vs Temperature at Various Levels of Relative Humidity

The measurements were made using a calibrated humidity chamber and an air wired circuit. Although air wiring the input pins eliminates many potential leakage paths, the feedback components remain sensitive to large changes in relative humidity. External components are typically the dominant source of leakage current when compared to the input bias current of the OPA928. To achieve outstanding input bias current performance, use low leakage components such as PTFE or polypropylene capacitors.

Moisture absorption and desorption is a strong function of both time and temperature. Baking is demonstrated to be an effective method of removing excess moisture. Baking time depends on several variables, including PCB and component material and bake temperature. If a baking procedure is implemented, a one-hour bake at 125°C is a good starting point.

7.1.5 Dielectric Relaxation

All materials are prone to polarization in the presence of an electric field. The molecules of the given material within the electric field become aligned at varying rates; a phenomena known as polarization. The rate depends on the strength of the electric field and the susceptibility of the material. When the electric field is removed, the molecules in the material return to the original alignment and random distribution, a phenomena known as relaxation. The rate at which the molecules return to normal alignment depends on the permittivity and resistivity of the material. In conductors, polarization and relaxation happens nearly instantaneously. In dielectrics, the time delay for polarization and relaxation can be significant.

In most applications, dielectric relaxation is not a major design concern. However, for femtoampere leakage current, dielectric relaxation becomes a major concern. The realignment of molecules causes a small displacement current to appear across the material. The displacement current from the dielectric relaxation is often greater than the input bias current level of the OPA928. The time required for the displacement current in common FR-4 PCB materials to dissipate under the input bias current level of the OPA928 can take well over an hour. The ingression of moisture into the dielectric material can significantly increase the relaxation time. To minimize the dielectric relaxation time and the leakage effects, use ceramic-based PCB materials such as Rogers 4350B and consider implementing a baking process to remove excess moisture.

7.1.6 Shielding

High-impedance, femtoampere-level circuits are highly sensitive to electrostatic and electromagnetic interference (EMI). Even weak electric fields can couple into high-impedance nodes and cause significant interference when in close proximity to the circuit. Simply waving your hand near the test fixture, for example, can disrupt the low leakage measurement. To help reduce the effects of electrostatic and electromagnetic fields, fully enclose all exposed high-impedance traces with a shield. The shield serves to reduce external dc and ac signals from coupling into the high-impedance nodes by shunting the signals to analog ground. Keep the shield installed to reduce unwanted pickup and prevent contaminants from entering sensitive nodes. Shield cans and surface mount shield clips are readily available from manufactures.

7.2 Typical Applications

7.2.1 High-Impedance Amplifier

The OPA928 behaves very close to an ideal op amp in regards to the input current. The near-zero input bias current performance enables applications with extremely high impedance signal sources. For example, pH probes can have an output impedance of up to 10GΩ. Most op amps are inadequate to use with this kind of sensor impedance. For example, a CMOS op amp with 1pA of input bias current loads the sensor and causes a large, and unacceptable, 10mV error at the input at room temperature. This error can increase exponentially across the industrial temperature range. In 図 7-7, the OPA928 is used as a high-impedance electrometer to amplify the small signal from the pH probe sensor. The high input impedance and ultra-low bias current into the positive input pin of the OPA928 does not load the sensor and minimizes the input bias current error.

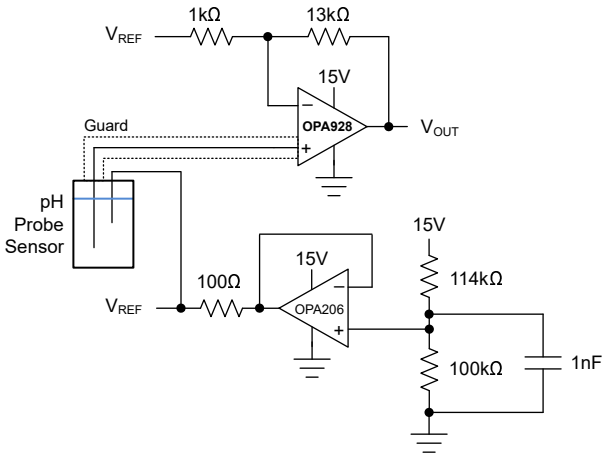


図 7-7. High Impedance pH Probe Amplifier Circuit

7.2.1.1 Design Requirements

The primary objective is to design a single-supply, pH-probe gain amplifier.

- Supply voltage: 15V
- pH-probe sensor impedance: 10GΩ
- pH-probe sensor slope: 59mV/pH at 25ºC
- Temperature range: 25ºC to 85ºC

7.2.1.2 Detailed Design Procedure

According to the NERNST Equation, the pH probe sensor produces an output of ±59mV/pH at room temperature, or 25°C, and ±71mV/pH at 85°C. 図 7-8 shows how the pH probe can be modeled as a small, variable battery in series with a 10GΩ resistor. The probe impedance can vary significantly with temperature. As a result of the intrinsic characteristics of the pH probe, a near 0V output is produced for a neutral pH value of 7, but a ±30mV offset is common. This offset can be easily calibrated to 0V. The slope is given in manufacture data sheets, but a 2-point calibration can be done using a pH 4 or pH 10 buffer solution to confirm the probe is working properly.

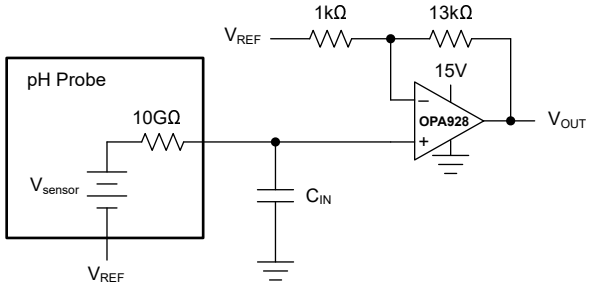


図 7-8. pH Probe Simplified Model

A gain of 14V/V provides a wide output swing of approximately ±7V. To enable single-supply operation, a 7V reference voltage (V_{REF}) is created using the 15V supply voltage and a simple voltage divider. The output swing is shifted to 0V to 14V, and is conveniently proportional to the approximately ±1V/pH at 85°C. 図 7-9 shows the resulting output voltage based on the theoretical pH sensor signal. In practice, pH probes show significant nonlinearity for very acidic and alkaline media; therefore, the measurement in 図 7-9 is constrained to ±400mV. Temperature calibration of the pH sensor (not shown) is necessary for accurate results when wide temperature variation is expected.

7.2.1.3 Application Curve

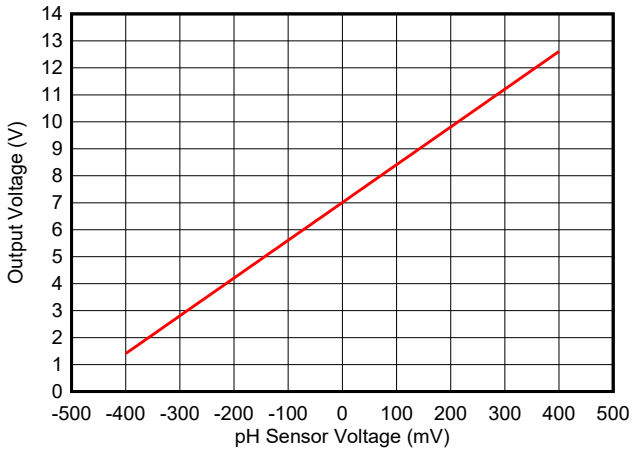


図 7-9. Single Supply, pH-Probe Sensor Transfer Function

7.2.2 Transimpedance Amplifier

図 7-10 shows the OPA928 configured as a transimpedance amplifier (TIA) for a low-light photodiode. TIAs are needed to amplify the light-dependent current of the photodiode. In low-light conditions, photodiodes produce a very small current and ultra-low input bias current and large gain in excess of 10^9V/A is required.

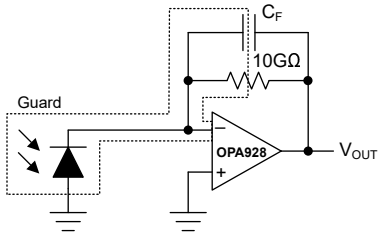


図 7-10. Simplified Photodiode Transimpedance Amplifier With the OPA928

7.2.2.1 Design Requirements

The design requirements for this design are:

- Transimpedance gain: 10,000,000,000A/V
- Supply voltage rail: 5V
- Photodiode shunt resistance: 5GΩ
- Photodiode shunt capacitance: 35pF

7.2.2.2 Detailed Design Procedure

Some photodiode applications operate in dark conditions and require low-light detection. In these cases, the current output from the photodiode can be miniscule. To make the small diode current measurable, a transimpedance amplifier (TIA) with a very large gain is required. The ideal transfer function of a resistive transimpedance amplifier is given by 式 1:

$$V_{OUT} = I_{PD} \times R_F \tag{1}$$

The photodiode current (I_{PD}) flows through the feedback resistor (R_F) and forces an output voltage (V_{OUT}) equal to the voltage drop across R_F. 式 1 gives an intuitive understanding of TIA operation. In practice, however, nonidealities must be taken into consideration to achieve the desired performance. 図 7-11 illustrates important nonidealities of the transimpedance amplifier circuit. The following sections describe how the op amp dc and ac performance interacts with the circuit.

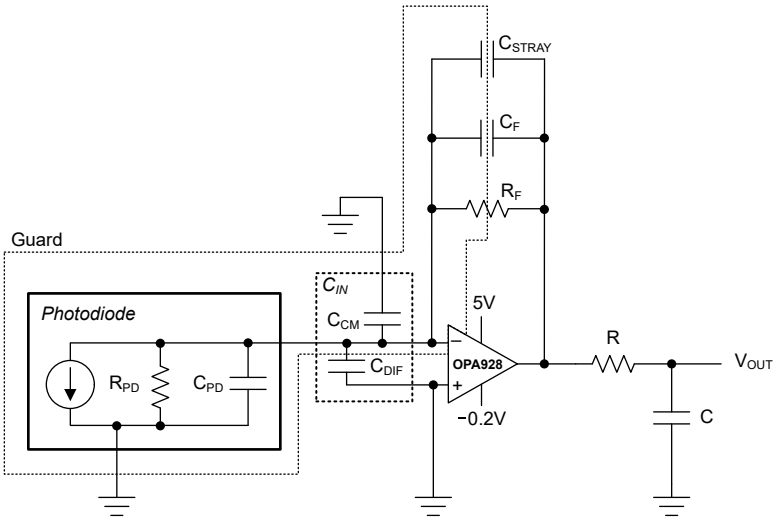


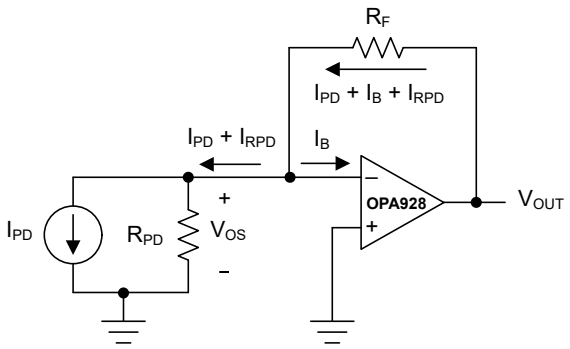
図 7-11. Transimpedance Photodiode Application

7.2.2.2.1 Input Bias

One very important consideration is the input bias current of the op amp. The input bias current directly adds to I_{PD} and creates an undesired error. The input bias current typically determines the minimum measurable I_{PD} within a given error tolerance. For example, a 1pA input bias current yields a 20% error when measuring a 5pA photodiode current. A 1% error target requires a 50fA input bias current maximum specification. Input bias current is strongly temperature dependent, and CMOS amplifier input bias current typically doubles for every 10°C increase of temperature. The OPA928 input bias current is tested to be less than 20fA at 85°C. The ultra-low input bias current of the OPA928 enables accurate, extremely low I_{PD} measurements across a wide temperature range. For information on how to maintain the specified input bias performance, see セクション 7.4.

7.2.2.2.2 Offset Voltage

The input offset voltage (V_{OS}) of the op amp is another significant source of error. The input offset voltage forces a voltage across the effective shunt resistance of the diode (R_{PD}) and creates an error current (I_{RPD}) equal to V_{OS} / R_{PD} as illustrated in 図 7-12. The shunt resistance of the photodiode is commonly specified in the manufacturer's data sheet. In some cases, V_{OS} can be the dominant source of error. For example, a V_{OS} of 50µV and an R_{PD} of 1GΩ creates an I_{RPD} of 50fA, which is more than double the maximum leakage current of the OPA928. Consider offset voltage variation with temperature and common-mode voltage.



$$V_{OUT} = I_{PD}R_F + I_BR_F + V_{OS}(1+R_F / R_{PD})$$

図 7-12. Transimpedance Amplifier DC Model

7.2.2.2.3 Stability

High transimpedance gain applications require very large R_F to be used, which can give rise to potential stability problems. R_F interacts with the input capacitance (C_{IN}) of the op amp, the photodiode capacitance (C_{PD}), and stray PCB capacitance to create a low-frequency zero (f_Z) in the noise gain transfer function (1/β) as illustrated in 図 7-13. Remember that C_{IN} includes the differential (C_{DF}) and common-mode (C_{CM}) capacitance of the op amp. The typical value of C_{DF} and C_{CM} are found in the *Electrical Characteristics*. The zero in 1/β causes the gain to increase over frequency and is the basis for instability problems. To counteract the zero, add a compensation capacitor (C_F) in the feedback loop to create a pole (f_P). Increasingly, larger R_F requires a decreasingly lower capacitor to remain stable. In some cases, parasitic capacitance from the resistor and PCB layout can alone be sufficient to maintain stability.

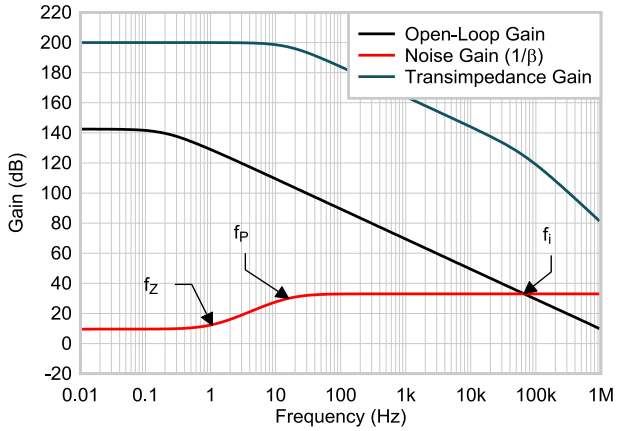


図 7-13. Transimpedance Amplifier Noise Gain

The optimized selection of C_F depends on several parameters and extensive literature exists on this topic. 式 2 provides a good starting point for the selection of C_F.

$$C_F = \frac{1 \pm \sqrt{1 + 8\pi GBWR_F(C_{IN} + C_{PD})}}{4\pi GBWR_F} \quad (2)$$

Increasing the value of C_F yields a higher phase margin and limits the peaking response at the expense of signal bandwidth. The bandwidth of the transimpedance amplifier is given by 式 3. Large R_F significantly limit the achievable bandwidth of the circuit. A compromise between gain, bandwidth, and stability can be made according to the specific requirements.

$$f_{-3dB} = \frac{1}{2\pi R_F C_F} \quad (3)$$

7.2.2.2.4 Noise

There are three primary sources of noise to consider in transimpedance amplifiers: the feedback resistor, the op amp (with both current and voltage noise), and the photodiode.

All resistors are sources of thermal noise and the feedback resistor contributes to the total noise of the circuit. In very high transimpedance gain configurations, the photodiode shunt resistance can have a significant affect on the total noise of the circuit. 式 4 shows the input-referred resistor noise density equation, which can be simplified to show that the input-referred resistor noise of the transimpedance amplifier is given by the thermal noise of R_F divided by the square root of the noise gain. The output-referred resistor noise is given by multiplying 式 4 by the noise gain. Thus, the output-referred resistor noise increases with the square root of the noise gain and the square root of the resistor value, while the signal gain increases directly with the resistor value. Therefore, increasing R_F provides a signal-to-noise ratio benefit as long as the current noise does not become a dominant source of noise.

$$e_{n\_R} = \sqrt{4kTR_F\left(\frac{R_{PD}}{R_{PD} + R_F}\right)} \tag{4}$$

図 7-14 shows the output voltage noise of OPA928 in a transimpedance amplifier configuration with R_F = 1TΩ and C_F = 0.15pF. The OPA928 current noise does not significantly contribute to the noise performance of the transimpedance amplifier.

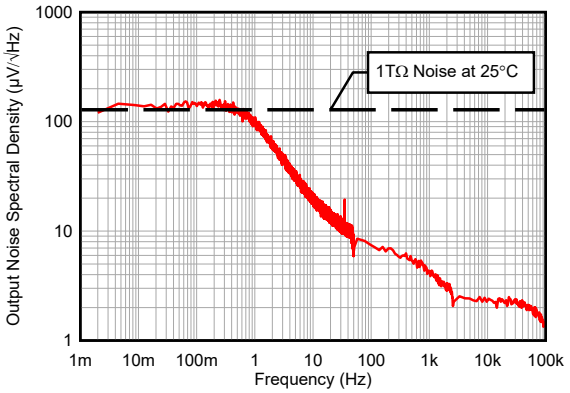


図 7-14. OPA928 Transimpedance Amplifier Output Voltage Noise With a 1TΩ Resistor

Comparing the input current noise of the OPA928 to the current noise of R_F can be useful to find the dominant noise source. A 1TΩ resistor, for example, is equivalent to 0.1287fA/√Hz of current noise which is well above the measured 0.07fA/√Hz of the OPA928. The OPA928 current noise is equivalent to a 3.34TΩ resistor. For more information on current noise, see the Impact of Current Noise in CMOS and JFET Amplifiers application report.

The total output-referred noise of the transimpedance amplifier is given by 式 5, where e_n is the amplifier voltage noise (including the 1/f and broadband regions), i_n is the amplifier current noise, i_{pd} is the photodiode current noise, f_{-3dB} is the transimpedance bandwidth, G is the dc noise gain, and G(f) is the frequency dependent noise gain.

$$E_{n\_total} = \sqrt{\int_{f_l}^{f_h}(e_nG(f))^2 df + \left[(i_nR_F)^2 + (i_{pd}R_F)^2 + 4kTR_FG\right] \times 1.57f_{-3dB}} \tag{5}$$

The total output-referred voltage noise calculation requires a complicated analysis of the frequency dependent noise gain and voltage noise density, and is not covered here. Unlike the current and resistor noise which are bandwidth limited by the transimpedance bandwidth given by 式 3, the op amp voltage noise is only limited by the gain bandwidth of the amplifier. Limit the noise bandwidth with an output filter to reduce the voltage noise contribution.

The ultra-low current noise of the OPA928 is not a significant contributor of noise in most applications, and an output low-pass filter makes the e_n term in 式 5 negligible. 式 6 provides a straight-forward calculation for the total output-referred noise for a filtered transimpedance amplifier.

$$E_{n\_total} = \sqrt{\left[\left(i_{pd}R_F\right)^2 + 4kTR_FG\right] \times 1.57f_{-3dB}} \quad (6)$$

図 7-15 shows the simulated noise of the OPA928 in a transimpedance configuration with R_F = 10GΩ, R_{PD} = 5GΩ, C_F = 1pF, C_{PD} = 35pF.

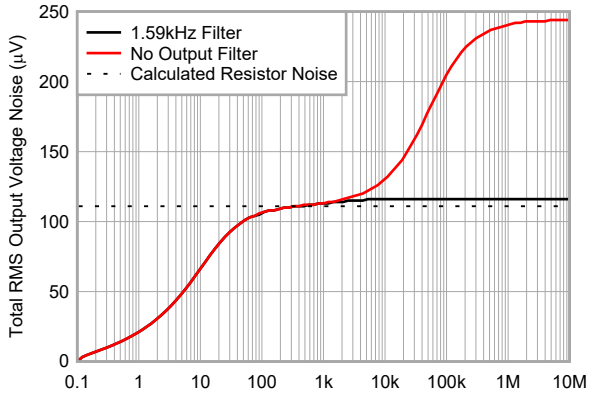


図 7-15. Transimpedance Amplifier RC-Filter Noise Comparison

7.2.3 Improved Diode Limiter

Low leakage current designs require special considerations. As described in セクション 7.1.5, polarization of dielectric material and capacitors can have severe adverse effects on low leakage measurements. Even small electric potentials can polarize dielectrics enough to result in residual leakage current greater than the input bias current of the OPA928. Depending on the severity, the dielectric relaxation of insulators and dielectric absorption of capacitance at the input can make measurements unreliable for a prolonged time period.

Dielectric polarization can be created unintentionally in some common applications. In particular, the transimpedance amplifier configuration is prone to dielectric polarization. The dynamic range of interfacing sensors can vary widely, and a current input beyond the expected range can cause the output to slam to the supply rail. When the output is slammed, the amplifier is unable to maintain a virtual short and the high impedance node voltage increases significantly. The voltage increase not only causes current flow into the input, but also polarizes the material enough to create dielectric relaxation related leakage.

A diode clamp in the feedback path can be used to limit the output voltage swing and prevent the op amp from saturating. The leakage from the diode, however, can be quite large and is unusable in low leakage circuits. A better design can be made using the internal guard buffer of the OPA928. A Zener diode can be connected from the output to the guard, bypassing the high impedance node altogether as shown in 図 7-16.

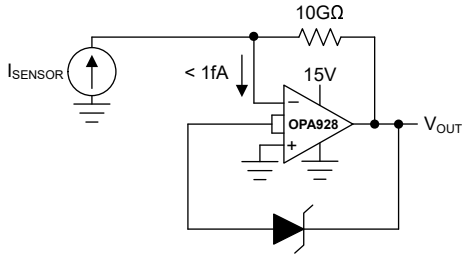


図 7-16. Improved Diode Limiter

During normal operation, the small leakage current from the Zener diode, $I_{Leakage}$, is handled by the internal guard buffer as shown in 図 7-17. In the overrange condition shown in 図 7-18, the Zener diode begins to conduct more current, I_R, and creates a voltage drop of across the 1kΩ resistor. The voltage that develops at the guard pin causes the internal protection diodes to conduct and source the remaining sensor current, I_{SENSOR}. The guarded diode limiter circuit regulates the voltage at the inverting node even during an overrange condition.

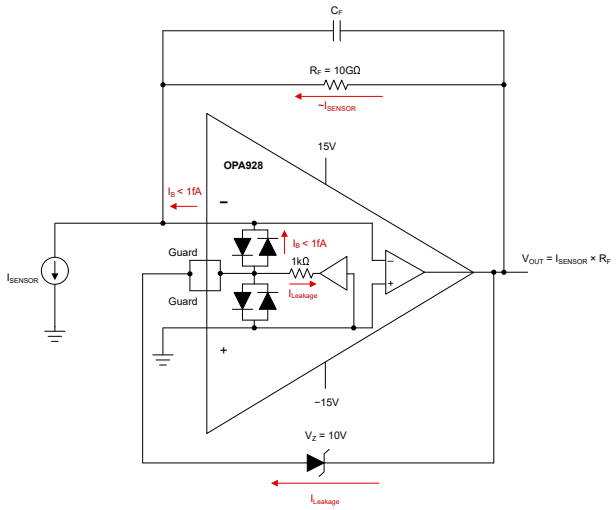


図 7-17. Guarded Diode Limiter During Normal Operation

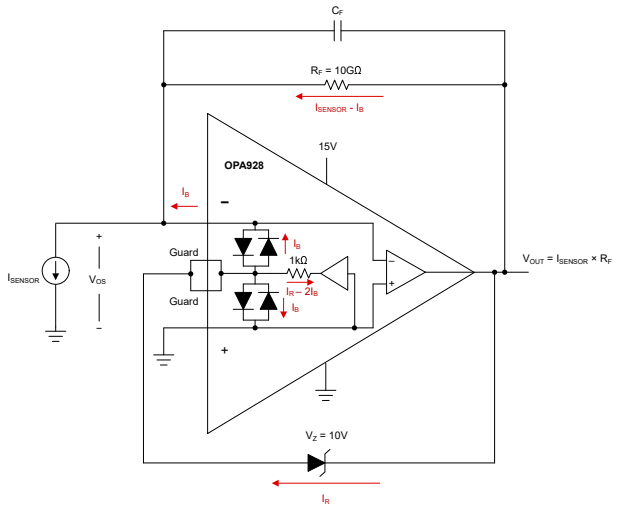


図 7-18. Guarded Diode Limiter During Overrange

7.2.4 Instrumentation Amplifier

Some applications require a differential signal measurement with very high input impedance. In such cases, an instrumentation amplifier is used. A high performance instrumentation amplifier can be built using the OPA928 and the RES11A series of matched resistor pairs. 図 7-19 enables a very high impedance, differential measurement with a gain of 10V/V.

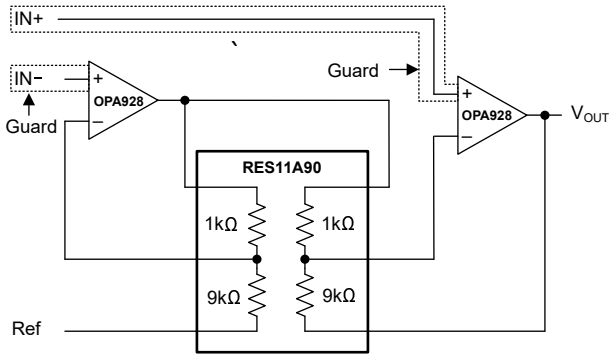


図 7-19. Two Op Amp Instrumentation Amplifier

To achieve higher common-mode rejection ratio, a three op amp instrumentation amplifier can be implemented with an additional op amp and RES11A. 図 7-20 shows a high CMRR, very high input impedance, instrumentation amplifier.

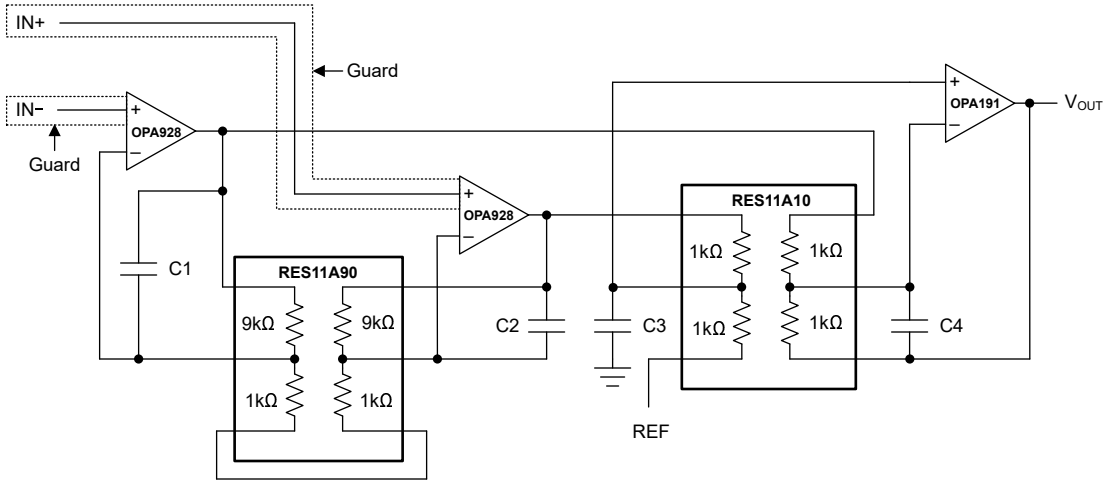


図 7-20. Three Op Amp Instrumentation Amplifier

7.3 Power-Supply Recommendations

The OPA928 is specified for operation from 4.5V to 36 (±2.25V to ±18V). The OPA928 features a high power-supply rejection ratio (PSRR) and significantly reduces power supply errors at dc. However, a decreasing PSRR at high frequencies means that high-frequency components in the power supply, such as noise, can be coupled to the output. Use a linear, low-noise power supply to optimize noise performance. Place 0.1µF bypass capacitors close to the power-supply pins to further reduce errors coupling in from the power supplies. For more detailed information on bypass capacitor placement, see セクション 7.4. Switching power supplies generate switching noise that can manifest at the output of the OPA928. When switching power supplies cannot be avoided, use proper filtering and a low-dropout regulator to attenuate the switching noise and respective harmonics to an acceptable level.

7.4 Layout

7.4.1 Layout Guidelines

For best operational performance of the device, follow PCB layout best practices, including:

- Connect 0.1µF ceramic bypass capacitors with low equivalent series resistance (ESR) between each supply pin and ground. Place the capacitors as close to the device as possible. For single-supply applications, use a single bypass capacitor from V+ to ground. Bypass capacitors are used to reduce coupled noise by providing low-impedance power sources local to the analog circuitry.
- Physically separate digital and analog grounds, paying attention to the flow of the ground current. Separate grounding for analog and digital circuitry is one of the simplest and most effective methods for noise suppression. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup.
- Place external components as close to the device as possible.
- Keep the length of input traces as short as possible. Input traces are the most sensitive part of the circuit.

In addition to general PCB layout considerations, specific layout techniques must be implemented to achieve femtoampere-level input bias current. Every insulator, including PCB material, has a finite resistance that can become a path for current to leak into input traces and degrade input bias performance. To minimize leakage current paths, implement a guard in the PCB layout. The guard presents a low-impedance path equipotential to the input traces. Leakage current toward the high impedance input path can be diverted to the low-impedance guard path. Current flowing between the input and guard traces is negligible because both traces are at the same potential. See also セクション 7.1.2.

Surround all high-impedance input traces with copper guard traces all the way from the source to the input pins of the OPA928. For inverting configurations, extend the guard copper to the middle of the feedback components, separating the low-impedance output from the high-impedance input node. Remove all solder mask and silkscreen from the guard area to reduce surface-charge accumulation and prevent surface-level leakage paths to the input.

Leakage currents can flow between layers vertically or diagonally through the PCB, as well as horizontally on the surface layer. The guard must be implemented in a three-dimensional scheme to prevent leakage currents originating in other layers from flowing into the signal path. Place the guard copper on the next layer directly below the surface-level signal and guard traces to protect from vertical leakage paths. Surround the sensitive input traces with a via fence connecting the guard copper on different layers to complete the three-dimensional guard enclosure. 図 7-23 shows the internal copper layers of a four-layer PCB using a three-dimensional guarding scheme.

A copper ground pour around the OPA928 and guard area is recommended to reduce noise and EMI. In addition to noise and EMI benefits, this ground pour presents another low-impedance path for leakage currents to take. Keep voltage potentials other than guard and ground as far as possible from sensitive nodes. The OPA928 SOIC pinout places the input and power supply pins at opposite ends of the amplifier package to reduce leakage currents across the package and PCB material. If the power supplies (or other voltages) are present in vias or through-holes near the OPA928, a ground-potential via fence can be applied locally to these through-holes to provide a low-impedance path for leakage currents in the direction of sensitive nodes.

High-impedance, femtoampere-level circuits are highly sensitive to EMI. Ground planes and ground pours in the PCB layout can help reduce the effects of EMI. During operation, a femtoampere-level PCB is commonly placed within a shielded enclosure tied to ground for further EMI rejection. In layout, consider enclosing the OPA928 and all high-impedance traces within a local grounded RF shield. An example of localized RF shielding for high-impedance nodes is available in the OPA928 Evaluation Module User's Guide.

7.4.2 Layout Examples

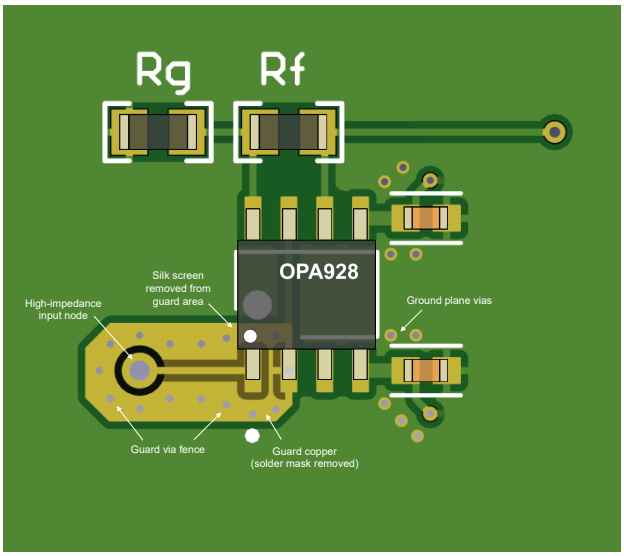


図 7-21. Layout Example: Noninverting Configuration

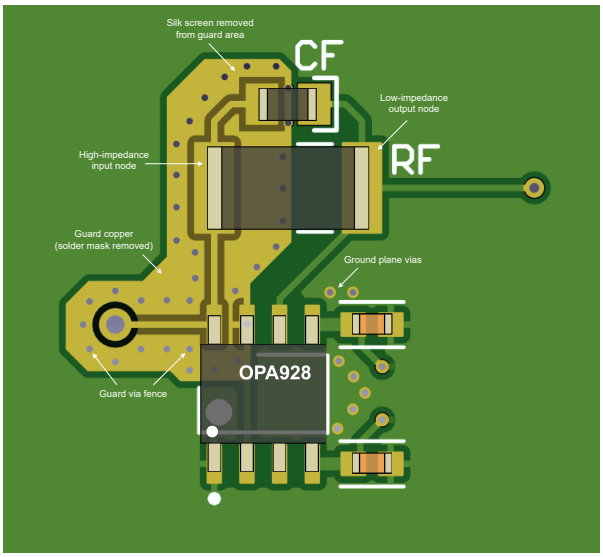


図 7-22. Layout Example: Inverting Configuration

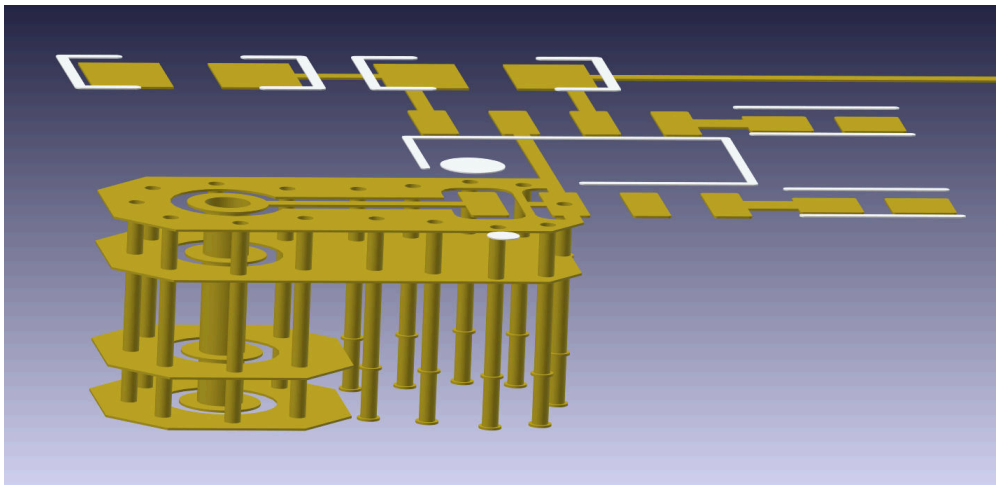


図 7-23. Layout Example: Three-Dimensional Guard (4-Layer PCB)

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 PSpice® for TI

PSpice® for TI は、アナログ回路の性能評価に役立つ設計およびシミュレーション環境です。レイアウトと製造に移る前に、サブシステムの設計とプロトタイプ・ソリューションを作成することで、開発コストを削減し、市場投入までの期間を短縮できます。

8.1.1.2 TINA-TI™シミュレーション・ソフトウェア (無償ダウンロード)

TINA-TI™ シミュレーション・ソフトウェアは、SPICE エンジンをベースにした単純かつ強力な、使いやすい回路シミュレーション・プログラムです。TINA-TI シミュレーション・ソフトウェアは、TINA™ ソフトウェアのすべての機能を持つ無償バージョンで、パッシブ・モデルとアクティブ・モデルに加えて、マクロモデルのライブラリがプリロードされています。TINA-TI シミュレーション・ソフトウェアには、SPICE の標準的な DC 解析、過渡解析、周波数ドメイン解析などの全機能に加え、追加の設計機能が搭載されています。

TINA-TI シミュレーション・ソフトウェアは設計ツールとシミュレーション Web ページから無料でダウンロードでき、ユーザーが結果をさまざまな方法でフォーマットできる、広範な後処理機能を備えています。仮想計測器により、入力波形を選択し、回路ノード、電圧、および波形をプローブして、動的なクイック・スタート・ツールを作成できます。

注

これらのファイルを使用するには、TINA ソフトウェアまたは TINA-TI ソフトウェアがインストールされている必要があります。TINA-TI™ ソフトウェア・フォルダから、無償の TINA-TI シミュレーション・ソフトウェアをダウンロードしてください。

8.1.1.3 TI のリファレンス・デザイン

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8.2 Documentation Support

8.2.1 Related Documentation

- Texas Instruments, *OPA928 Evaluation Module User's Guide*

8.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.4 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (March 2023) to Revision A (April 2024)	Page
• データシートのステータスを事前情報 (プレビュー) から量産データ (アクティブ) に変更	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA928DR	ACTIVE	SOIC	D	8	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	OPA928	Samples
OPA928DT	ACTIVE	SOIC	D	8	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	OPA928	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

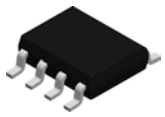
(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

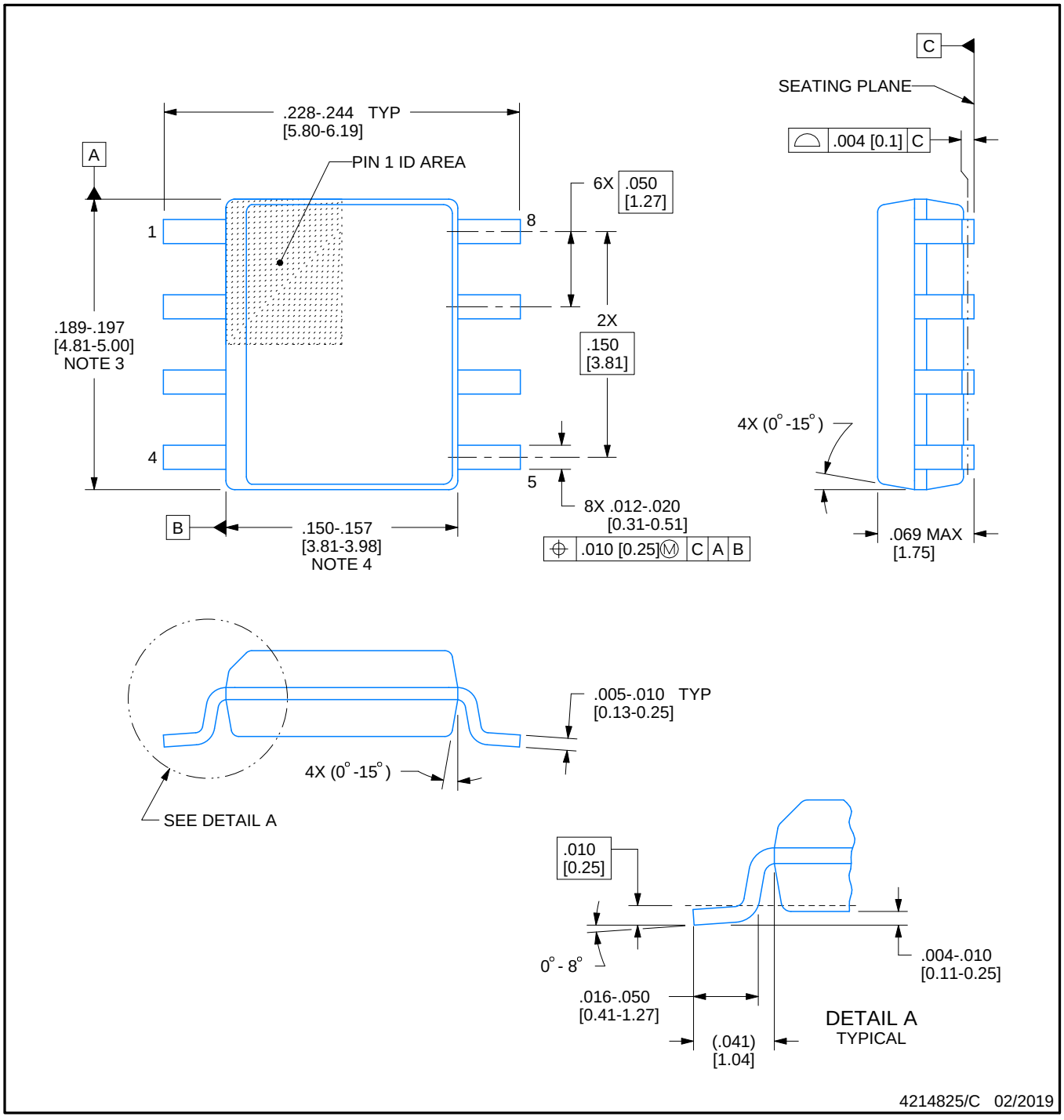


PACKAGE OUTLINE

D0008A

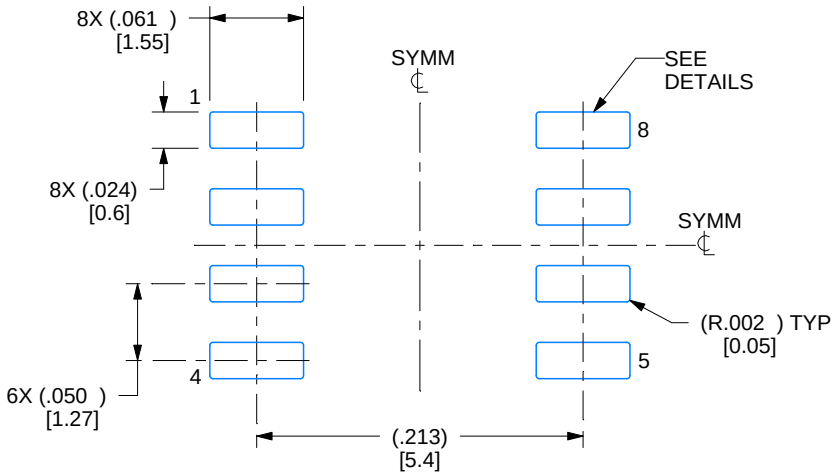
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

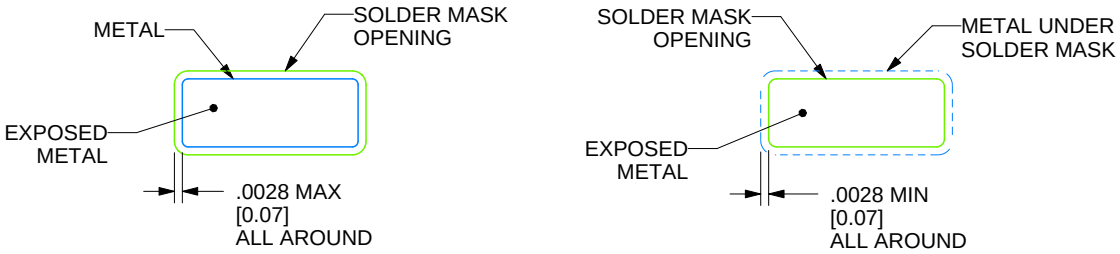


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

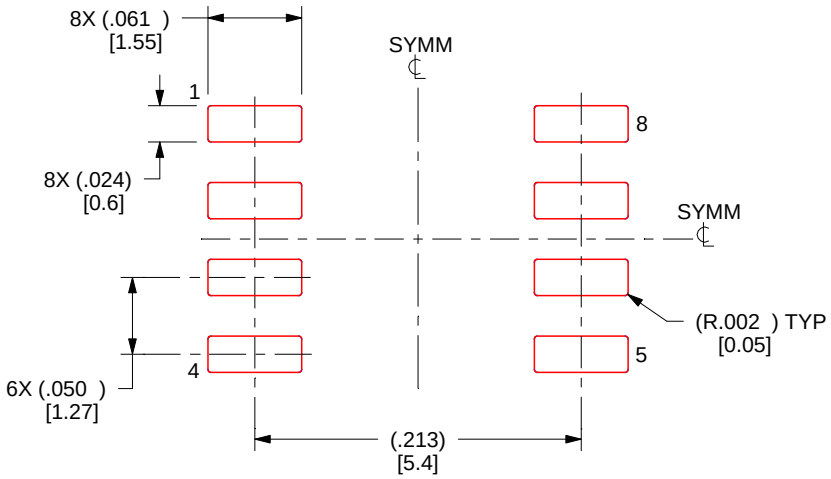
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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