TEXAS INSTRUMENTS
OPA2994-Q1
JAJSS74 – NOVEMBER 2023

# OPAx994-Q1 無制限の容量性負荷駆動付き、車載用、24V、レール ツー レール入出力、25MHz、150mA 出力電流、オペアンプ

## 1 特長

- 広い電源電圧範囲:2.7V～24V
- レール・ツー・レール入出力
- 広い帯域幅:25MHz GBW、ユニティ・ゲイン安定
- 無制限の容量性負荷駆動能力:
  - 10µF、1MΩ の負荷を駆動した場合の位相マージンは 60°
- 大出力電流の駆動:±150mA
- 低いオフセット電圧:±200µV (標準値)
- 低いオフセット電圧ドリフト:±0.17µV/°C (標準値)
- 低ノイズ:1kHz 時に 12nV/√Hz
- 高い同相信号除去比:135dB
- 高いスルーレート:18V/µs
- 低静止電流:アンプ 1 個あたり 1.25mA

## 2 アプリケーション

- AEC-Q100 グレード 1 アプリケーションに最適化
- HEV/EV のインバータおよびモータ制御
- HEV/EV の DC/DC コンバータ
- オンボード充電器 (OBC) およびワイヤレス充電器
- AC 充電 (パイル) ステーション
- GFCI 故障検出およびテスト
- ソフトウェア無線
- ハイサイドおよびローサイド電流検出

## 3 概要

OPAx994-Q1 ファミリ (OPA994-Q1 および OPA2994-Q1) は、高電圧 (24V) レール ツー レール入出力 (RRIO) オペアンプのファミリです。これらのデバイスは、25MHz の広いユニティ・ゲイン帯域幅と 18V/µs の高いスルーレートを含む優れた AC 性能を実現しながら、チャネルあたり 1.25mA の静止電流しか必要としません。

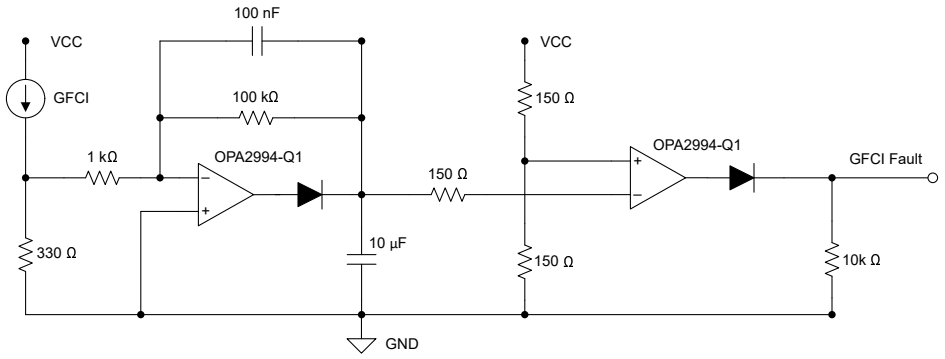
OPAx994-Q1 ファミリは、広範囲の容量性負荷にわたって安定性を維持するように設計されています。たとえば、OPAx994-Q1 は、1MΩ の負荷抵抗を使用して 10µF の大きな容量性負荷を駆動する場合、60 度の位相マージンを達成できます。OPAx994-Q1 は、大きな容量性負荷に対する持続的なリンギングを軽減する補償アーキテクチャを使用して設計されています。これにより、大規模な、変動する、または未知の容量性負荷を持つシステムに対して、信頼性の高い性能と容易な設計が可能になります。

また、これらのデバイスは、150mA/チャネルの高い短絡出力電流、低いオフセット電圧 (±200µV、標準値)、低いオフセットのドリフト (±0.17µV/°C、標準値)、メイン入力ペア内の高電圧動作に対する 135dB の高い CMRR など、優れた DC 精度を提供します。これにより、OPAx994-Q1 は高電圧車載アプリケーション向けの柔軟で堅牢な高性能オペアンプになっています。

### 製品情報

| 部品番号(1) | チャネル数 | パッケージ | パッケージ サイズ(3) |
|---|---|---|---|
| OPA994-Q1 | シングル | DBV (SOT-23、5)(2) | 2.90mm × 2.80mm |
| OPA2994-Q1 | デュアル | D (SOIC、8)(2) | 4.90mm × 6.00mm |
| | | DGK (VSSOP、8)(2) | 3.00mm × 4.90mm |

(1) 詳細については、セクション 10 を参照してください。
(2) このパッケージはプレビューのみです。
(3) パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。




**OPAx994-Q1 電気自動車サービス機器 (EVSE) 用漏電遮断器 (GFCI) フォルト検出およびテスト回路内で**

ADVANCE INFORMATION

# Table of Contents



ADVANCE INFORMATION

# 4 Pin Configuration and Functions

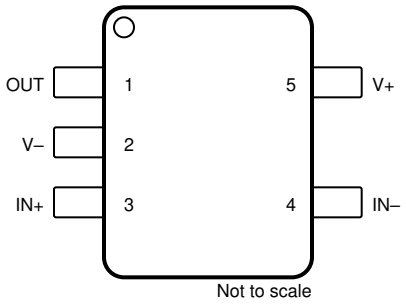



**図 4-1. OPA994-Q1 DBV Package, 5-Pin SOT-23 (Top View)**

**表 4-1. Pin Functions: OPA994-Q1**

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| IN+ | 3 | I | Noninverting input |
| IN– | 4 | I | Inverting input |
| OUT | 1 | O | Output |
| V+ | 5 | — | Positive (highest) power supply |
| V– | 2 | — | Negative (lowest) power supply |

(1) I = input, O = output

ADVANCE INFORMATION

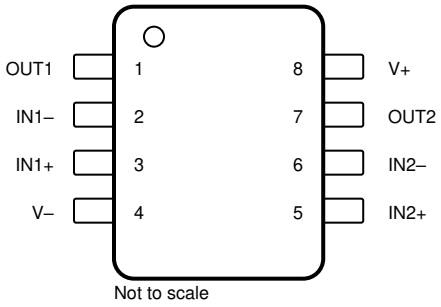



**図 4-2. OPA2994-Q1 D and DGK Package, 8-Pin SOIC and VSSOP (Top View)**

**表 4-2. Pin Functions: OPA2994-Q1**

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| IN1+ | 3 | I | Noninverting input, channel 1 |
| IN1– | 2 | I | Inverting input, channel 1 |
| IN2+ | 5 | I | Noninverting input, channel 2 |
| IN2– | 6 | I | Inverting input, channel 2 |
| OUT1 | 1 | O | Output, channel 1 |
| OUT2 | 7 | O | Output, channel 2 |
| V+ | 8 | — | Positive (highest) power supply |
| V– | 4 | — | Negative (lowest) power supply |

(1) I = input, O = output

ADVANCE INFORMATION

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_S$ = (V+) – (V–) | | 0 | 24 | V |
| Signal input pins | Common-mode voltage(3) | (V–) – 0.5 | (V+) + 0.5 | V |
| | Differential voltage(4) | | ±0.5 | V |
| | Current(3) | | ±10 | mA |
| Output short-circuit(2) | | Continuous | | |
| Operating ambient temperature, $T_A$ | | –55 | 150 | °C |
| Junction temperature, $T_J$ | | | 150 | °C |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |

(1) Operating the device beyond the ratings listed under *Absolute Maximum Ratings* will cause permanent damage to the device. These are stress ratings only, based on process and design limitations, and this device has not been designed to function outside the conditions indicated under *Recommended Operating Conditions*. Exposure to any condition outside *Recommended Operating Conditions* for extended periods, including absolute-maximum-rated conditions, may affect device reliability and performance.
(2) Short-circuit to ground, one amplifier per package. Extended short-circuit current, especially with higher supply voltage, can cause excessive heating and eventual destruction.
(3) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(4) Input pins are connected by back-to-back diodes for input protection. If the differential input voltage may exceed 0.5 V, limit the input current to 10 mA or less.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2500 | V |
| | | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2) | ±1500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_S$ | Supply voltage, (V+) – (V–) | 2.7 | 24 | V |
| $V_I$ | Common mode voltage range | (V–) – 0.1 | (V+) + 0.1 | V |
| $T_A$ | Specified temperature | –40 | 125 | °C |

ADVANCE INFORMATION

## 5.4 Thermal Information for Single Channel

| THERMAL METRIC(1) | | OPA994-Q1 DBV (SOT-23) 5 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | TBD | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | TBD | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | TBD | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | TBD | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | TBD | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | TBD | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 5.5 Thermal Information for Dual Channel

| THERMAL METRIC(1) | | OPA2994-Q1 D (SOIC) 8 PINS | OPA2994-Q1 DGK (VSSOP) 8 PINS | Unit |
|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | TBD | TBD | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | TBD | TBD | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | TBD | TBD | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | TBD | TBD | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | TBD | TBD | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | TBD | TBD | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

ADVANCE INFORMATION

## 5.6 Electrical Characteristics

For $V_S$ = (V+) – (V–) = 2.7 V to 24 V (±1.35 V to ±12 V) at $T_A$ = 25°C, $R_L$ = 10 kΩ connected to $V_S$ / 2, $V_{CM}$ = $V_S$ / 2, and $V_{OUT}$ = $V_S$ / 2, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | | |
| $V_{OS}$ | Input offset voltage | $V_{CM}$ = V– | | | ±0.2 | ±1 | mV |
| | | | $T_A$ = –40°C to 125°C | | | ±1.2 | |
| $dV_{OS}/dT$ | Input offset voltage drift | $V_{CM}$ = V– | $T_A$ = –40°C to 125°C | | ±0.17 | | µV/°C |
| PSRR | Input offset voltage versus power supply | $V_{CM}$ = V–, $V_S$ = 5 V to 24 V | $T_A$ = –40°C to 125°C | | ±3.5 | ±22 | µV/V |
| PSRR | Input offset voltage versus power supply | $V_{CM}$ = V–, $V_S$ = 2.7 V to 24 V | $T_A$ = –40°C to 125°C | | | ±60(1) | µV/V |
| | DC channel separation | | | | 1 | | µV/V |
| **INPUT BIAS CURRENT** | | | | | | | |
| $I_B$ | Input bias current | | | | ±400 | ±1500 | nA |
| $I_{OS}$ | Input offset current | | | | ±2 | | nA |
| **NOISE** | | | | | | | |
| $E_N$ | Input voltage noise | f = 0.1 Hz to 10 Hz | | | 1.8 | | $\mu V_{PP}$ |
| | | | | | 0.3 | | $\mu V_{RMS}$ |
| $e_N$ | Input voltage noise density | f = 1 kHz | | | 12 | | $nV/\sqrt{Hz}$ |
| | | f = 10 kHz | | | 11 | | |
| $i_N$ | Input current noise density | f = 1 kHz | | | 1 | | $pA/\sqrt{Hz}$ |
| **INPUT VOLTAGE RANGE** | | | | | | | |
| $V_{CM}$ | Common-mode input voltage range | | | (V–) – 0.1 | | (V+) + 0.1 | V |
| $V_{Diff}$ | Differential input voltage range | | | | | ±0.5 | V |
| CMRR | Common-mode rejection ratio | $V_S$ = 24 V, V– < $V_{CM}$ < (V+) – 2 V (Main Input Pair) | $T_A$ = –40°C to 125°C | 115 | 135 | | dB |
| | | $V_S$ = 5 V, V– < $V_{CM}$ < (V+) – 2 V (Main Input Pair)(1) | | 105 | 120 | | |
| | | $V_S$ = 2.7 V, V– < $V_{CM}$ < (V+) – 2 V (Main Input Pair) | | | 100 | | |
| | | $V_S$ = 2.7 – 24 V, (V+) – 1 V < $V_{CM}$ < V+ (Aux Input Pair) | | | 95 | | |
| | | (V+) – 2 V < $V_{CM}$ < (V+) – 1 V | $T_A$ = –40°C to 125°C | | See | | |
| **INPUT IMPEDANCE** | | | | | | | |
| $Z_{ID}$ | Differential | | | | 10 \|\| 3 | | MΩ \|\| pF |
| $Z_{ICM}$ | Common-mode | | | | 1 \|\| 1 | | TΩ \|\| pF |
| **OPEN-LOOP GAIN** | | | | | | | |
| $A_{OL}$ | Open-loop voltage gain | $V_S$ = 24 V, $V_{CM}$ = $V_S$ / 2, (V–) + 1 V < $V_O$ < (V+) – 1 V | | 80 | 87 | | dB |
| | | | $T_A$ = –40°C to 125°C | | 87 | | |
| | | $V_S$ = 5 V, $V_{CM}$ = $V_S$ / 2, (V–) + 1 V < $V_O$ < (V+) – 1 V(1) | | 75 | 80 | | |
| | | | $T_A$ = –40°C to 125°C | | 80 | | |
| | | $V_S$ = 2.7 V, $V_{CM}$ = $V_S$ / 2, (V–) + 1 V < $V_O$ < (V+) – 1 V(1) | | 75 | 80 | | |
| | | | $T_A$ = –40°C to 125°C | | 80 | | |

ADVANCE INFORMATION

## 5.6 Electrical Characteristics (続き)

For $V_S$ = (V+) – (V–) = 2.7 V to 24 V (±1.35 V to ±12 V) at $T_A$ = 25°C, $R_L$ = 10 kΩ connected to $V_S$ / 2, $V_{CM}$ = $V_S$ / 2, and $V_{OUT}$ = $V_S$ / 2, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **FREQUENCY RESPONSE** | | | | | | | |
| GBW | Gain-bandwidth product | | | | 25 | | MHz |
| SR | Slew rate | $V_S$ = 24 V, $V_{STEP}$ = 10 V, G = +1, $C_L$ = 20 pF(6) | | | 18 | | V/µs |
| $t_S$ | Settling time | To 0.1%, $V_S$ = 24 V, $V_{STEP}$ = 10 V, G = +1, $C_L$ = 50 pF | | | 0.15 | | µs |
| | | To 0.1%, $V_S$ = 24 V, $V_{STEP}$ = 10 V, G = +1, $C_L$ = 500 pF | | | 0.5 | | |
| | | To 0.01%, $V_S$ = 24 V, $V_{STEP}$ = 10 V, G = +1, $C_L$ = 50 pF | | | 0.65 | | |
| | | To 0.01%, $V_S$ = 24 V, $V_{STEP}$ = 10 V, G = +1, $C_L$ = 500 pF | | | 1 | | |
| | Phase margin | G = +1, $R_L$ = 10 kΩ, $C_L$ = 20 pF | | | 55 | | ° |
| | Overload recovery time | $V_{IN}$ × gain > $V_S$ | | | 200 | | ns |
| THD+N | Total harmonic distortion + noise | $V_S$ = 24 V, $V_O$ = 3 $V_{RMS}$, G = 1, f = 1 kHz, $R_L$ = 10 kΩ | | | 0.0001% | | |
| | | | | | 120 | | dB |
| | | $V_S$ = 10 V, $V_O$ = 3 $V_{RMS}$, G = 1, f = 1 kHz, $R_L$ = 128 Ω | | | 0.001% | | |
| | | | | | 100 | | dB |
| | | $V_S$ = 10 V, $V_O$ = 0.4 $V_{RMS}$, G = 1, f = 1 kHz, $R_L$ = 32 Ω | | | 0.00032% | | |
| | | | | | 110 | | dB |
| **OUTPUT** | | | | | | | |
| | Voltage output swing from rail | Positive and negative rail headroom | $V_S$ = 24 V, $R_L$ = no load | | 35 | | mV |
| | | | $V_S$ = 24 V, $R_L$ = 10 kΩ | | 45 | 55 | |
| | | | $V_S$ = 24 V, $R_L$ = 2 kΩ | | 60 | 70 | |
| | | | $V_S$ = 5 V, $R_L$ = no load | | 35 | | |
| | | | $V_S$ = 5 V, $R_L$ = 10 kΩ | | 40 | 45 | |
| | | | $V_S$ = 5 V, $R_L$ = 2 kΩ | | 45 | 50 | |
| | | | $V_S$ = 2.7 V, $R_L$ = no load | | 30 | | |
| | | | $V_S$ = 2.7 V, $R_L$ = 10 kΩ | | 35 | 40 | |
| | | | $V_S$ = 2.7 V, $R_L$ = 2 kΩ | | 40 | 50 | |
| $I_{SC}$ | Short-circuit current | $V_S$ = 24 V | | ±62 | ±150 | | mA |
| | | $V_S$ = 5 V(1) | | ±50 | ±100 | | |
| | | $V_S$ = 2.7 V(1) | | ±45 | ±65 | | |
| $C_{LOAD}$ | Capacitive load drive | | | | Unlimited; See | | pF |
| $Z_O$ | Open-loop output impedance | $I_O$ = 0 A | | | See | | Ω |
| **POWER SUPPLY** | | | | | | | |
| $I_Q$ | Quiescent current per amplifier | $I_O$ = 0 A | | | 1.25 | 1.7 | mA |
| $I_Q$ | Quiescent current per amplifier | | $T_A$ = –40°C to 125°C | | | 2.1 | mA |

(1) Specified by characterization only.
(2) See for more information.

ADVANCE INFORMATION

# 6 Detailed Description

## 6.1 Overview

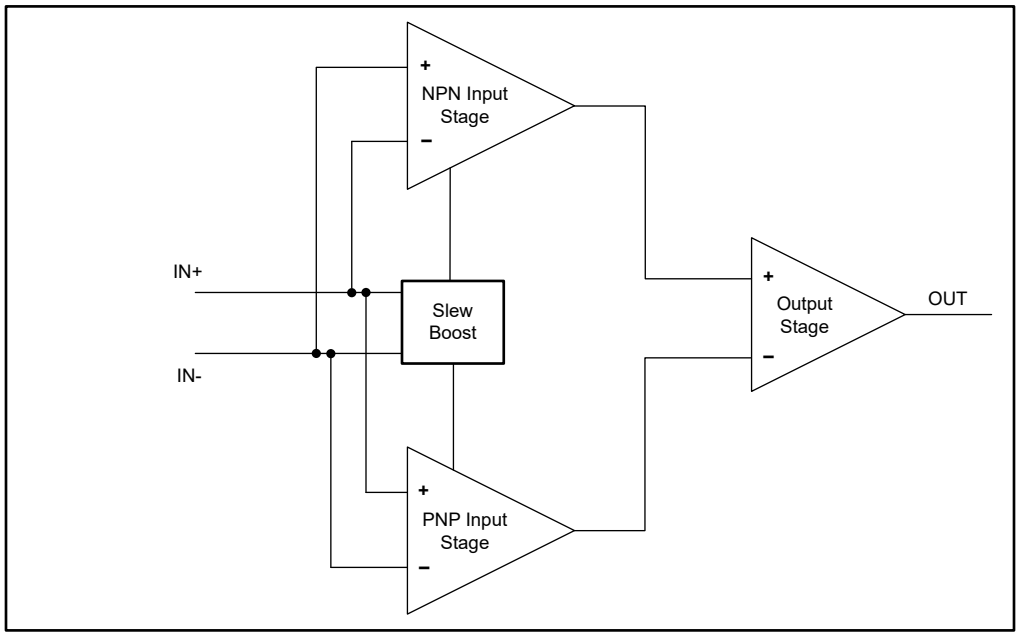
The OPAx994-Q1 family (OPA994-Q1 and OPA2994-Q1) is a family of high voltage (24-V) general purpose operational amplifiers.

The OPAx994-Q1 family has a wide gain bandwidth of 25 MHz when no capacitive load is present. These devices have unlimited capacitive load drive and are able to drive large capacitive loads without continuous oscillations.

These devices also offer excellent DC precision, including rail-to-rail input/output, low offset (±200 µV, typ), and low offset drift (±0.17 µV/°C, typ).

Special features such as unlimited capacitive load drive, high short-circuit current (±150 mA, typ), and high slew rate (18 V/µs, typ) make the OPAx994-Q1 an extremely flexible, robust, and high-performance operational amplifier for high-voltage automotive applications.

## 6.2 Functional Block Diagram




ADVANCE INFORMATION

## 6.3 Feature Description

### 6.3.1 Unlimited Capacitive Load Drive

One of the challenges when designing an op-amp circuit is verifying that the op-amp is stable when driving capacitive loads. The OPAx994-Q1 has a unique architecture that features Unlimited Capacitive Load Drive (UCLD), which is used to prevent sustained oscillations on the amplifier's output signals when driving large capacitive loads. This is achieved by maintaining an acceptable phase margin as the size of the capacitive load increases.

An op-amp circuit that is unstable will have an unpredictable or unexpected output with poor transient performance. This typically results in large overshoots and ringing when changes occur on the input or load, but may also result in sustained oscillations. One common cause of instability in op-amps can occur when connecting a load capacitor, CL, to the output of the amplifier. This instability is a result of the op-amp's internal output resistance, Zo, that creates a secondary pole with CL.

The OPAx994-Q1 family's UCLD has a proprietary output compensation structure that is able to sense the capacitance on the output and adjust internal pole and zero structures to achieve acceptable phase margins. This behavior is unique to UCLD devices and allows the op-amp to remain stable under larger capacitive loads compared to traditional amplifiers.

To keep an acceptable phase margin, UCLD devices lower the gain bandwidth product under larger capacitive loads. The OPAx994-Q1 is specified to have a gain bandwidth product of 25 MHz without significant capacitive load, but this value will begin to decrease at the point where a traditional amplifier would begin to become unstable. This tradeoff is what extends the output drive capability. OPAx994-Q1 is designed with a wide gain bandwidth product to make sure there is headroom for many general-purpose applications with higher capacitive loads.

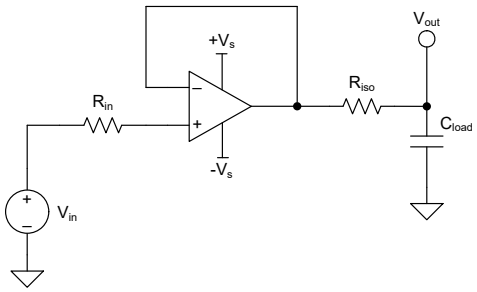



**図 6-1. Extending Capacitive Load Drive With the OPAx994-Q1**

### 6.3.2 EMI Rejection

The OPAx994-Q1 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx994-Q1 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. 表 6-1 provides the EMIRR IN+ values for the OPAx994-Q1 at particular frequencies commonly encountered in real-world applications. The *EMI Rejection Ratio of Operational Amplifiers* application report contains detailed information on the topic of EMIRR performance as it relates to op amps and is available for download from www.ti.com.

ADVANCE INFORMATION

表 6-1. OPAx994-Q1 EMIRR IN+ For Frequencies of Interest

| FREQUENCY | APPLICATION OR ALLOCATION | EMIRR IN+ |
|---|---|---|
| 400 MHz | Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications | 50.0 dB |
| 900 MHz | Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications | 56.3 dB |
| 1.8 GHz | GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz) | 65.6 dB |
| 2.4 GHz | 802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz) | 70.0 dB |
| 3.6 GHz | Radiolocation, aero communication and navigation, satellite, mobile, S-band | 78.9 dB |
| 5 GHz | 802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz) | 91.0 dB |

### 6.3.3 Common-Mode Voltage Range

The OPAx994-Q1 is a 24-V, true rail-to-rail input operational amplifier with an input common-mode range that extends to both supply rails. This wide range is achieved with paralleled complementary PNP and NPN differential input pairs, as shown in 図 6-2. The NPN pair is active for input voltages close to the positive rail, typically from (V+) – 1 V to the positive supply. The PNP pair is active for inputs from the negative supply to approximately (V+) – 2 V. There is a small transition region, typically (V+) – 2 V to (V+) – 1 V, in which both input pairs are on. This transition region can vary modestly with process variation. Within this region PSRR, CMRR, offset voltage, offset drift, noise, and THD performance may be degraded compared to operation outside this region.

For more information on common-mode voltage range and complementary pair interaction, see *Op Amps With Complementary-Pair Input Stages* application note.

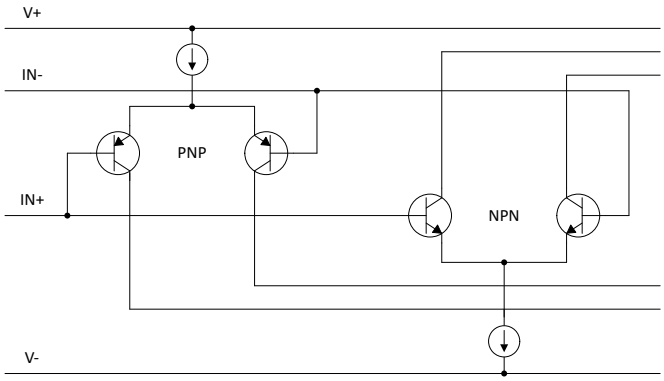



図 6-2. Rail-to-Rail Input Stage

### 6.3.4 Phase Reversal Protection

The OPAx994-Q1 family has internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in non-inverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The OPAx994-Q1 is a rail-to-rail input op amp; therefore, the common-mode range can extend up to the rails. Input signals beyond the rails do not cause phase reversal; instead, the output limits into the appropriate rail. This performance is shown in 図 6-3. For more information on phase reversal, see *Op Amps With Complementary-Pair Input Stages* application note.

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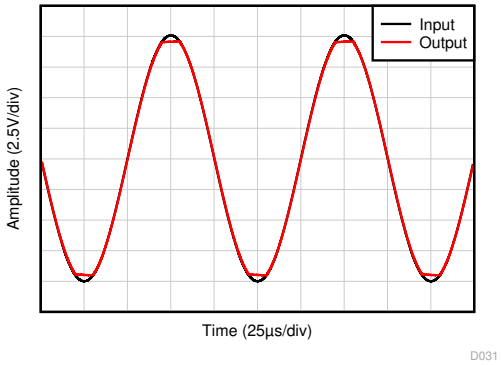


**図 6-3. No Phase Reversal**

### 6.3.5 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. 図 6-4 shows an illustration of the ESD circuits contained in the OPAx994-Q1 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

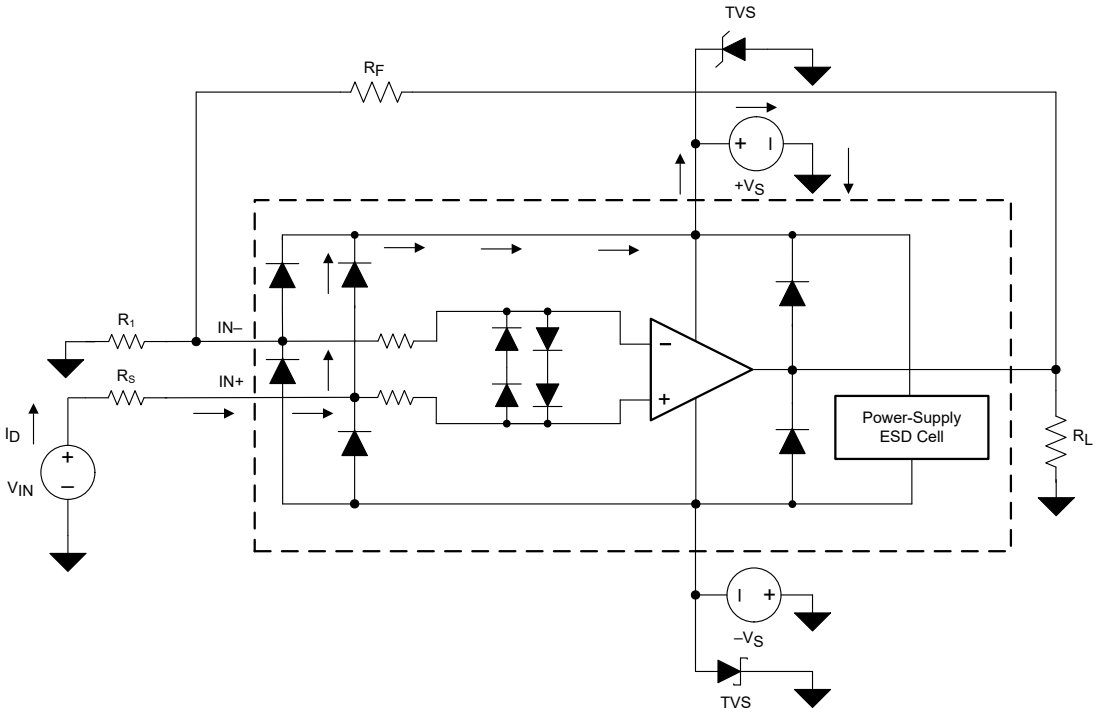


**図 6-4. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application**





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An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse while discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device terminals, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPAx994-Q1 but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit (as shown in 図 6-4), the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given terminal. If this condition occurs, there is a risk that some internal ESD protection circuits can turn on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

図 6-4 shows a specific example where the input voltage ($V_{IN}$) exceeds the positive supply voltage ($+V_S$) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher $V_{IN}$. As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, $V_{IN}$ can begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ or $–V_S$ are at 0 V. Again, this question depends on the supply characteristic while at 0 V, or at a level below the input-signal amplitude. If the supplies appear as high impedance, then the input source supplies the operational amplifier current through the current-steering diodes. This state is not a normal bias condition; most likely, the amplifier will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, add external zener diodes to the supply terminals; see 図 6-4. Select the zener voltage so that the diode does not turn on during normal operation. However, the zener voltage must be low enough so that the zener diode conducts if the supply terminal begins to rise above the safe-operating, supply-voltage level.

The OPAx994-Q1 input terminals are protected from excessive differential voltage with back-to-back diodes; see 図 6-4. In most circuit applications, the input protection circuitry has no effect. However, in low-gain or G = 1 circuits, fast-ramping input signals can forward-bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward-bias condition, limit the input signal current to 10 mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the input signal current. This input series resistor degrades the low-noise performance of the OPAx994-Q1. 図 6-4 shows an example configuration that implements a current-limiting feedback resistor.

### 6.3.6 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the

ADVANCE INFORMATION

propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the OPAx994-Q1 is approximately 200 ns.

### 6.3.7 Typical Specifications and Distributions

Designers often have questions about a typical specification of an amplifier to design a more robust circuit. Due to natural variation in process technology and manufacturing procedures, every specification of an amplifier will exhibit some amount of deviation from the ideal value, like an amplifier's input offset voltage. These deviations often follow *Gaussian* (*bell curve*), or *normal* distributions, and circuit designers can leverage this information to guardband their system, even when there is not a minimum or maximum specification in the *Electrical Characteristics* table.

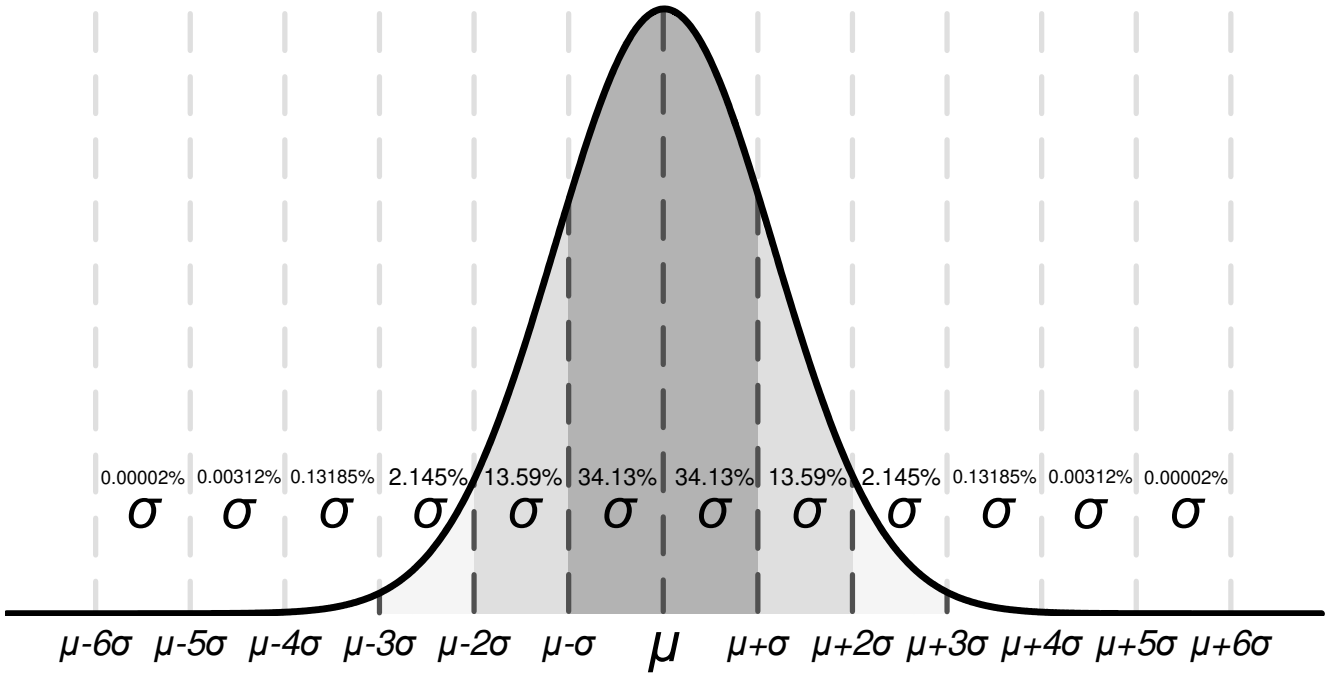


**図 6-5. Ideal Gaussian Distribution**

The 図 6-5 figure shows an example distribution, where *μ*, or *mu*, is the mean of the distribution, and where *σ*, or *sigma*, is the standard deviation of a system. For a specification that exhibits this kind of distribution, approximately two-thirds (68.26%) of all units can be expected to have a value within one standard deviation, or one sigma, of the mean (from *μ–σ* to *μ+σ*).

Depending on the specification, values listed in the *typical* column of the *Electrical Characteristics* table are represented in different ways. As a general rule, if a specification naturally has a nonzero mean (for example, like gain bandwidth), then the typical value is equal to the mean (μ). However, if a specification naturally has a mean near zero (like input offset voltage), then the typical value is equal to the mean plus one standard deviation (μ + σ) to most accurately represent the typical value.

Designers can use this chart to calculate approximate probability of a specification in a unit; for example, for OPAx994-Q1, the typical input voltage offset is 200 μV. So 68.2% of all OPAx994-Q1 devices are expected to have an offset from –200 μV to +200 μV. At 4 *σ* (±800 μV), 99.9937% of the distribution has an offset voltage less than ±800 μV, which means 0.0063% of the population is outside of these limits, which corresponds to about 1 in 15,873 units.

Specifications with a value in the minimum or maximum column are assured by TI, and units outside these limits will be removed from production material. For example, the OPAx994-Q1 family has a maximum offset voltage of 1 mV at 25°C, and even though this corresponds to slightly less than 5 σ (≈1 in 1.7 million units), which is extremely unlikely, TI assures that any unit with larger offset than 1 mV will be removed from production material.

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For specifications with no value in the minimum or maximum column, consider selecting a sigma value of sufficient guardband for the designers application, and design worst-case conditions using this value. For example, the 6-σ value corresponds to about 1 in 500 million units, which is an extremely unlikely chance, and could be an option as a wide guardband to design a system around. In this case, the OPAx994-Q1 family does not have a maximum or minimum for offset voltage drift. But based on the typical value of 0.17 µV/°C in the *Electrical Characteristics* table, it can be calculated that the 6-σ value for offset voltage drift is about 1.02 µV/°C. When designing for worst-case system conditions, this value can be used to estimate the worst possible offset across temperature without having an actual minimum or maximum value.

Note that process variation and adjustments over time can shift typical means and standard deviations, and unless there is a value in the minimum or maximum specification column, TI cannot assure the performance of a device. This information should be used only to estimate the performance of a device.

### 6.4 Device Functional Modes

The OPAx994-Q1 has a single functional mode and is operational when the power-supply voltage is greater than or equal to 2.7 V (±1.35 V). The maximum power supply voltage for the OPAx994-Q1 is 24 V (±12 V).

# 7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 7.1 Application Information

The OPAx994-Q1 family offers excellent DC precision and AC performance. These devices operate up to 24-V supply rails and offer true rail-to-rail input/output, low offset voltage and offset voltage drift, as well as 25-MHz bandwidth and high output drive. These features make the OPAx994-Q1 a robust, high-performance operational amplifier for high-voltage automotive applications.

## 7.2 Typical Applications

### 7.2.1 Low-Side Current Measurement

図 7-1 shows the OPA994-Q1 configured in a low-side current sensing application. For a full analysis of the circuit shown in 図 7-1 including theory, calculations, simulations, and measured data, see TI Precision Design TIPD129, *0-A to 1-A Single-Supply Low-Side Current-Sensing Solution*.

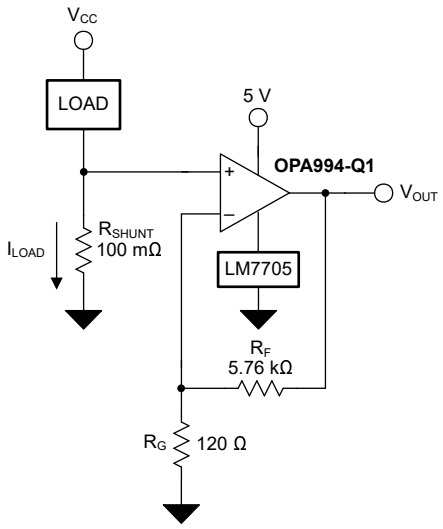


**図 7-1. OPAx994-Q1 in a Low-Side, Current-Sensing Application**

#### *7.2.1.1 Design Requirements*

The design requirements for this design are as follows:

- Load current: 0 A to 1 A
- Max output voltage: 4.9 V
- Maximum shunt voltage: 100 mV

#### *7.2.1.2 Detailed Design Procedure*

The transfer function of the circuit in 図 7-1 is given in 式 1:

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times Gain \quad (1)$$

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The load current ($I_{LOAD}$) produces a voltage drop across the shunt resistor ($R_{SHUNT}$). The load current is set from 0 A to 1 A. To keep the shunt voltage below 100 mV at maximum load current, the largest shunt resistor is defined using 式 2:

$$R_{SHUNT} = \frac{V_{SHUNT\_MAX}}{I_{LOAD\_MAX}} = \frac{100\,mV}{1\,A} = 100\,m\Omega \quad (2)$$

Using 式 2, $R_{SHUNT}$ is calculated to be 100 mΩ. The voltage drop produced by $I_{LOAD}$ and $R_{SHUNT}$ is amplified by the OPA994-Q1 to produce an output voltage of 0 V to 4.9 V. The gain needed by the OPA994-Q1 to produce the necessary output voltage is calculated using 式 3:

$$Gain = \frac{(V_{OUT\_MAX} - V_{OUT\_MIN})}{(V_{IN\_MAX} - V_{IN\_MIN})} \quad (3)$$

Using 式 3, the required gain is calculated to be 49 V/V, which is set with resistors $R_F$ and $R_G$. 式 4 is used to size the resistors, $R_F$ and $R_G$, to set the gain of the OPA994-Q1 to 49 V/V.

$$Gain = 1 + \frac{(R_F)}{(R_G)} \quad (4)$$

Choosing $R_F$ as 5.76 kΩ, $R_G$ is calculated to be 120 Ω. $R_F$ and $R_G$ were chosen as 5.76 kΩ and 120 Ω because they are standard value resistors that create a 49:1 ratio. Other resistors that create a 49:1 ratio can also be used. However, excessively large resistors will generate thermal noise that exceeds the intrinsic noise of the op amp. 図 7-2 shows the measured transfer function of the circuit shown in 図 7-1.

#### *7.2.1.3 Application Curve*

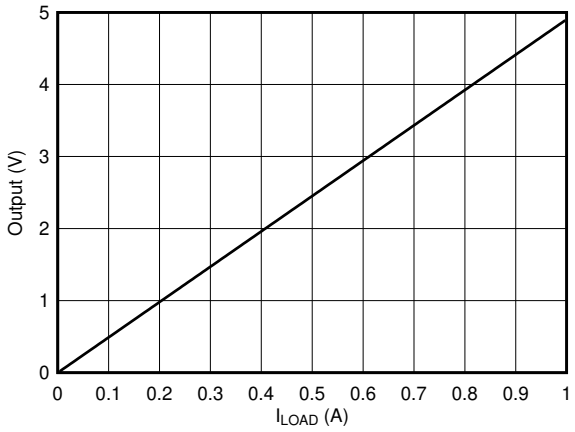


**図 7-2. Low-Side, Current-Sense, Transfer Function**

## 7.3 Power Supply Recommendations

The OPAx994-Q1 is specified for operation from 2.7 V to 24 V (±1.35 V to ±12 V); many specifications apply from –40°C to 125°C or with specific supply voltages and test conditions.

> **注意**
>
> Supply voltages larger than 24 V can permanently damage the device; see *Absolute Maximum Ratings*.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to セクション 7.4.

ADVANCE INFORMATION

## 7.4 Layout

### 7.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in , keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

### 7.4.2 Layout Example

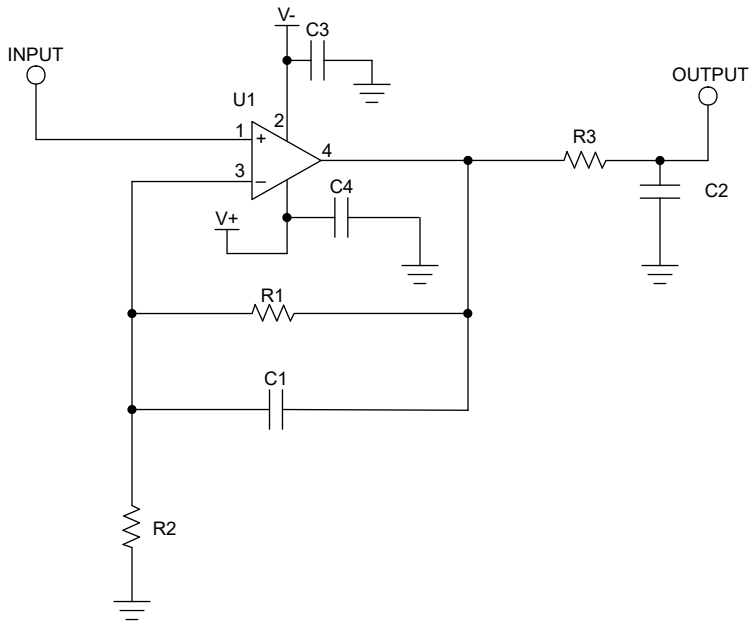


**図 7-3. Schematic for Noninverting Configuration Layout Example**

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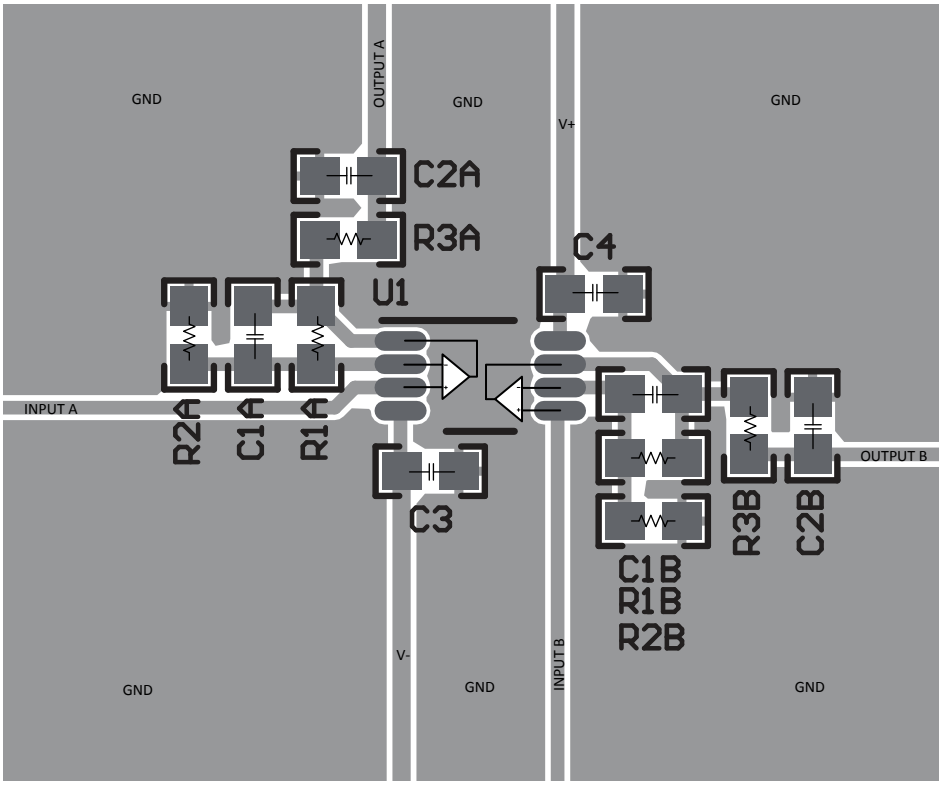


**図 7-4. Example Layout for VSSOP-8 (DGK) Package**

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# 8 Device and Documentation Support

## 8.1 Device Support

### 8.1.1 Development Support

#### *8.1.1.1 TINA-TI™ (Free Software Download)*

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

注

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

## 8.2 Documentation Support

### 8.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *MUX-Friendly, Precision Operational Amplifiers* application brief
- Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers* application report
- Texas Instruments, *Op Amps With Complementary-Pair Input Stages* application note
- Texas Instruments, *0-1-A, Single-Supply, Low-Side, Current Sensing Solution* reference design (TIPD129)

## 8.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

## 8.4 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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## 8.5 Trademarks

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Bluetooth® is a registered trademark of Bluetooth SIG, Inc.
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## 8.6 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

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### 8.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

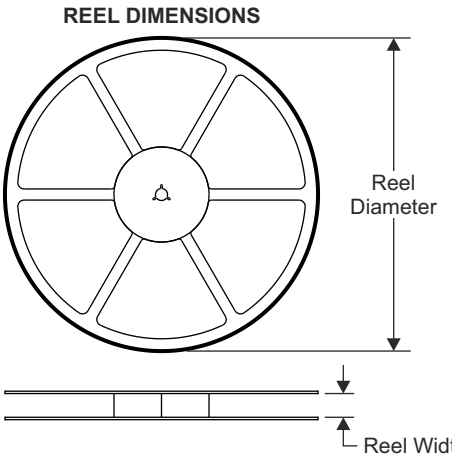
## 9 Revision History

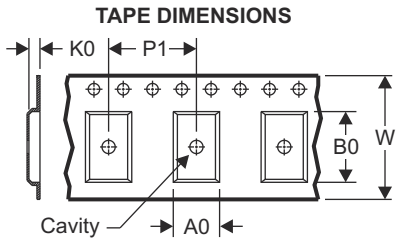
| DATE | REVISION | NOTES |
|---|---|---|
| November 2023 | * | Initial Release |

## 10 Mechanical, Packaging, and Orderable Information

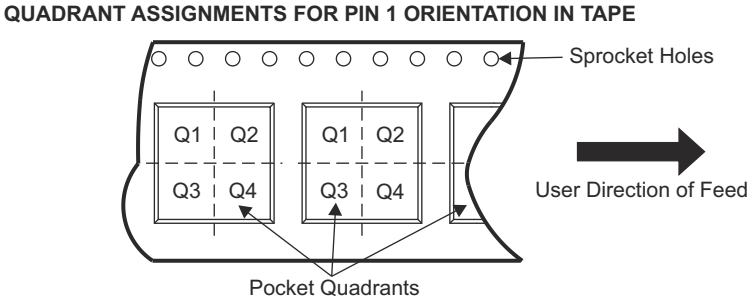
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

### 10.1 Tape and Reel Information



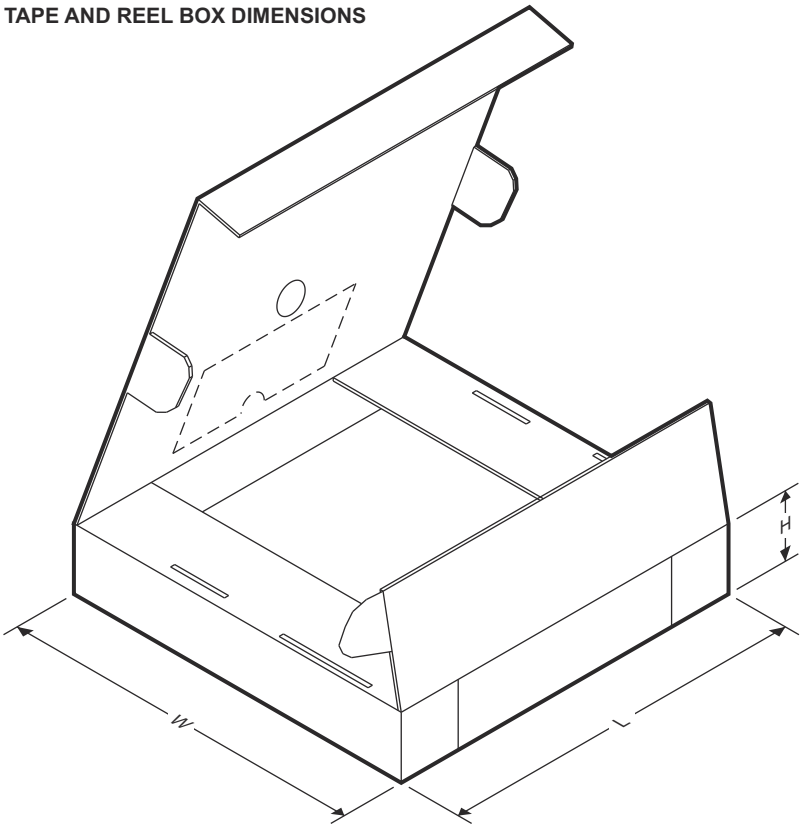

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |




| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OPA994QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| OPA2994QDRQ1 | SOIC | D | 8 | 3000 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| OPA2994QDGKRQ1 | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |

ADVANCE INFORMATION

**TAPE AND REEL BOX DIMENSIONS**




| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| OPA994QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| OPA2994QDRQ1 | SOIC | D | 8 | 3000 | 356.0 | 356.0 | 35.0 |
| OPA2994QDGKRQ1 | VSSOP | DGK | 8 | 2500 | 366.0 | 364.0 | 50.0 |

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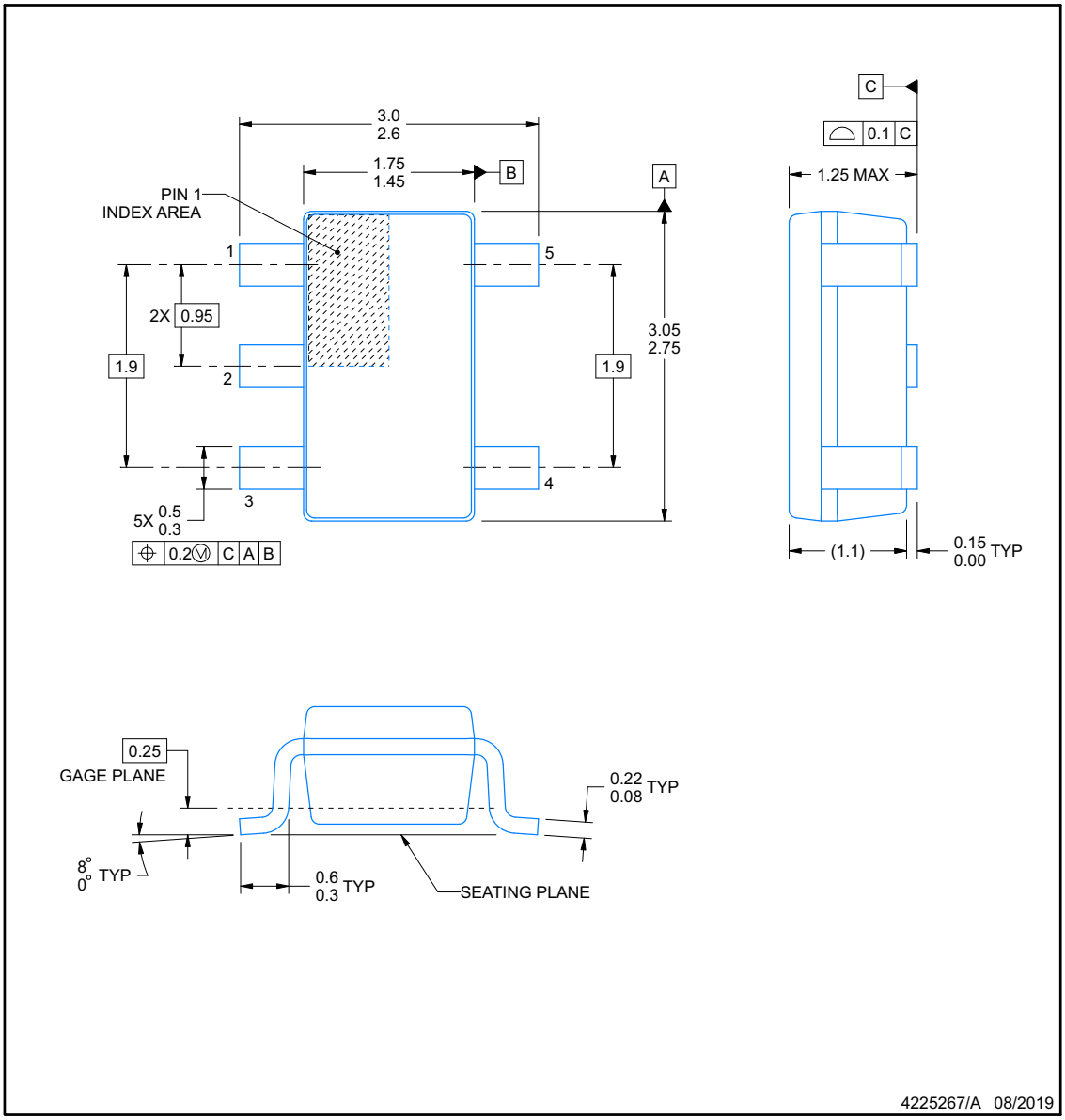
## 10.2 Mechanical Data

### PACKAGE OUTLINE

**DBV0005A-C01** — **SOT-23 - 1.25 mm max height**

SMALL OUTLINE TRANSISTOR




NOTES:

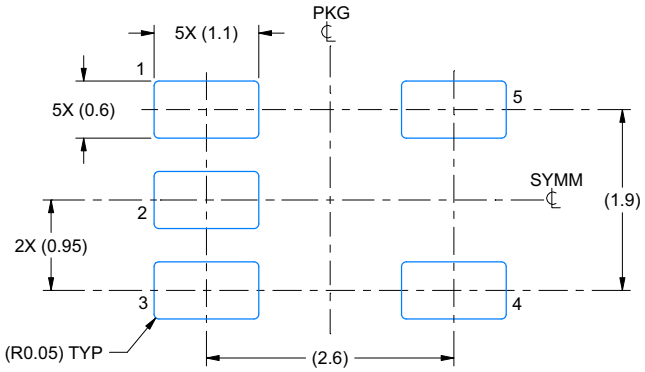
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

# EXAMPLE BOARD LAYOUT

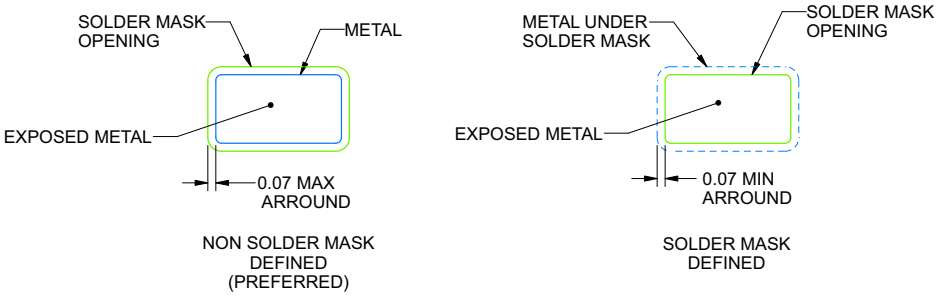
## DBV0005A-C01

### SOT-23 - 1.25 mm max height

SMALL OUTLINE TRANSISTOR




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X




SOLDER MASK DETAILS

4225267/A 08/2019

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

ADVANCE INFORMATION

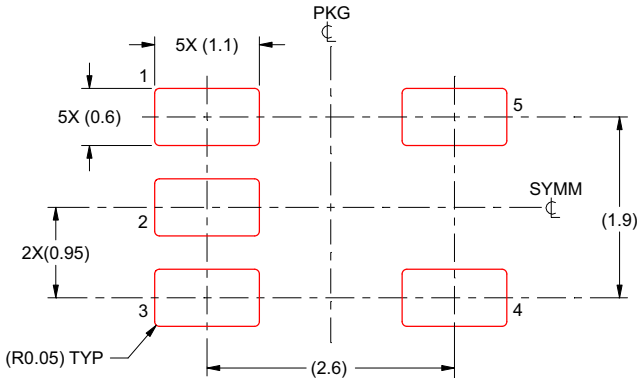
ADVANCE INFORMATION

## EXAMPLE STENCIL DESIGN

### DBV0005A-C01

### SOT-23 - 1.25 mm max height

SMALL OUTLINE TRANSISTOR




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4225267/A 08/2019

NOTES: (continued)

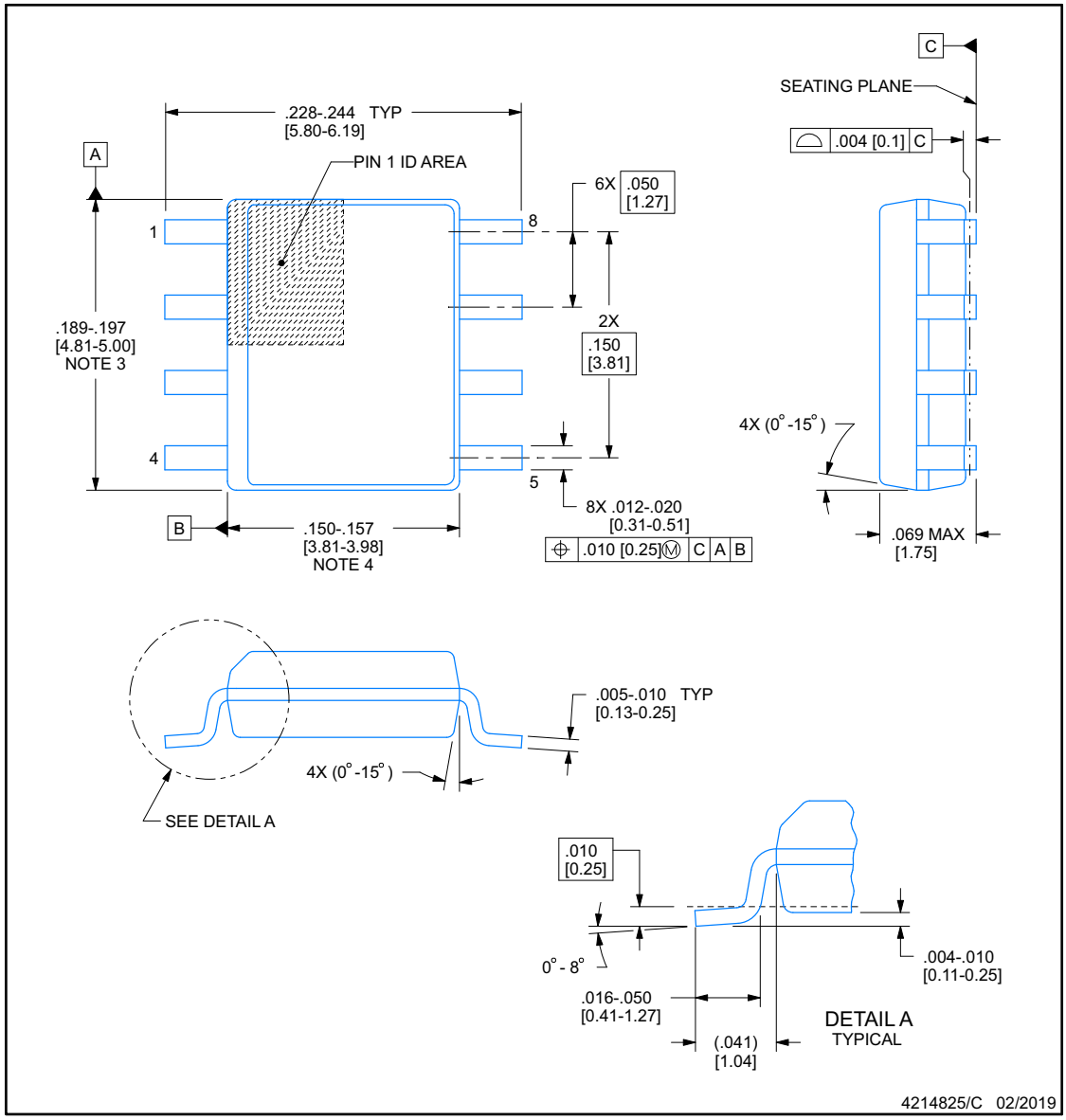
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.







ADVANCE INFORMATION

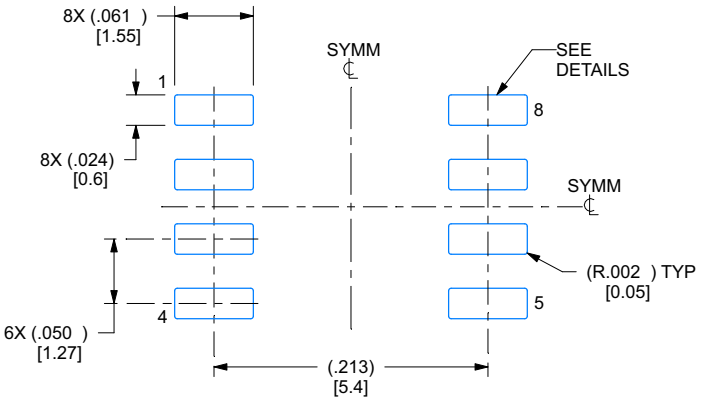
ADVANCE INFORMATION

## EXAMPLE BOARD LAYOUT

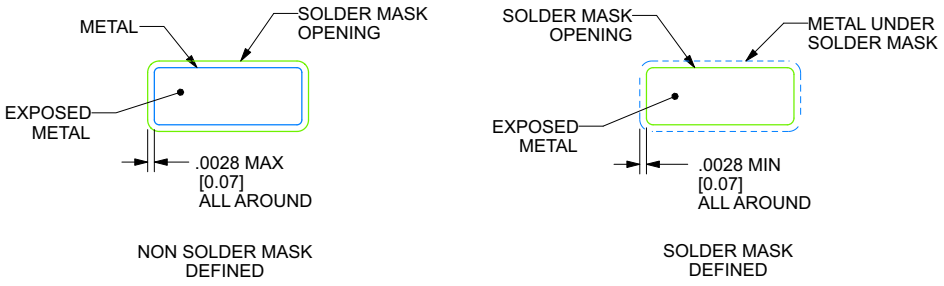
### D0008A

### SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

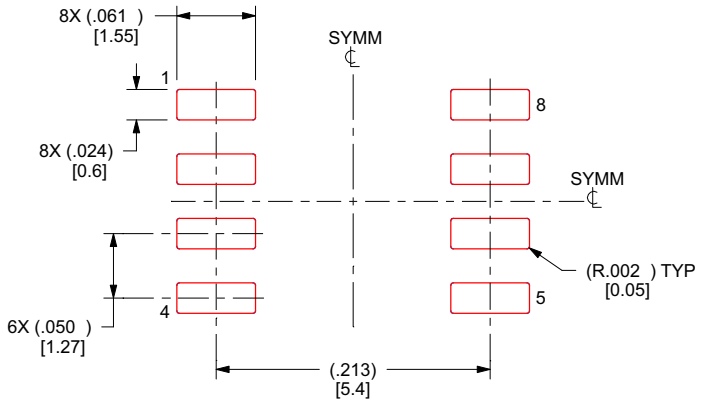
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

### SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

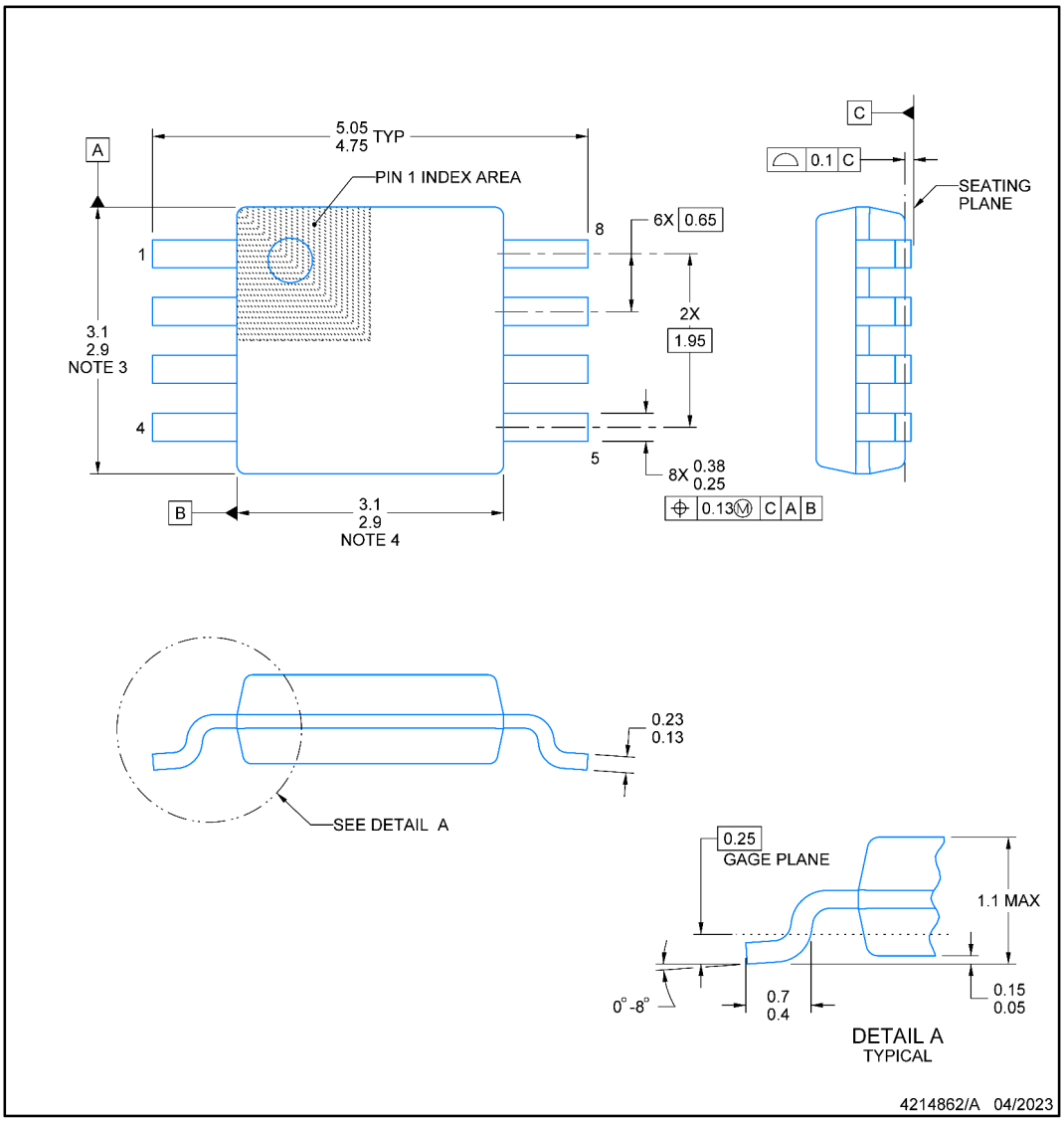
ADVANCE INFORMATION

# PACKAGE OUTLINE

## DGK0008A

## VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE




PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

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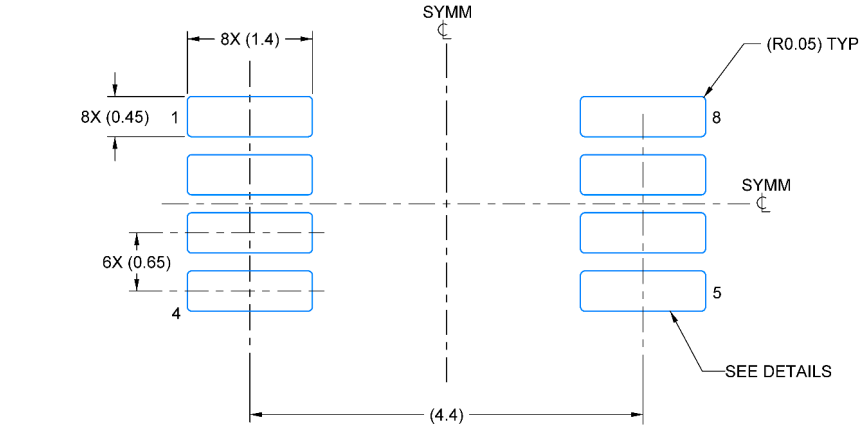
## EXAMPLE BOARD LAYOUT

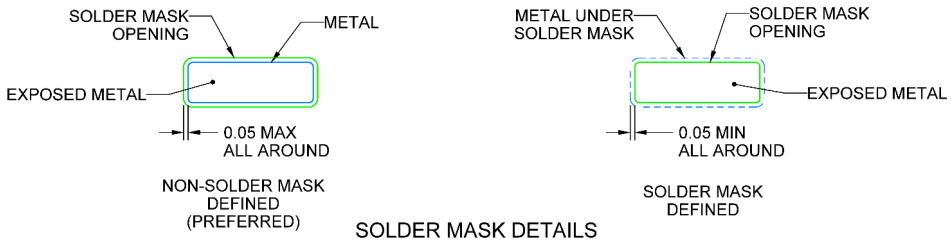
### DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X




SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

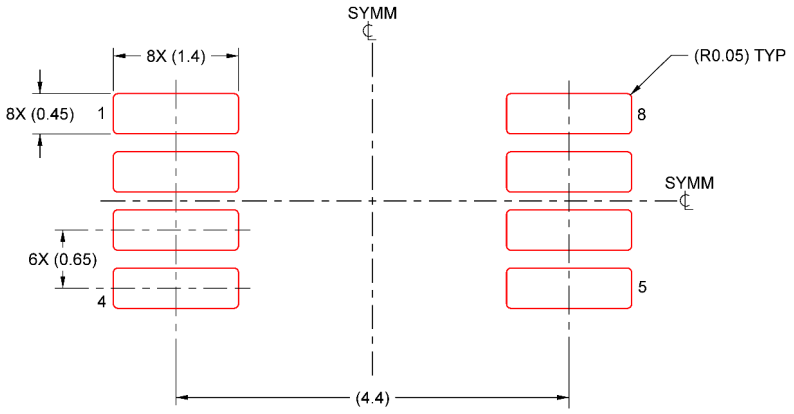
ADVANCE INFORMATION

## EXAMPLE STENCIL DESIGN

### DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE




SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| POPA2994QDRQ1 | ACTIVE | SOIC | D | 8 | 3000 | TBD | Call TI | Call TI | -40 to 125 | | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



**OTHER QUALIFIED VERSIONS OF OPA2994-Q1 :**

- Catalog : OPA2994

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

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