TEXAS INSTRUMENTS
OPA991, OPA2991, OPA4991
JAJSI52F – OCTOBER 2019 – REVISED JANUARY 2022

# OPAx991 40V レール・ツー・レール入出力、低オフセット電圧、低ノイズ・オペアンプ

## 1 特長

- 低いオフセット電圧:±125μV
- 低い入力オフセット電圧ドリフト:±0.3μV/℃
- 低いノイズ:1kHz 時に 10.8nV/√Hz
- 大きい同相除去比:130dB
- 小さいバイアス電流:±10pA
- レール・ツー・レール入出力
- 広い帯域幅:4.5MHz GBW
- 高いスルーレート:21V/μs
- 高い容量性負荷駆動能力:1nF
- 多重化対応 / コンパレータ入力
  - 電源レールまでの差動入力でアンプが動作
  - アンプを開ループで、またはコンパレータとして使用可能
- 低い静止電流:560μA (アンプ 1 個あたり)
- 広い電源範囲:±1.35V～±20V、2.7V～40V
- 堅牢な EMIRR 性能:入力ピンと電源ピンの EMI/RFI フィルタ
- 差動および同相入力電圧範囲は電源レールまで

## 2 アプリケーション

- 低消費電力オーディオ・プリアンプ
- 多重化データ収集システム
- 試験および計測機器
- ADC ドライバ・アンプ
- SAR ADC リファレンス・バッファ
- プログラマブル・ロジック・コントローラ
- ハイサイドおよびローサイド電流センシング

## 3 概要

The OPAx991 ファミリ (OPA991、OPA2991、OPA4991) は、高電圧 (40V) 汎用オペアンプ・ファミリです。これらのデバイスは、レール・ツー・レール入出力、低いオフセット (±125μV、標準値)、低いオフセット・ドリフト (±0.3μV/℃、標準値)、低ノイズ (10.5nV/√Hz、1.8μVPP)、4.5MHz の帯域幅など、非常に優れた DC 精度と AC 性能を備えています。

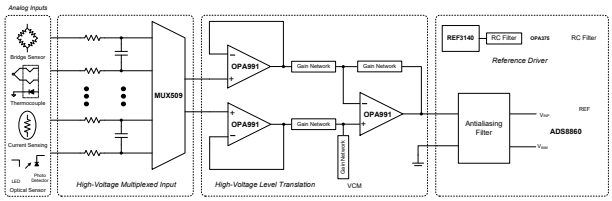
電源レールまでの差動および同相入力電圧範囲、大きい出力電流 (±75mA)、高いスルーレート (21V/μs)、高い容量性負荷駆動能力 (1nF)、シャットダウン機能など、独自の特長を備えた OPAx991 は、高電圧産業用アプリケーション向けの堅牢な高性能オペアンプです。

OPAx991 ファミリのオペアンプは、標準パッケージ (SOT-23、SOIC、TSSOP など) だけでなくマイクロサイズ・パッケージ (X2QFN、WSON など) でも供給され、-40℃～125℃で仕様が規定されています。

**製品情報**

| 部品番号(1) | パッケージ | 本体サイズ (公称) |
|---|---|---|
| OPA991 | SOT-23 (5) | 2.90mm × 1.60mm |
| | SOT-23 (6) | 2.90mm × 1.60mm |
| | SC70 (5) | 2.00mm × 1.25mm |
| OPA2991 | SOIC (8) | 4.90mm × 3.90mm |
| | SOT-23 (8) | 2.90mm × 1.60mm |
| | TSSOP (8) | 3.00mm × 4.40mm |
| | VSSOP (8) | 3.00mm × 3.00mm |
| | WSON (8) | 2.00mm × 2.00mm |
| | X2QFN (10) | 2.00mm × 1.50mm |
| OPA4991 | SOIC (14) | 8.65mm × 3.90mm |
| | SOT-23 (14) | 4.20mm × 1.90mm |
| | TSSOP (14) | 5.00mm × 4.40mm |
| | X2QFN (14) | 2.00mm × 2.00mm |

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。




**OPAx991 を使用した高電圧の多重化データ収集システム**

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| Changes from Revision E (May 2021) to Revision F (January 2022) | Page |
|---|---|
| • 「*製品情報*」に SOT-23-14 (DYY) パッケージを追加 | 1 |
| • 「*製品情報*」から WQFN (RTE) パッケージを削除 | 1 |
| • 「*概要*」から SOT-553 (DRL) パッケージを削除 | 1 |
| • Added SOT-23-14 (DYY) package in *Pin Configuration and Functions* section | 4 |
| • Removed WQFN (RTE) package in *Pin Configuration and Functions* section | 4 |
| • Corrected two typos mislabeling the RUC package as a "WQFN" package instead of as a "X2QFN" package in *Pin Configuration and Functions* section | 4 |
| • Corrected typo mislabeling the RUC package as having an "Exposed Thermal Pad" in *Pin Configuration and Functions* section | 4 |
| • Added X2QFN pinout to Pin Functions: OPA4991 in *Pin Configuration and Functions* section | 4 |
| • Updated OPA991S DBV and DRL pinout to correct typo mislabeling "SHDN" pin as the "NC" pin in *Pin Configuration and Functions* section | 4 |
| • Removed overbar on "SHDN" pin from OPA2991S DGS and RUG pinouts for added clarity and consistency in the *Pin Configuration and Functions* section | 4 |
| • Added SOT-23-14 (DYY) package in *Thermal Information for Quad Channel* section | 10 |
| • Removed "OPA4991S" from header of *Thermal Information for Quad Channel* section | 10 |
| • Corrected typo mislabeling the RUC package as a "WQFN" package instead of as a "X2QFN" package in *Thermal Information for Quad Channel* section | 10 |
| • Removed the overbar from the SHDN pin name in the note on $t_{off}$ and $t_{on}$ in the *Electrical Characteristics* section for consistency | 11 |
| • Changed input resistor values in *Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application* in *Electrical Overstress* section to more closely resemble device | 27 |
| • Removed WQFN (RTE) package from *Packages With an Exposed Thermal Pad* | 30 |
| • Expanded the *Shutdown* section in the *Detailed Description* section to further clarify shutdown operation. Also corrected the current consumption in shutdown from 20µA to 30µA, the valid logic low voltage threshold from "V- + 0.4 V" to "V- + 0.2 V", the valid logic high voltage threshold from "V- + 1.2 V" to "V- + 1.1 V", and the "typical enable time" in the section from 30µs to 8µs to align with the *Electrical Characteristics* section | 30 |


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- Corrected typo for specified operating supply region from "2.7 V to 40 V (±1.35 V to ±40 V)" to "2.7 V to 40 V (±1.35 V to ±20 V)" in *Power Supply Recommendations* section ..... 34

**Changes from Revision D (July 2020) to Revision E (May 2021)** **Page**

- 「*製品情報*」の X2QFN-14 (RUC) パッケージからプレビュー注記を削除..... 1
- 「*製品情報*」の VSSOP-8 (DGK) パッケージからプレビュー注記を削除..... 1
- Removed preview notation from X2QFN-14 (RUC) package in *Pin Configuration and Functions* section .....4
- Removed preview notation from VSSOP-8 (DGK) in *Pin Configuration and Functions* section .....4
- Removed Table of Graphs from the *Specifications* section..... 9

**Changes from Revision C (May 2020) to Revision D (July 2020)** **Page**

- 文書全体にわたって表、図、相互参照の採番方法を更新.....1
- 「*製品情報*」の SOIC-14 (D) パッケージからプレビュー注記を削除.....1
- 「*製品情報*」の SOT-23-5 (DBV) パッケージからプレビュー注記を削除..... 1
- 「*製品情報*」の SOT-23-6 (DBV) パッケージからプレビュー注記を削除..... 1
- 「*製品情報*」の SC70 (DCK) パッケージからプレビュー注記を削除.....1
- 「*製品情報*」の SOT-23-8 (DDF) パッケージからプレビュー注記を削除..... 1
- 「*製品情報*」の TSSOP-14 (PW) パッケージからプレビュー注記を削除..... 1
- Removed preview notation on SOT-23-5 (DBV), and SC70 (DCK).....4
- Clarified SHDN notation in the OPA991S *Pin Configuration and Functions* section ..... 4
- Removed preview notation from SOT-23-6 (DBV) package in *Pin Configuration and Functions* section .....4
- Removed preview notation from SOT-23-8 (DDF) package in *Pin Configuration and Functions* section .....4
- Clarified SHDN notation in OPA2991S *Pin Configuration and Functions* section ..... 4
- Removed preview notation from SOIC-14 (D) and TSSOP-14 (PW) packages in *Pin Configuration and Functions* section .....4
- Clarified SHDN notation in OPA4991S *Pin Configuration and Functions* section ..... 4

**Changes from Revision B (May 2020) to Revision C (May 2020)** **Page**

- Removed preview notation from TSSOP (PW) package in *Pin Configuration and Functions* section .....4
- Removed preview notation from X2QFN (RUG) package in *Pin Configuration and Functions* section .....4

**Changes from Revision A (December 2019) to Revision B (May 2020)** **Page**

- OPA991 および OPA4991 デバイスをデータシートに追加.....1
- 「*製品情報*」の WSON (DSG) パッケージからプレビュー注記を削除..... 1
- 「*製品情報*」セクションで X2QFN (10) の寸法を変更.....1
- Changed formatting of Pin Functions tables to align with data sheet standards..... 4
- Deleted preview notation from WSON (DSG) package in *Pin Configuration and Functions* section .....4

**Changes from Revision * (October 2019) to Revision A (December 2019)** **Page**

- デバイス・ステータスを「*事前情報*」から「*量産データ*」に変更..... 1
- 「*製品情報*」の SOIC (D) パッケージからプレビュー注記を削除..... 1
- Removed preview notation from SOIC (D) package in *Pin Configuration and Functions* section..... 4
- Added *Typical Characteristics* section in *Specifications* section..... 14
- Added additional references in *Related Documentation* section..... 36

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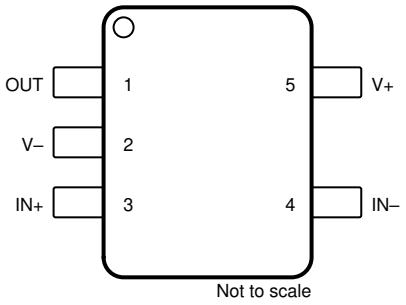
## 5 Pin Configuration and Functions




A. DRL package is preview only.

**図 5-1. OPA991 DBV, T DCK, and DRL Package(A) 5-Pin SOT-23, SC70, and SOT-553 (Top View)**

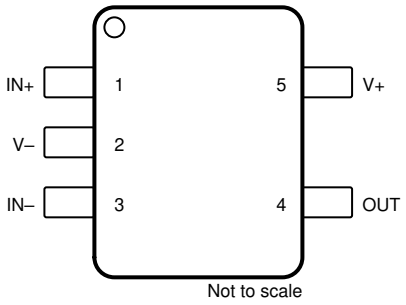



**図 5-2. OPA991 DCK Package 5-Pin SC70 (Top View)**

**表 5-1. Pin Functions: OPA991**

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | DBV, DRL | DCK | | |
| IN+ | 3 | 1 | I | Noninverting input |
| IN– | 4 | 3 | I | Inverting input |
| OUT | 1 | 4 | O | Output |
| V+ | 5 | 5 | — | Positive (highest) power supply |
| V– | 2 | 2 | — | Negative (lowest) power supply |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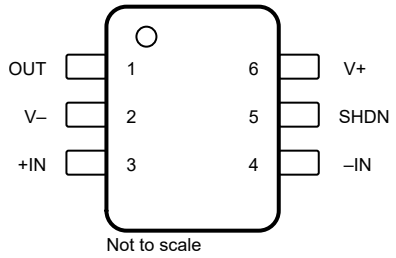


A. DRL package is preview only.

**図 5-3. OPA991S DBV and DRL Package(A)**
**6-Pin SOT-23 and SOT-563**
**(Top View)**

**表 5-2. Pin Functions: OPA991S**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| +IN | 3 | I | Noninverting input |
| –IN | 4 | I | Inverting input |
| OUT | 1 | O | Output |
| SHDN | 5 | I | Shutdown: low = amplifier enabled, high = amplifier disabled. See セクション 7.3.11 for more information. |
| V+ | 6 | — | Positive (highest) power supply |
| V– | 2 | — | Negative (lowest) power supply |

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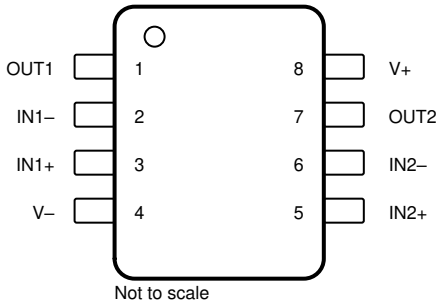
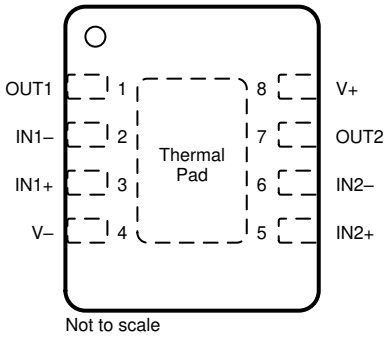



**図 5-4. OPA2991 D, DDF, DGK, and PW Package 8-Pin SOIC, SOT-23, TSSOP, and VSSOP (Top View)**




A. Connect thermal pad to V–. See セクション 7.3.10 for more information.

**図 5-5. OPA2991 DSG Package(A) 8-Pin WSON With Exposed Thermal Pad (Top View)**

**表 5-3. Pin Functions: OPA2991**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| +IN A | 3 | I | Noninverting input, channel A |
| +IN B | 5 | I | Noninverting input, channel B |
| –IN A | 2 | I | Inverting input, channel A |
| –IN B | 6 | I | Inverting input, channel B |
| OUT A | 1 | O | Output, channel A |
| OUT B | 7 | O | Output, channel B |
| V+ | 8 | — | Positive (highest) power supply |
| V– | 4 | — | Negative (lowest) power supply |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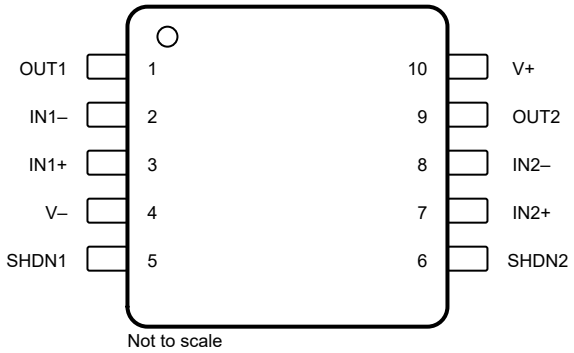


A. Package is preview only.

**図 5-6. OPA2991S DGS Package(A)**
**10-Pin VSSOP**
**(Top View)**

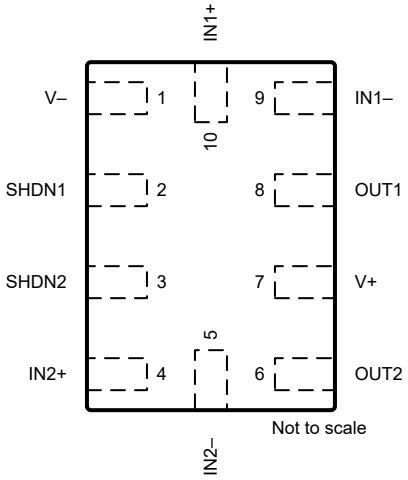


**図 5-7. OPA2991S RUG Package**
**10-Pin X2QFN**
**(Top View)**

**表 5-4. Pin Functions: OPA2991S**

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | VSSOP | X2QFN | | |
| +IN A | 3 | 10 | I | Noninverting input, channel A |
| +IN B | 7 | 4 | I | Noninverting input, channel B |
| –IN A | 2 | 9 | I | Inverting input, channel A |
| –IN B | 8 | 5 | I | Inverting input, channel B |
| OUT A | 1 | 8 | O | Output, channel A |
| OUT B | 9 | 6 | O | Output, channel B |
| SHDN1 | 5 | 2 | I | Shutdown, channel 1: low = amplifier enabled, high = amplifier disabled. See セクション 7.3.11 for more information. |
| SHDN2 | 6 | 3 | I | Shutdown, channel 2: low = amplifier enabled, high = amplifier disabled. See セクション 7.3.11 for more information. |
| V+ | 10 | 7 | — | Positive (highest) power supply |
| V– | 4 | 1 | — | Negative (lowest) power supply |

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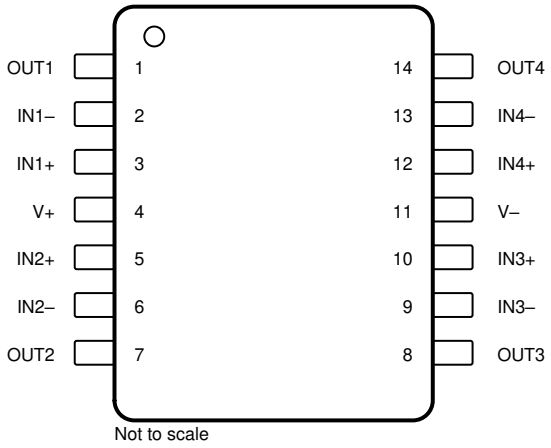


**図 5-8. OPA4991 D, PW, and DYY Packages 14-Pin SOIC, TSSOP, SOT-23 (Top View)**

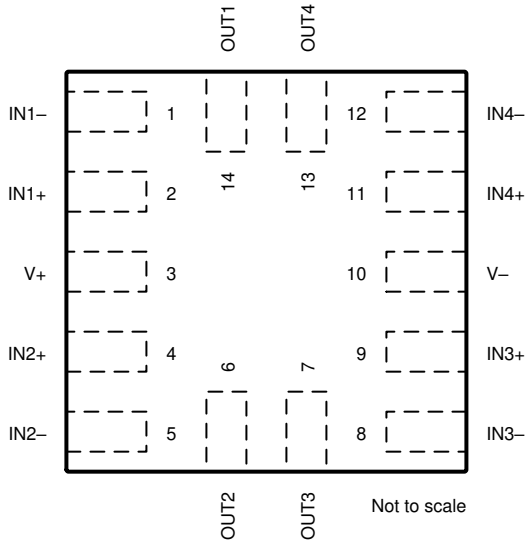


**図 5-9. OPA4991 RUC Package 14-Pin X2QFN (Top View)**

**表 5-5. Pin Functions: OPA4991**

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | SOIC, TSSOP, SOT-23 | X2QFN | | |
| IN1+ | 3 | 2 | I | Noninverting input, channel 1 |
| IN1– | 2 | 1 | I | Inverting input, channel 1 |
| IN2+ | 5 | 4 | I | Noninverting input, channel 2 |
| IN2– | 6 | 5 | I | Inverting input, channel 2 |
| IN3+ | 10 | 9 | I | Noninverting input, channel 3 |
| IN3– | 9 | 8 | I | Inverting input, channel 3 |
| IN4+ | 12 | 11 | I | Noninverting input, channel 4 |
| IN4– | 13 | 12 | I | Inverting input, channel 4 |
| NC | — | — | — | Do not connect |
| OUT1 | 1 | 14 | O | Output, channel 1 |
| OUT2 | 7 | 6 | O | Output, channel 2 |
| OUT3 | 8 | 7 | O | Output, channel 3 |
| OUT4 | 14 | 13 | O | Output, channel 4 |
| V+ | 4 | 3 | — | Positive (highest) power supply |
| V– | 11 | 10 | — | Negative (lowest) power supply |


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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) (1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_S$ = (V+) – (V–) | | 0 | 42 | V |
| Signal input pins | Common-mode voltage (3) | (V–) – 0.5 | (V+) + 0.5 | V |
| | Differential voltage (3) | | $V_S$ + 0.2 | V |
| | Current (3) | –10 | 10 | mA |
| Output short-circuit (2) | | Continuous | | |
| Operating ambient temperature, $T_A$ | | –55 | 150 | °C |
| Junction temperature, $T_J$ | | | 150 | °C |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |

(1) Operating the device beyond the ratings listed under *Absolute Maximum Ratings* will cause permanent damage to the device. These are stress ratings only, based on process and design limitations, and this device has not been designed to function outside the conditions indicated under *Recommended Operating Conditions*. Exposure to any condition outside *Recommended Operating Conditions* for extended periods, including absolute-maximum-rated conditions, may affect device reliability and performance.
(2) Short-circuit to ground, one amplifier per package. This device has been designed to limit *electrical* damage due to excessive output current, but extended short-circuit current, especially with higher supply voltage, can cause excessive heating and eventual *thermal* destruction. See the *Thermal Protection* section for more information.
(3) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101 (2) | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_S$ | Supply voltage, (V+) – (V–) | 2.7 | 40 | V |
| $V_I$ | Input voltage range | (V–) – 0.2 | (V+) + 0.2 | V |
| $V_{IH}$ | High level input voltage at shutdown pin (amplifier disabled) | (V–) + 1.1 | (V–) + 20 V(1) | V |
| $V_{IL}$ | Low level input voltage at shutdown pin (amplifier enabled) | (V–) | (V–) + 0.2 | V |
| $T_A$ | Specified temperature | –40 | 125 | °C |

(1) Cannot exceed V+.

## 6.4 Thermal Information for Single Channel

| THERMAL METRIC (1) | | OPA991, OPA991S | | | UNIT |
|---|---|---|---|---|---|
| | | DBV (SOT-23) | | DCK (SC70) | |
| | | 5 PINS | 6 PINS | 5 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 185.7 | 167.8 | 202.6 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 108.2 | 107.9 | 101.5 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 54.5 | 49.7 | 47.8 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 31.2 | 33.9 | 18.8 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 54.2 | 49.5 | 47.4 | °C/W |

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## 6.4 Thermal Information for Single Channel (continued)

| THERMAL METRIC (1) | | OPA991, OPA991S | | | UNIT |
|---|---|---|---|---|---|
| | | DBV (SOT-23) | | DCK (SC70) | |
| | | 5 PINS | 6 PINS | 5 PINS | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 6.5 Thermal Information for Dual Channel

| THERMAL METRIC (1) | | OPA2991, OPA2991S | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | D (SOIC) | DDF (SOT-23) | DGK (VSSOP) | DSG (WSON) | PW (TSSOP) | RUG (X2QFN) | |
| | | 8 PINS | 8 PINS | 8 PINS | 8 PINS | 8 PINS | 10 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 130.7 | 143.5 | 176.5 | 77.6 | 185.1 | 142.3 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 72.8 | 79.9 | 68.1 | 93.7 | 74.0 | 53.5 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 74.0 | 61.6 | 98.2 | 43.9 | 115.7 | 68.5 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 24.0 | 5.7 | 12.0 | 4.4 | 12.3 | 1.0 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 73.3 | 61.3 | 96.7 | 43.9 | 114.0 | 68.4 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | N/A | 19.0 | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 6.6 Thermal Information for Quad Channel

| THERMAL METRIC (1) | | OPA4991 | | | | UNIT |
|---|---|---|---|---|---|---|
| | | D (SOIC) | DYY (SOT-23) | PW (TSSOP) | RUC (X2QFN) | |
| | | 14 PINS | 14 PINS | 14 PINS | 14 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 101.4 | 110.6 | 131.4 | 125.9 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 57.6 | 53.7 | 51.8 | 39.8 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 57.3 | 35.3 | 75.8 | 68.0 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 18.5 | 2.2 | 7.9 | 0.8 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 56.9 | 35.0 | 74.8 | 67.8 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.


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## 6.7 Electrical Characteristics

For $V_S$ = (V+) – (V–) = 2.7 V to 40 V (±1.35 V to ±20 V) at $T_A$ = 25°C, $R_L$ = 10 kΩ connected to $V_S$ / 2, $V_{CM}$ = $V_S$ / 2, and $V_{OUT}$ = $V_S$ / 2, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | | |
| $V_{OS}$ | Input offset voltage | OPA991, OPA2991<br>$V_{CM}$ = V– | | | ±125 | ±750 | µV |
| | | | $T_A$ = –40°C to 125°C | | | ±780 | |
| | | OPA4991<br>$V_{CM}$ = V– | | | ±125 | ±830 | |
| | | | $T_A$ = –40°C to 125°C | | | ±850 | |
| $dV_{OS}/dT$ | Input offset voltage drift | | $T_A$ = –40°C to 125°C | | ±0.3 | | µV/°C |
| PSRR | Input offset voltage versus power supply | $V_{CM}$ = V–, $V_S$ = 4 V to 40 V | $T_A$ = –40°C to 125°C | | ±0.3 | ±1 | µV/V |
| | | $V_{CM}$ = V–, $V_S$ = 2.7 V to 40 V[2] | | | ±1 | ±5 | |
| | Channel separation | f = 0 Hz | | | 5 | | µV/V |
| **INPUT BIAS CURRENT** | | | | | | | |
| $I_B$ | Input bias current | | | | ±10 | | pA |
| $I_{OS}$ | Input offset current | | | | ±10 | | pA |
| **NOISE** | | | | | | | |
| $E_N$ | Input voltage noise | f = 0.1 Hz to 10 Hz | | | 1.8 | | $\mu V_{PP}$ |
| | | | | | 0.3 | | $\mu V_{RMS}$ |
| $e_N$ | Input voltage noise density | f = 1 kHz | | | 10.8 | | nV/√Hz |
| | | f = 10 kHz | | | 9.4 | | |
| $i_N$ | Input current noise | f = 1 kHz | | | 2 | | fA/√Hz |
| **INPUT VOLTAGE RANGE** | | | | | | | |
| $V_{CM}$ | Common-mode voltage range | | | (V–) – 0.1 | | (V+) + 0.1 | V |
| CMRR | Common-mode rejection ratio | $V_S$ = 40 V, (V–) – 0.1 V < $V_{CM}$ < (V+) – 2 V (Main input pair) | $T_A$ = –40°C to 125°C | 109 | 130 | | dB |
| | | $V_S$ = 4 V, (V–) – 0.1 V < $V_{CM}$ < (V+) – 2 V (Main input pair) | | 84 | 100 | | |
| | | $V_S$ = 2.7 V, (V–) – 0.1 V < $V_{CM}$ < (V+) – 2 V (Main input pair)[2] | | 75 | 95 | | |
| | | $V_S$ = 2.7 V to 40 V, (V+) – 1 V < $V_{CM}$ < (V+) + 0.1 V (Aux input pair) | | | 85 | | |
| **INPUT CAPACITANCE** | | | | | | | |
| $Z_{ID}$ | Differential | | | | 540 \|\| 9 | | GΩ \|\| pF |
| $Z_{ICM}$ | Common-mode | | | | 6 \|\| 1 | | TΩ \|\| pF |

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## 6.7 Electrical Characteristics (continued)

For $V_S$ = (V+) – (V–) = 2.7 V to 40 V (±1.35 V to ±20 V) at $T_A$ = 25°C, $R_L$ = 10 kΩ connected to $V_S$ / 2, $V_{CM}$ = $V_S$ / 2, and $V_{OUT}$ = $V_S$ / 2, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **OPEN-LOOP GAIN** | | | | | | | |
| $A_{OL}$ | Open-loop voltage gain | $V_S$ = 40 V, $V_{CM}$ = V– (V–) + 0.1 V < $V_O$ < (V+) – 0.1 V | | 120 | 145 | | dB |
| | | | $T_A$ = –40°C to 125°C | | 142 | | |
| | | $V_S$ = 4 V, $V_{CM}$ = V– (V–) + 0.1 V < $V_O$ < (V+) – 0.1 V | | 104 | 130 | | |
| | | | $T_A$ = –40°C to 125°C | | 125 | | |
| | | $V_S$ = 2.7 V, $V_{CM}$ = V– (V–) + 0.1 V < $V_O$ < (V+) – 0.1 V[2] | | 101 | 120 | | |
| | | | $T_A$ = –40°C to 125°C | | 118 | | |
| **FREQUENCY RESPONSE** | | | | | | | |
| GBW | Gain-bandwidth product | | | | 4.5 | | MHz |
| SR | Slew rate | $V_S$ = 40 V, G = +1, $C_L$ = 20 pF | | | 21 | | V/µs |
| $t_S$ | Settling time | To 0.01%, $V_S$ = 40 V, $V_{STEP}$ = 10 V , G = +1, CL = 20 pF | | | 2.5 | | µs |
| | | To 0.01%, $V_S$ = 40 V, $V_{STEP}$ = 2 V , G = +1, CL = 20 pF | | | 1.5 | | |
| | | To 0.1%, $V_S$ = 40 V, $V_{STEP}$ = 10 V , G = +1, CL = 20 pF | | | 2 | | |
| | | To 0.1%, $V_S$ = 40 V, $V_{STEP}$ = 2 V , G = +1, CL = 20 pF | | | 1 | | |
| | Phase margin | G = +1, $R_L$ = 10 kΩ | | | 60 | | ° |
| | Overload recovery time | $V_{IN}$ × gain > $V_S$ | | | 400 | | ns |
| THD+N | Total harmonic distortion + noise | $V_S$ = 40 V, $V_O$ = 3 $V_{RMS}$, G = 1, f = 1 kHz | | | 0.00021% | | |
| **OUTPUT** | | | | | | | |
| | Voltage output swing from rail | Positive and negative rail headroom | $V_S$ = 40 V, $R_L$ = no load[2] | | 5 | 10 | mV |
| | | | $V_S$ = 40 V, $R_L$ = 10 kΩ | | 50 | 55 | |
| | | | $V_S$ = 40 V, $R_L$ = 2 kΩ | | 200 | 250 | |
| | | | $V_S$ = 2.7 V, $R_L$ = no load[2] | | 1 | 6 | |
| | | | $V_S$ = 2.7 V, $R_L$ = 10 kΩ | | 5 | 12 | |
| | | | $V_S$ = 2.7 V, $R_L$ = 2 kΩ | | 25 | 40 | |
| $I_{SC}$ | Short-circuit current | | | | ±75 | | mA |
| $C_{LOAD}$ | Capacitive load drive | | | | 1000 | | pF |
| $Z_O$ | Open-loop output impedance | f = 1 MHz, $I_O$ = 0 A | | | 525 | | Ω |


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## 6.7 Electrical Characteristics (continued)

For $V_S$ = (V+) – (V–) = 2.7 V to 40 V (±1.35 V to ±20 V) at $T_A$ = 25°C, $R_L$ = 10 kΩ connected to $V_S$ / 2, $V_{CM}$ = $V_S$ / 2, and $V_{OUT}$ = $V_S$ / 2, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | | |
| $I_Q$ | Quiescent current per amplifier | $V_{CM}$ = V–, $I_O$ = 0 A | | | 560 | 685 | µA |
| | | | $T_A$ = –40°C to 125°C | | | 750 | |
| **SHUTDOWN** | | | | | | | |
| $I_{QSD}$ | Quiescent current per amplifier | $V_S$ = 2.7 V to 40 V, all amplifiers disabled, SHDN = V– + 2 V | | | 30 | 45 | µA |
| $Z_{SHDN}$ | Output impedance during shutdown | $V_S$ = 2.7 V to 40 V, amplifier disabled, SHDN = V– + 2 V | | | 320 \|\| 2 | | MΩ \|\| pF |
| $V_{IH}$ | Logic high threshold voltage (amplifier disabled) | For valid input high, the SHDN pin voltage should be greater than the maximum threshold but less than or equal to (V–) + 20 V | | | (V–) + 0.8 | (V–) + 1.1 | V |
| $V_{IL}$ | Logic low threshold voltage (amplifier enabled) | For valid input low, the SHDN pin voltage should be less than the minimum threshold but greater than or equal to V– | | (V–) + 0.2 | (V–) + 0.8 | | V |
| $t_{ON}$ | Amplifier enable time (1) | G = +1, $V_{CM}$ = V-, $V_O$ = 0.1 × $V_S$/2 | | | 8 | | µs |
| $t_{OFF}$ | Amplifier disable time (1) | $V_{CM}$ = V-, $V_O$ = $V_S$/2 | | | 3 | | µs |
| | SHDN pin input bias current (per pin) | $V_S$ = 2.7 V to 40 V, (V–) + 20 V ≥ SHDN ≥ (V–) + 0.9 V | | | 500 | | nA |
| | | $V_S$ = 2.7 V to 40 V, (V–) ≤ SHDN ≤ (V–) + 0.7 V | | | 150 | | |

(1) Disable time ($t_{OFF}$) and enable time ($t_{ON}$) are defined as the time interval between the 50% point of the signal applied to the SHDN pin and the point at which the output voltage reaches the 10% (disable) or 90% (enable) level.
(2) Specified by characterization only.

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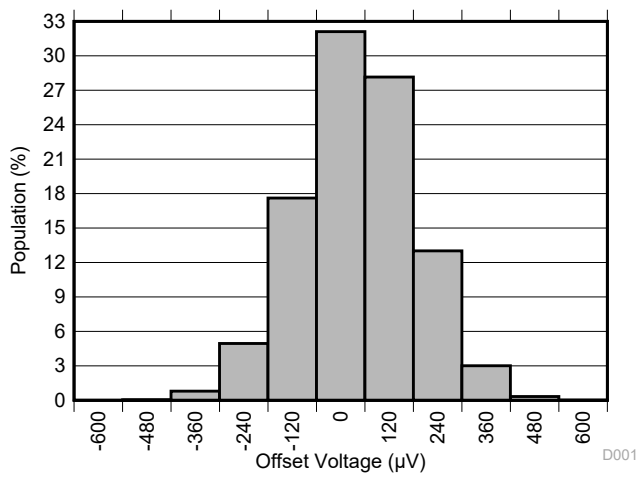
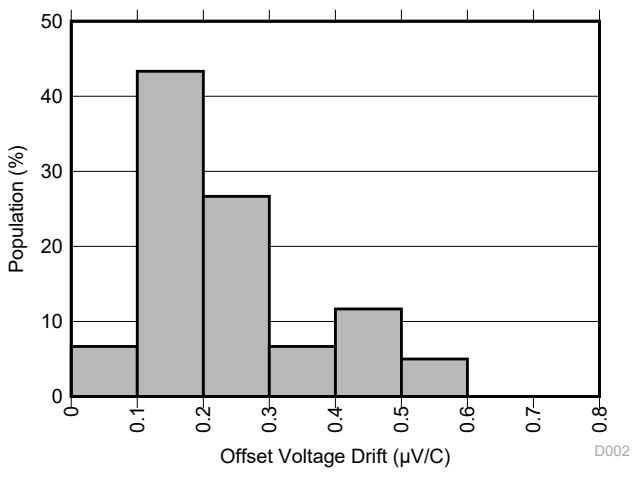
## 6.8 Typical Characteristics

at $T_A$ = 25°C, $V_S$ = ±20 V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10 kΩ connected to $V_S$ / 2, and $C_L$ = 10 pF (unless otherwise noted)



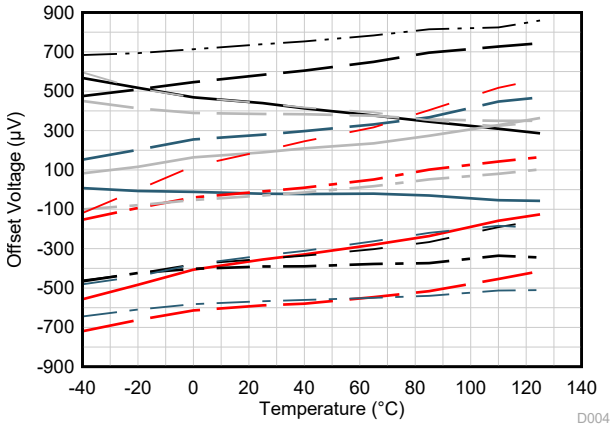

Distribution from 15462 amplifiers, $T_A$ = 25°C

**図 6-1. Offset Voltage Production Distribution**



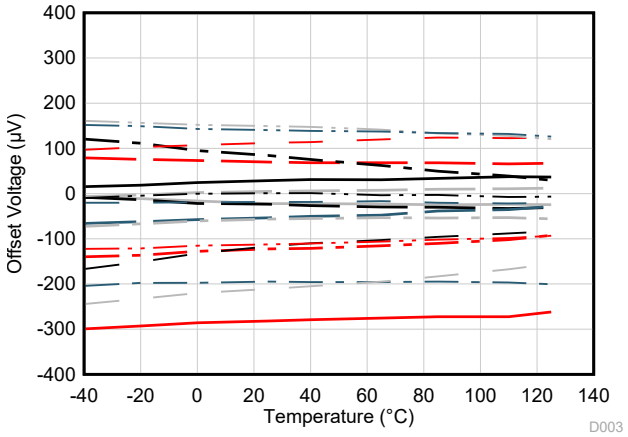

Distribution from 60 amplifiers

**図 6-2. Offset Voltage Drift Distribution**



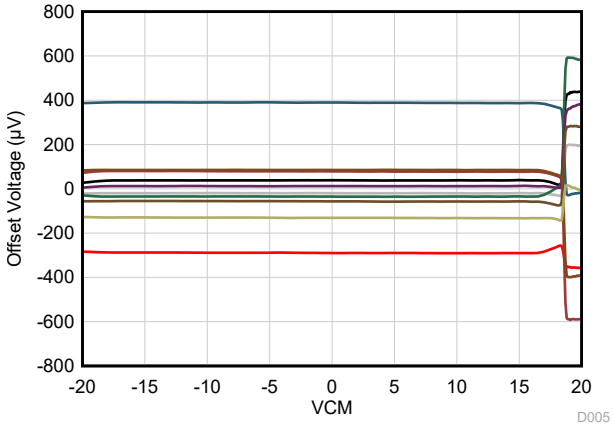

$V_{CM}$ = V+

**図 6-3. Offset Voltage vs Temperature**



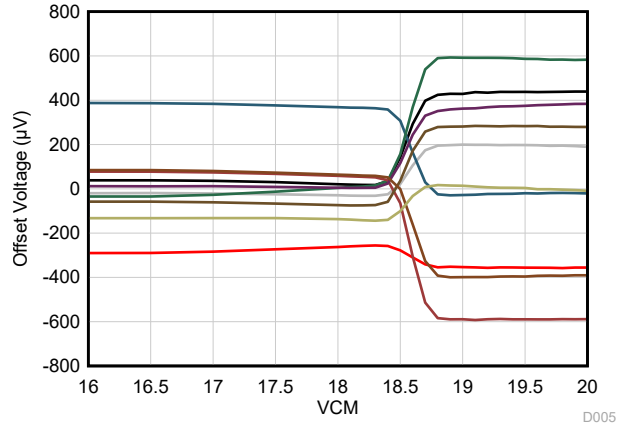

$V_{CM}$ = V–

**図 6-4. Offset Voltage vs Temperature**




$T_A$ = 25°C

**図 6-5. Offset Voltage vs Common-Mode Voltage**




$T_A$ = 25°C

**図 6-6. Offset Voltage vs Common-Mode Voltage (Transition Region)**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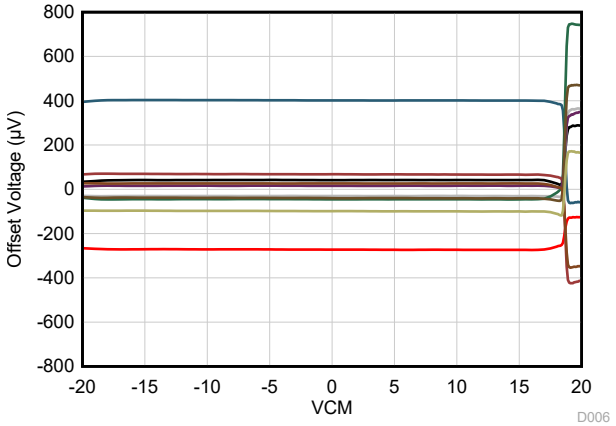
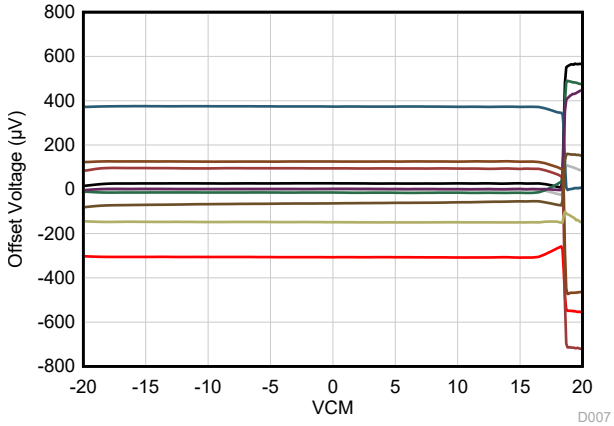
## 6.8 Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = ±20 V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10 kΩ connected to $V_S$ / 2, and $C_L$ = 10 pF (unless otherwise noted)




$T_A$ = 125°C

**図 6-7. Offset Voltage vs Common-Mode Voltage**




$T_A$ = –40°C

**図 6-8. Offset Voltage vs Common-Mode Voltage**

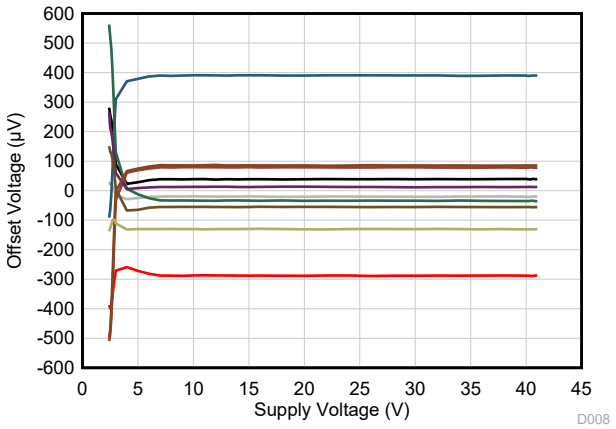
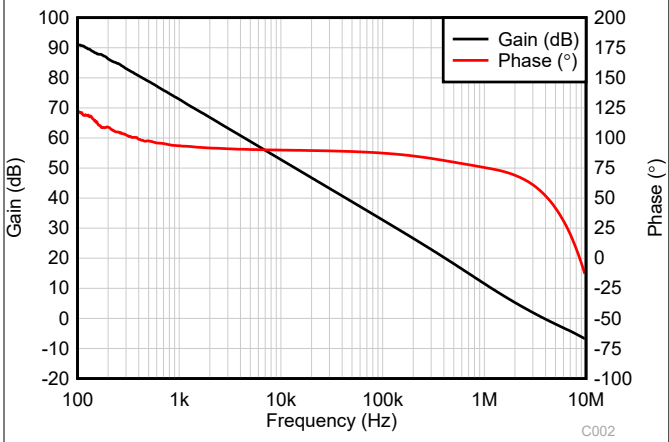



**図 6-9. Offset Voltage vs Power Supply**




$C_L$ = 20 pF

**図 6-10. Open-Loop Gain and Phase vs Frequency**

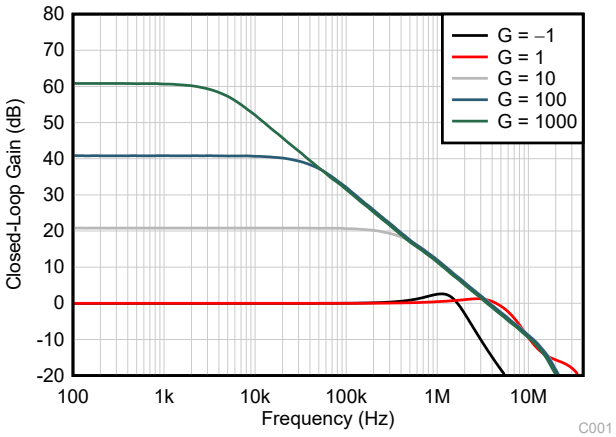



**図 6-11. Closed-Loop Gain vs Frequency**

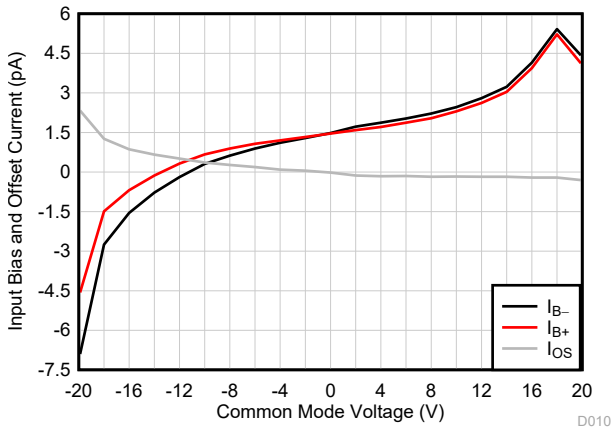



**図 6-12. Input Bias Current vs Common-Mode Voltage**

## 6.8 Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = ±20 V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10 kΩ connected to $V_S$ / 2, and $C_L$ = 10 pF (unless otherwise noted)

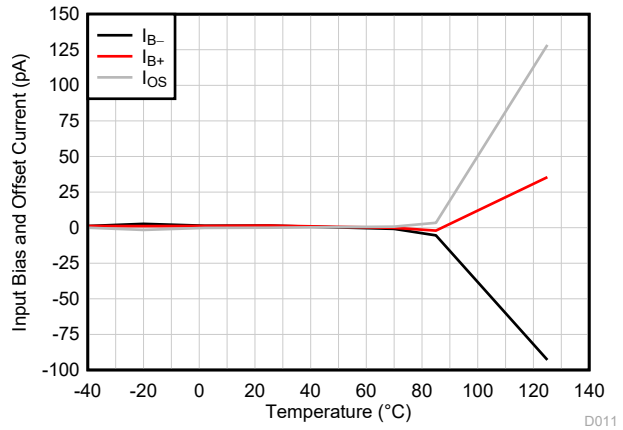



**図 6-13. Input Bias Current vs Temperature**

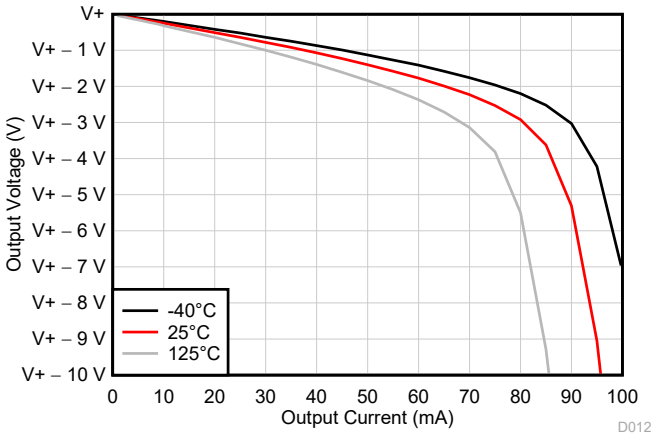



**図 6-14. Output Voltage Swing vs Output Current (Sourcing)**

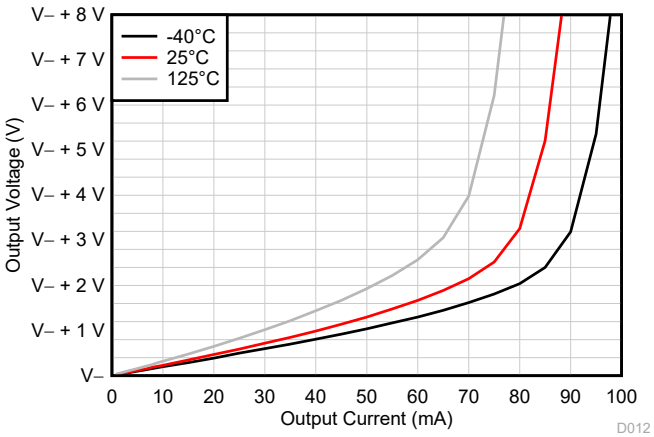



**図 6-15. Output Voltage Swing vs Output Current (Sinking)**

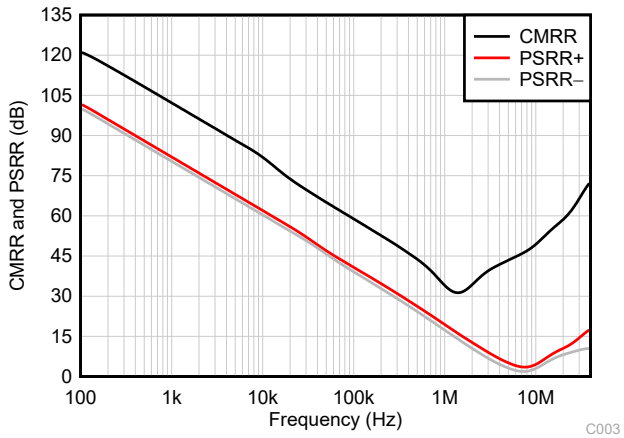
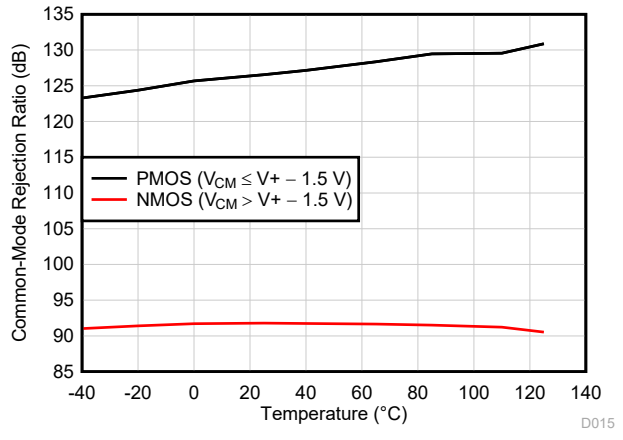
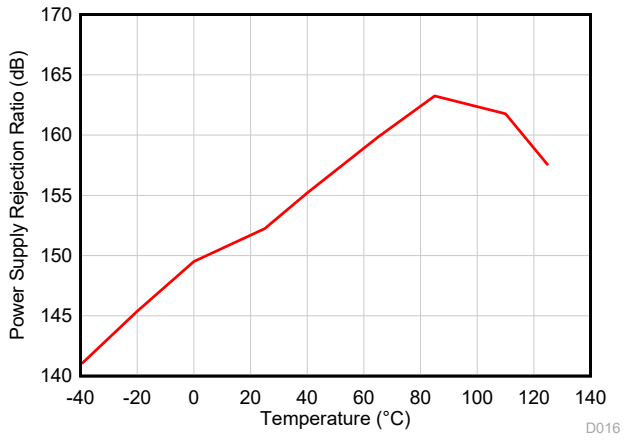



**図 6-16. CMRR and PSRR vs Frequency**




f = 0 Hz

**図 6-17. CMRR vs Temperature (dB)**




f = 0 Hz

**図 6-18. PSRR vs Temperature (dB)**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## 6.8 Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = ±20 V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10 kΩ connected to $V_S$ / 2, and $C_L$ = 10 pF (unless otherwise noted)

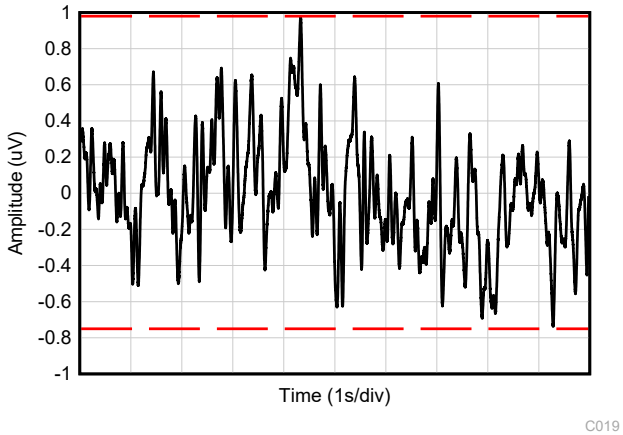



図 6-19. 0.1-Hz to 10-Hz Noise

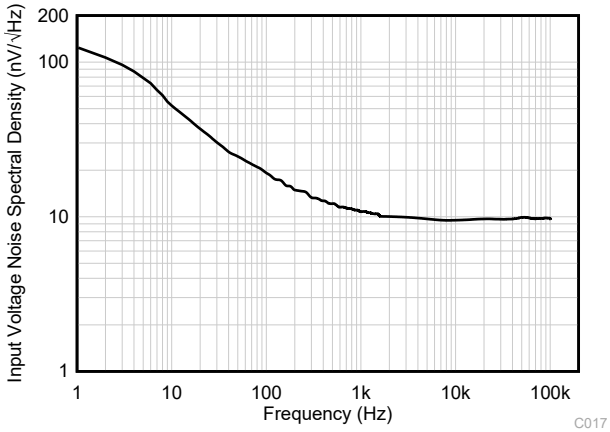
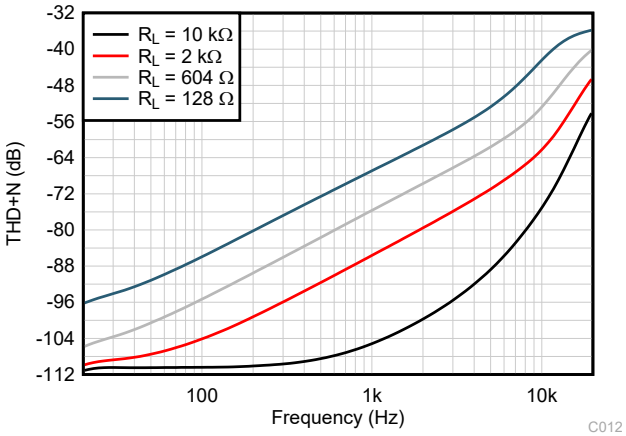
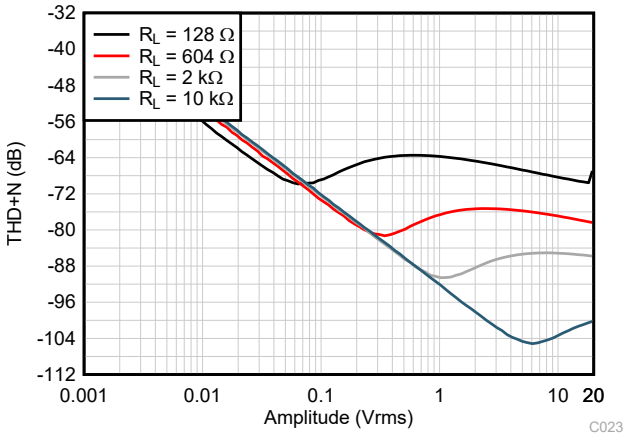



図 6-20. Input Voltage Noise Spectral Density vs Frequency



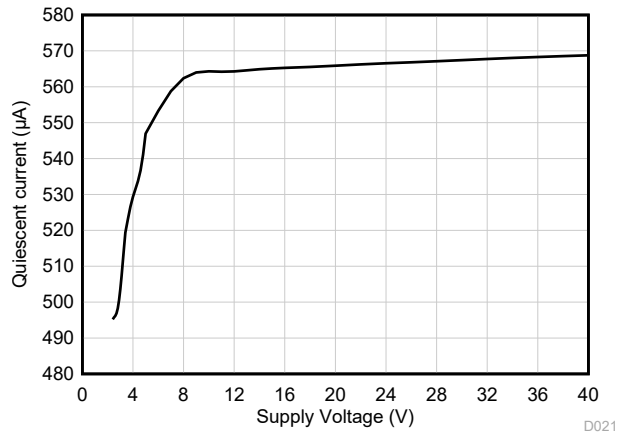

BW = 80 kHz, $V_{OUT}$ = 1 $V_{RMS}$

図 6-21. THD+N Ratio vs Frequency




BW = 80 kHz, f = 1 kHz

図 6-22. THD+N vs Output Amplitude




$V_{CM}$ = V–

図 6-23. Quiescent Current vs Supply Voltage

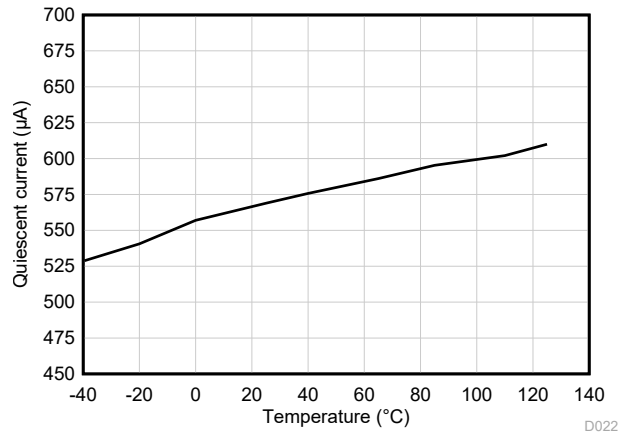



図 6-24. Quiescent Current vs Temperature

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## 6.8 Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = ±20 V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10 kΩ connected to $V_S$ / 2, and $C_L$ = 10 pF (unless otherwise noted)

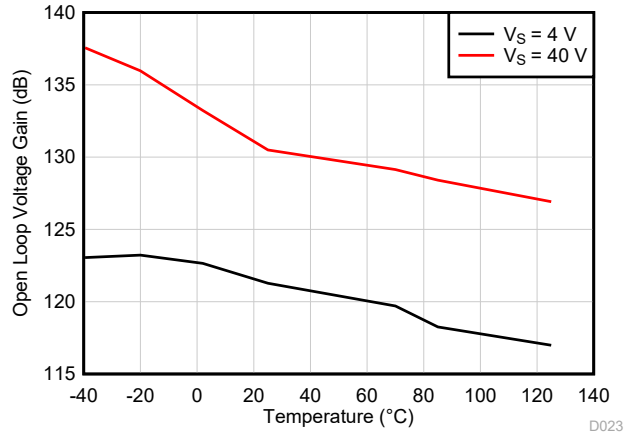



図 6-25. Open-Loop Voltage Gain vs Temperature (dB)

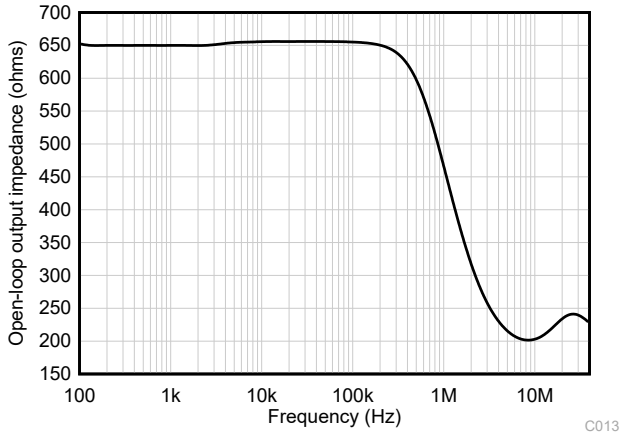
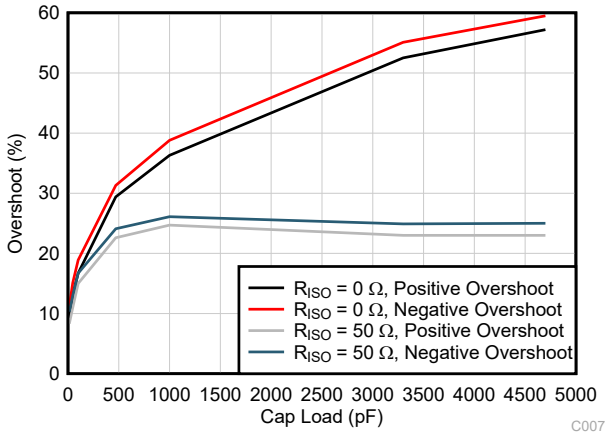
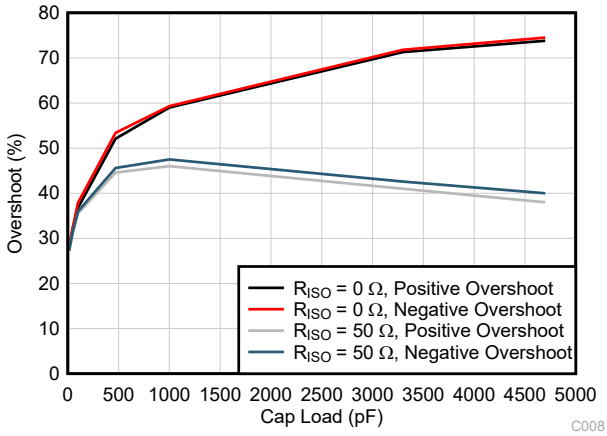



図 6-26. Open-Loop Output Impedance vs Frequency




G = –1, 10-mV output step

図 6-27. Small-Signal Overshoot vs Capacitive Load




G = 1, 10-mV output step

図 6-28. Small-Signal Overshoot vs Capacitive Load

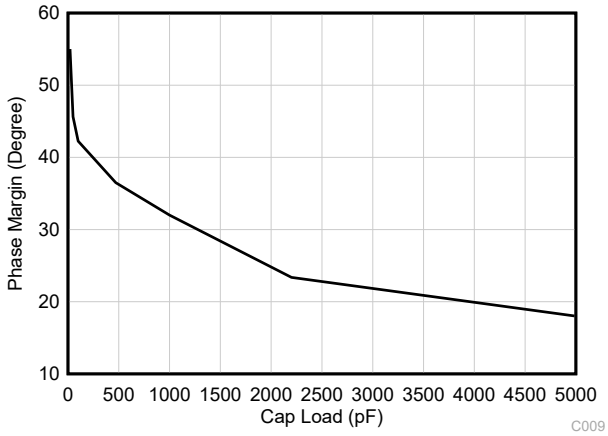
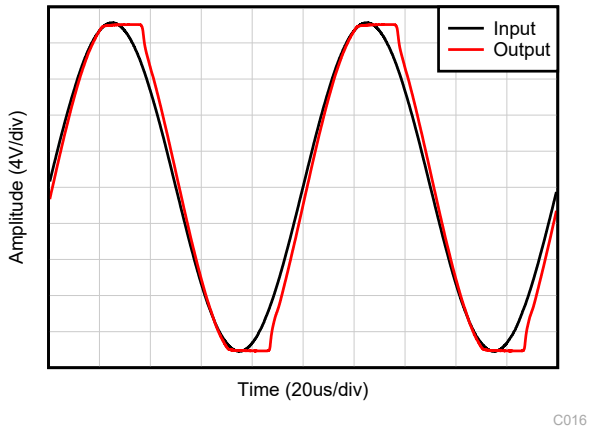



図 6-29. Phase Margin vs Capacitive Load




$V_{IN}$ = ±20 V; $V_S$ = $V_{OUT}$ = ±17 V

図 6-30. No Phase Reversal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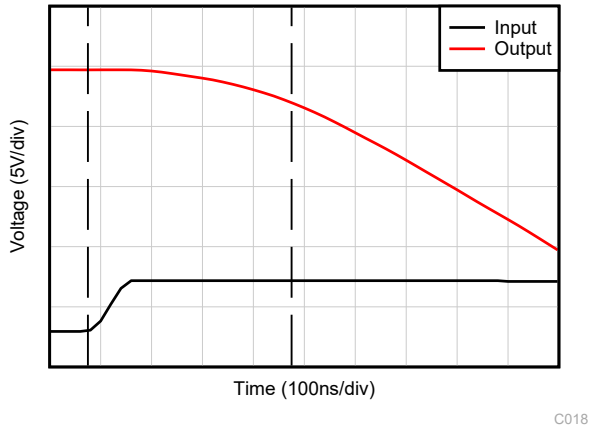
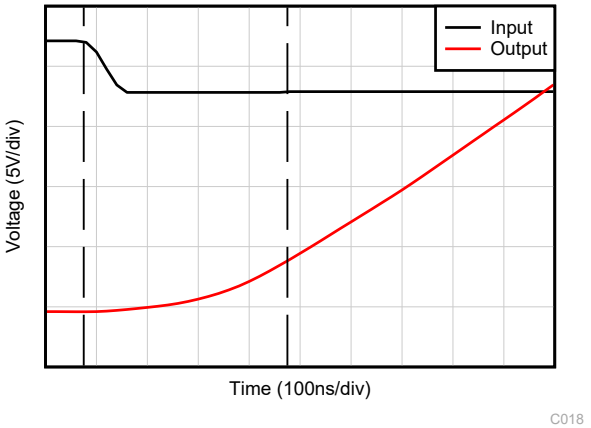
## 6.8 Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = ±20 V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10 kΩ connected to $V_S$ / 2, and $C_L$ = 10 pF (unless otherwise noted)



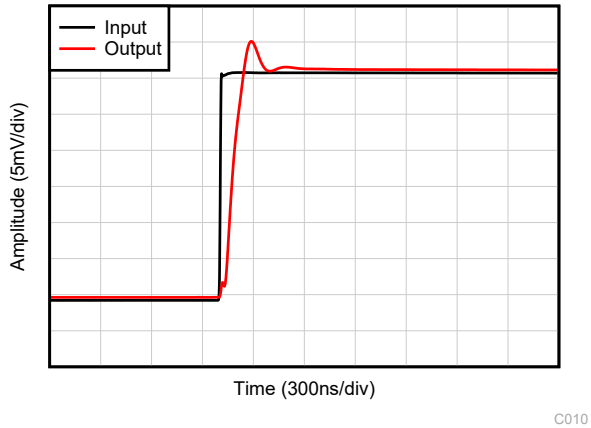

G = –10

**図 6-31. Positive Overload Recovery**



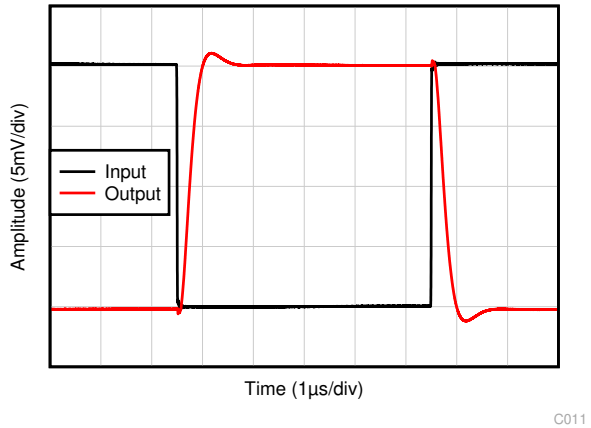

G = –10

**図 6-32. Negative Overload Recovery**



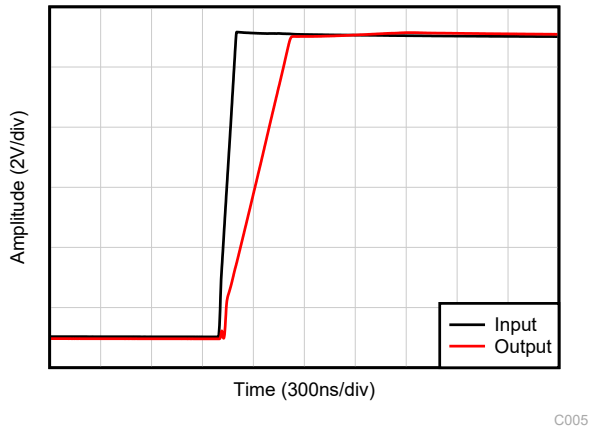

$C_L$ = 20 pF, G = 1, 20-mV step response

**図 6-33. Small-Signal Step Response, Rising**



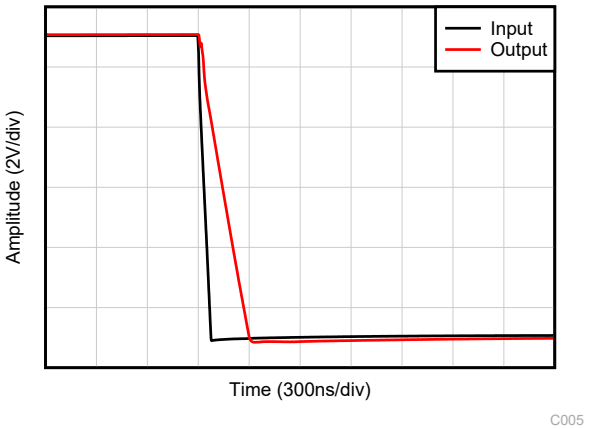

$C_L$ = 20 pF, G = 1, 20-mV step response

**図 6-34. Small-Signal Step Response, Falling**




$C_L$ = 20 pF, G = 1

**図 6-35. Large-Signal Step Response (Rising)**




$C_L$ = 20 pF, G = 1

**図 6-36. Large-Signal Step Response (Falling)**

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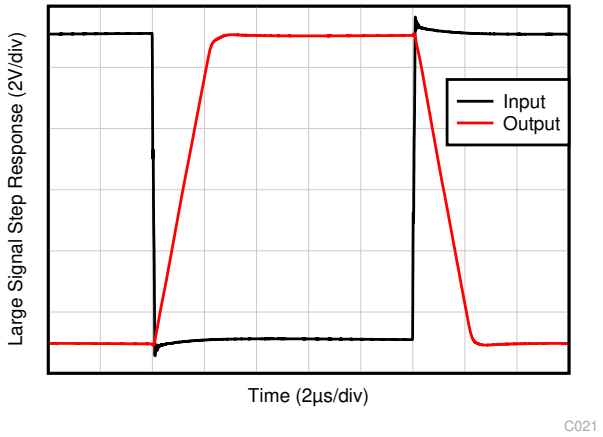
## 6.8 Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = ±20 V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10 kΩ connected to $V_S$ / 2, and $C_L$ = 10 pF (unless otherwise noted)




$C_L$ = 20 pF, G = –1

**図 6-37. Large-Signal Step Response**

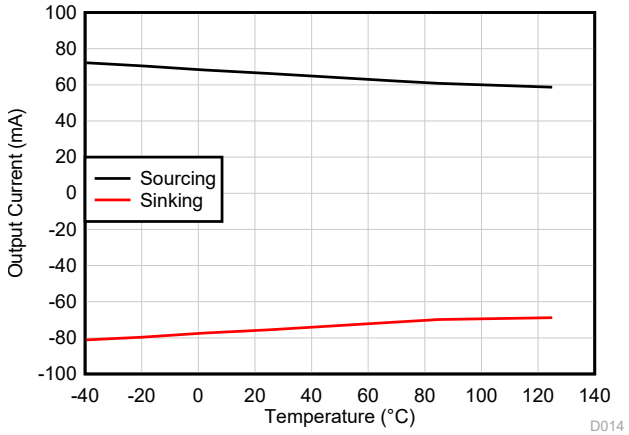



**図 6-38. Short-Circuit Current vs Temperature**

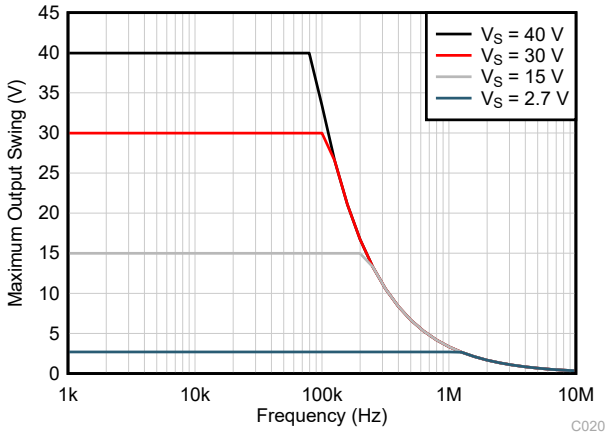



**図 6-39. Maximum Output Voltage vs Frequency**

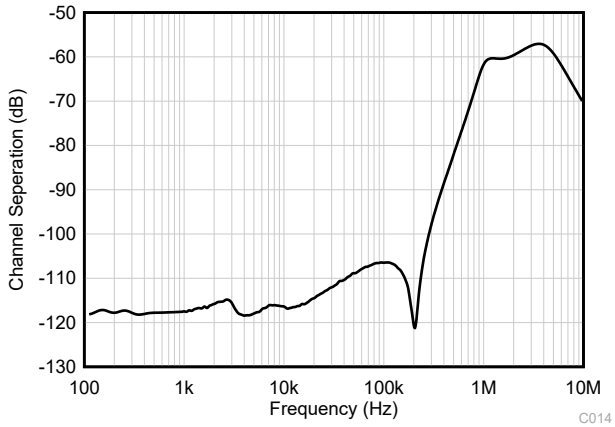



**図 6-40. Channel Separation vs Frequency**

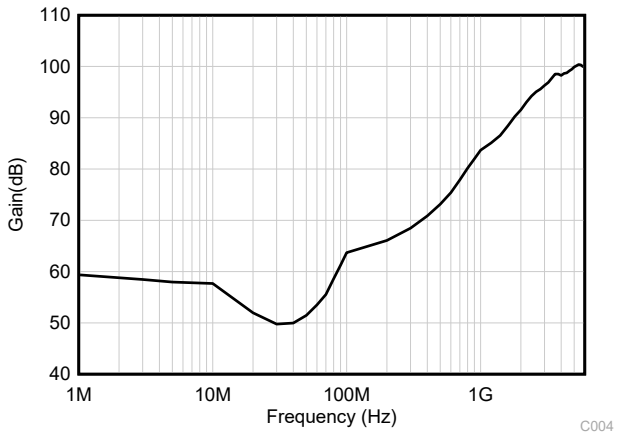



**図 6-41. EMIRR (Electromagnetic Interference Rejection Ratio) vs Frequency**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# 7 Detailed Description

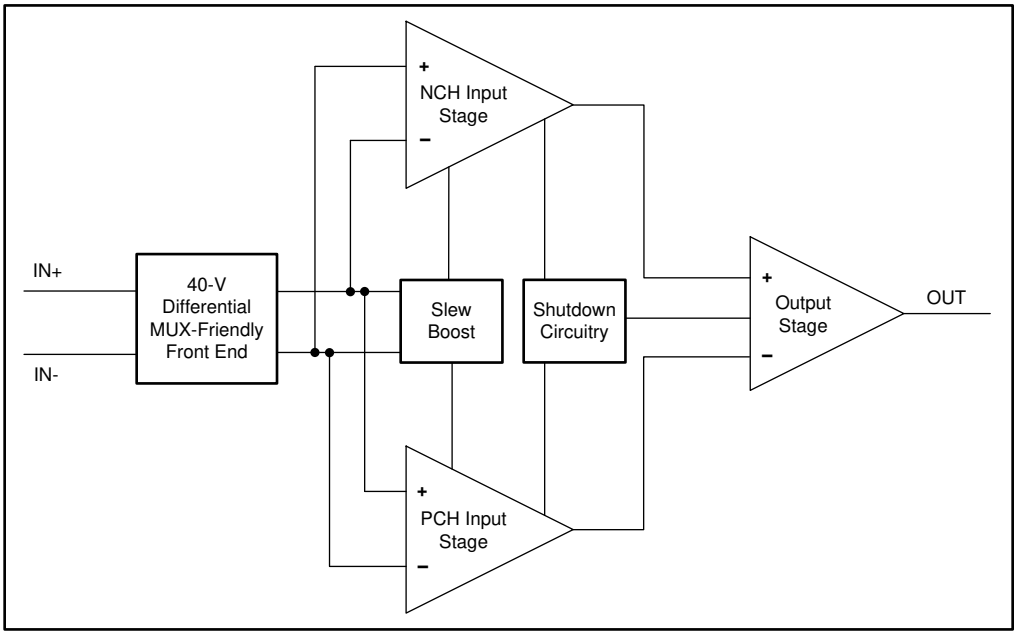
## 7.1 Overview

The OPAx991 family (OPA991, OPA2991, and OPA4991) is a new generation of 40-V general purpose operational amplifiers.

These devices offer excellent DC precision and AC performance, including rail-to-rail input/output, low offset (±125 µV, typ), low offset drift (±0.3 µV/°C, typ), and 4.5-MHz bandwidth.

Unique features such as differential and common-mode input-voltage range to the supply rail, high output current (±75 mA), high slew rate (21 V/µs), and shutdown functionality make the OPAx991 a robust, high-performance operational amplifier for high-voltage industrial applications.

## 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Input Protection Circuitry

The OPAx991 uses a unique input architecture to eliminate the requirement for input protection diodes but still provides robust input protection under transient conditions. 図 7-1 shows conventional input diode protection schemes that are activated by fast transient step responses and introduce signal distortion and settling time delays because of alternate current paths, as shown in 図 7-2. For low-gain circuits, these fast-ramping input signals forward-bias back-to-back diodes, causing an increase in input current and resulting in extended settling time.

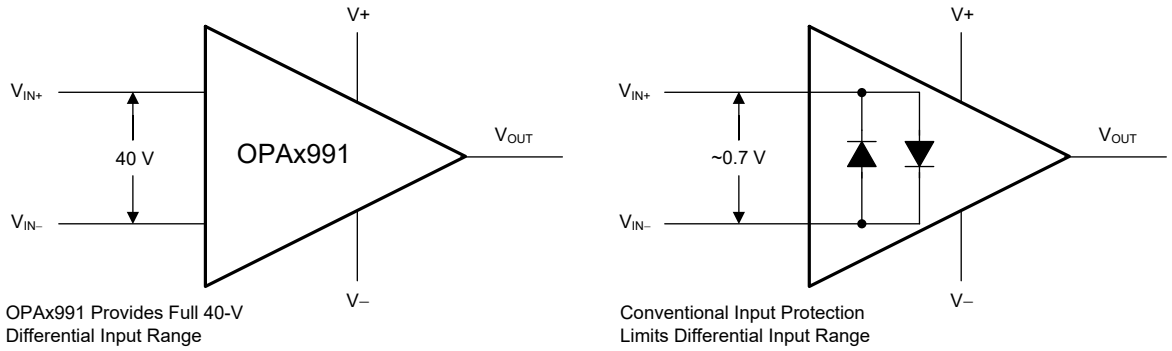



**図 7-1. OPAx991 Input Protection Does Not Limit Differential Input Capability**

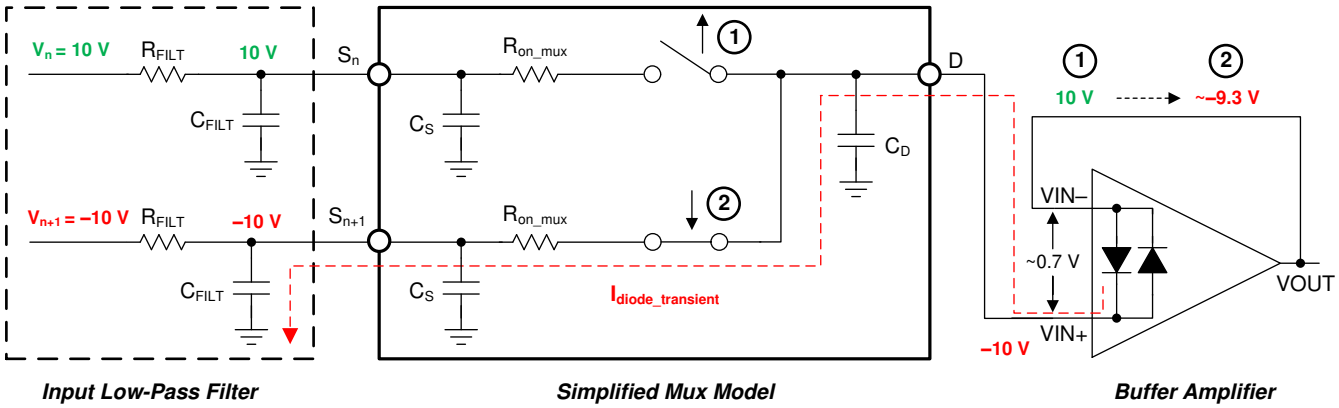



**図 7-2. Back-to-Back Diodes Create Settling Issues**

The OPAx991 family of operational amplifiers provides a true high-impedance differential input capability for high-voltage applications using a patented input protection architecture that does not introduce additional signal distortion or delayed settling time, making the device an optimal op amp for multichannel, high-switched, input applications. The OPA991 tolerates a maximum differential swing (voltage between inverting and non-inverting pins of the op amp) of up to 40 V, making the device suitable for use as a comparator or in applications with fast-ramping input signals such as data-acquisition systems; see the TI TechNote *MUX-Friendly Precision Operational Amplifiers* for more information.

### 7.3.2 EMI Rejection

The OPAx991 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx991 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. 図 7-3 shows the results of this testing on the OPAx991. 表 7-1 shows the EMIRR IN+ values for the OPAx991 at particular frequencies commonly encountered in real-world applications. The *EMI Rejection Ratio of Operational*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*Amplifiers* application report contains detailed information on the topic of EMIRR performance as it relates to op amps and is available for download from www.ti.com.

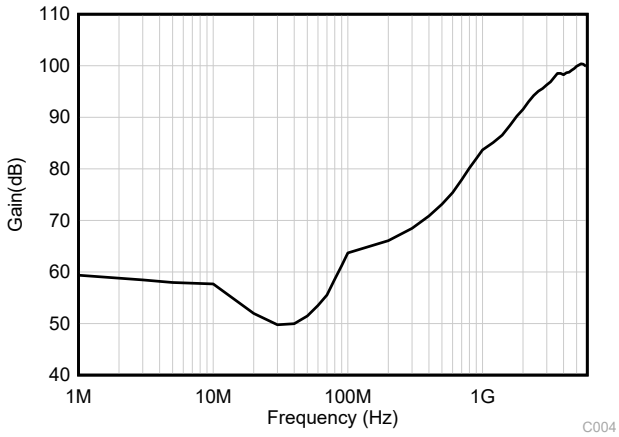


**図 7-3. EMIRR Testing**

**表 7-1. OPA991 EMIRR IN+ for Frequencies of Interest**

| FREQUENCY | APPLICATION OR ALLOCATION | EMIRR IN+ |
|---|---|---|
| 400 MHz | Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications | 73.2 dB |
| 900 MHz | Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications | 82.5 dB |
| 1.8 GHz | GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz) | 89.7 dB |
| 2.4 GHz | 802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz) | 93.9 dB |
| 3.6 GHz | Radiolocation, aero communication and navigation, satellite, mobile, S-band | 95.7 dB |
| 5 GHz | 802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz) | 98.0 dB |

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### 7.3.3 Thermal Protection

The internal power dissipation of any amplifier causes its internal (junction) temperature to rise. This phenomenon is called *self heating*. The absolute maximum junction temperature of the OPAx991 is 150°C. Exceeding this temperature causes damage to the device. The OPAx991 has a thermal protection feature that reduces damage from self heating. The protection works by monitoring the temperature of the device and turning off the op amp output drive for temperatures above 170°C. 図 7-4 shows an application example for the OPA991 that has significant self heating because of its power dissipation (0.81 W). Thermal calculations indicate that for an ambient temperature of 65°C, the device junction temperature must reach 177°C. The actual device, however, turns off the output drive to recover towards a safe junction temperature. 図 7-4 shows how the circuit behaves during thermal protection. During normal operation, the device acts as a buffer so the output is 3 V. When self heating causes the device junction temperature to increase above the internal limit, the thermal protection forces the output to a high-impedance state and the output is pulled to ground through resistor $R_L$. If the condition that caused excessive power dissipation is not removed, the amplifier will oscillate between a shutdown and enabled state until the output fault is corrected.

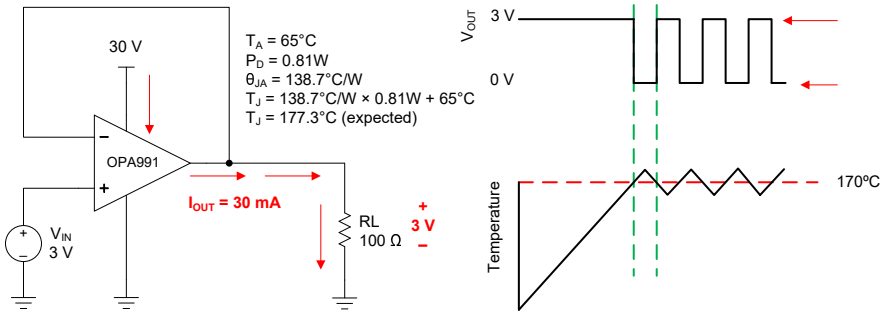


**図 7-4. Thermal Protection**

If the device continues to operate at high junction temperatures with high output power over a long period of time, regardless if the device is or is not entering thermal shutdown, the thermal dissipation of the device can slowly degrade performance of the device and eventually cause catastrophic destruction. Designers should be careful to limit output power of the device at high temperatures, or control ambient and junction temperatures under high output power conditions.

### 7.3.4 Capacitive Load and Stability

The OPAx991 features a resistive output stage capable of driving moderate capacitive loads, and by leveraging an isolation resistor, the device can easily be configured to drive large capacitive loads. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads; see 図 7-5 and 図 7-6. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier will be stable in operation.


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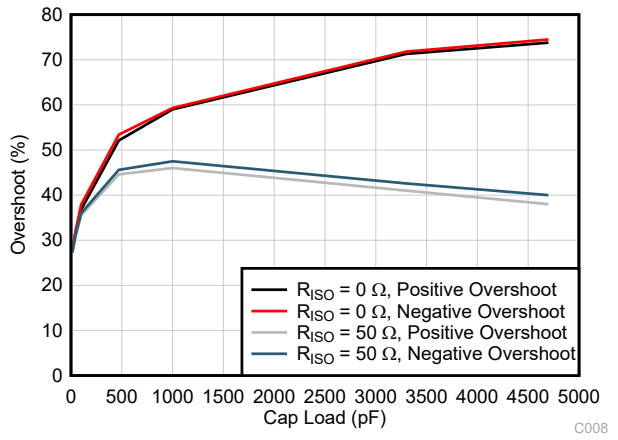


**図 7-5. Small-Signal Overshoot vs Capacitive Load (10-mV Output Step, G = 1)**

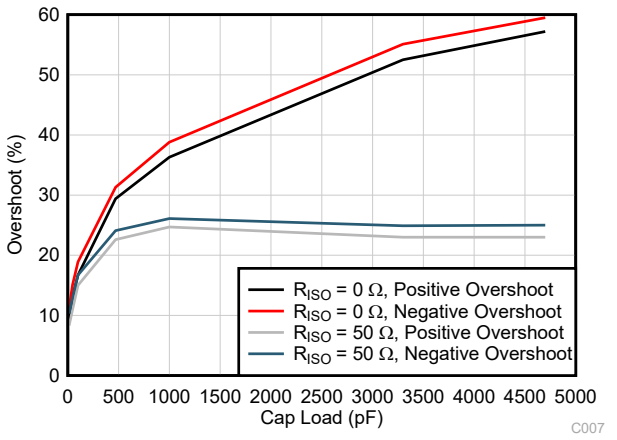


**図 7-6. Small-Signal Overshoot vs Capacitive Load (10-mV Output Step, G = –1)**

For additional drive capability in unity-gain configurations, improve capacitive load drive by inserting a small resistor, $R_{ISO}$, in series with the output, as shown in 図 7-7. This resistor significantly reduces ringing and maintains DC performance for purely capacitive loads. However, if a resistive load is in parallel with the capacitive load, then a voltage divider is created, thus introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio $R_{ISO}$ / $R_L$, and is generally negligible at low output levels. A high capacitive load drive makes the OPAx991 well suited for applications such as reference buffers, MOSFET gate drives, and cable-shield drives. The circuit shown in 図 7-7 uses an isolation resistor, $R_{ISO}$, to stabilize the output of an op amp. $R_{ISO}$ modifies the open-loop gain of the system for increased phase margin.

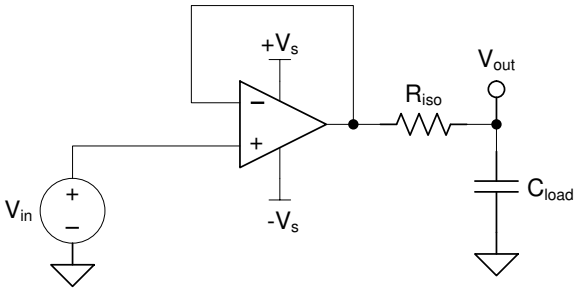


**図 7-7. Extending Capacitive Load Drive With the OPA991**

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### 7.3.5 Common-Mode Voltage Range

The OPAx991 is a 40-V, true rail-to-rail input operational amplifier with an input common-mode range that extends 100 mV beyond either supply rail. This wide range is achieved with paralleled complementary N-channel and P-channel differential input pairs, as shown in 図 7-8. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1 V to 100 mV above the positive supply. The P-channel pair is active for inputs from 100 mV below the negative supply to approximately (V+) – 2 V. There is a small transition region, typically (V+) – 2 V to (V+) – 1 V in which both input pairs are on. This transition region can vary modestly with process variation, and within this region PSRR, CMRR, offset voltage, offset drift, noise, and THD performance may be degraded compared to operation outside this region.

図 6-5 shows this transition region for a typical device in terms of input voltage offset in more detail.

For more information on common-mode voltage range and PMOS/NMOS pair interaction, see *Op Amps With Complementary-Pair Input Stages* application note.

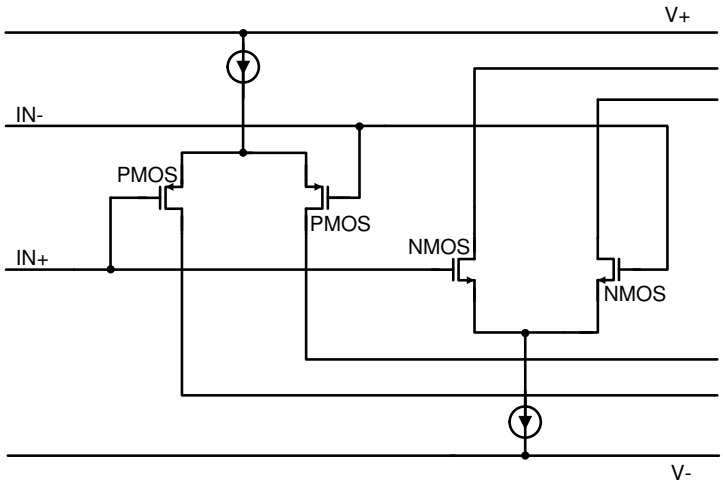


**図 7-8. Rail-to-Rail Input Stage**

### 7.3.6 Phase Reversal Protection

The OPAx991 family has internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in non-inverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The OPAx991 is a rail-to-rail input op amp; therefore, the common-mode range can extend up to the rails. Input signals beyond the rails do not cause phase reversal; instead, the output limits into the appropriate rail. This performance is shown in 図 7-9. For more information on phase reversal, see *Op Amps With Complementary-Pair Input Stages* application note.


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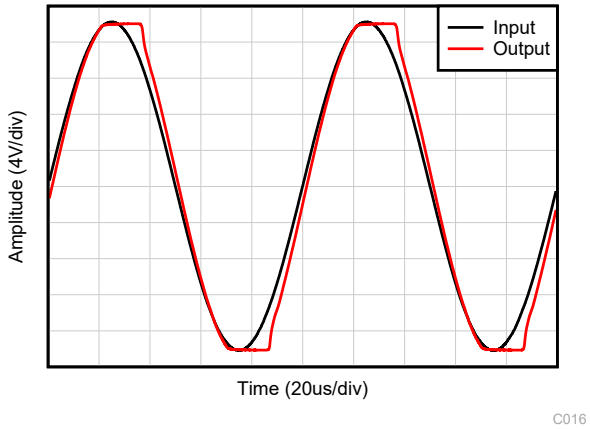


**図 7-9. No Phase Reversal**

### 7.3.7 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. 図 7-10 shows an illustration of the ESD circuits contained in the OPAx991 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

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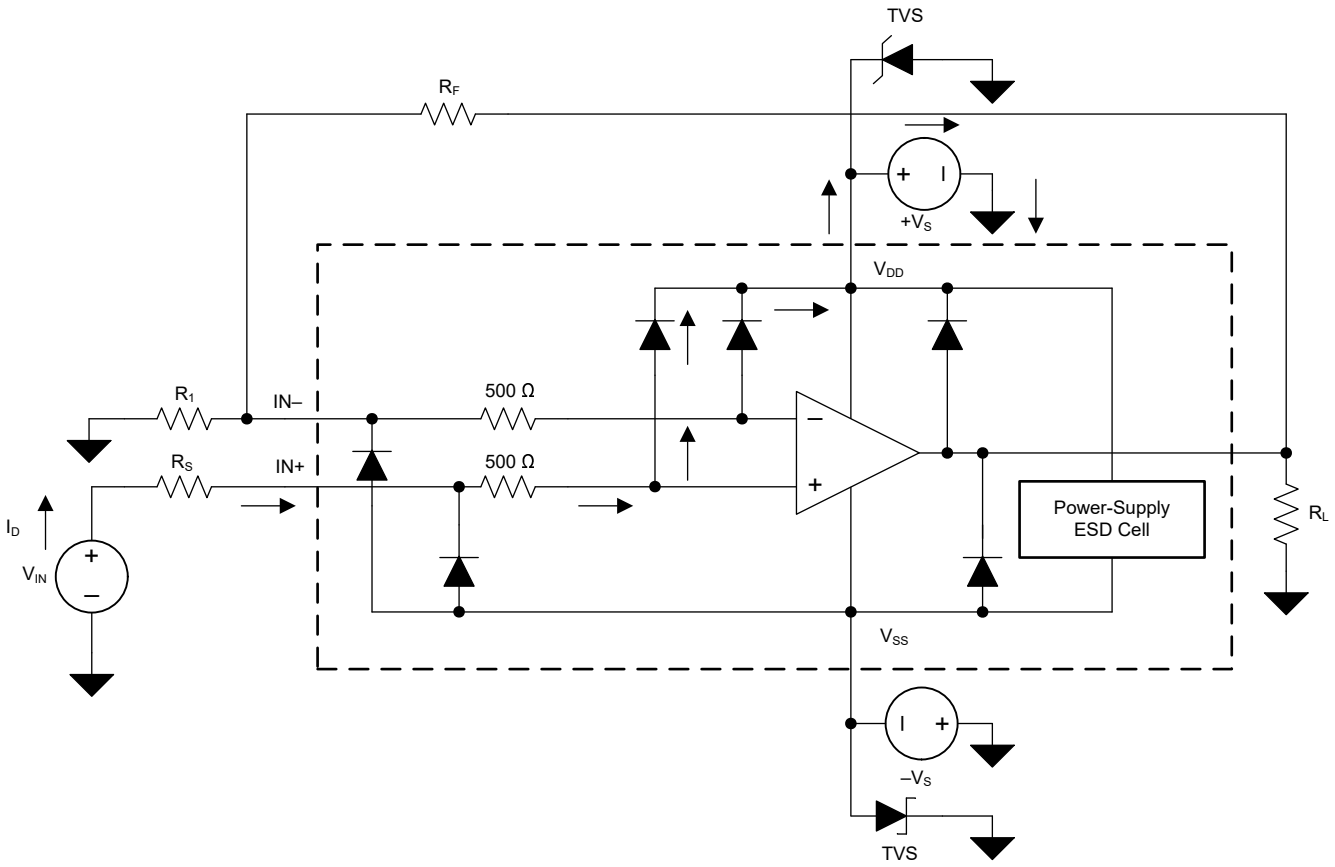


**図 7-10. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application**

An ESD event is very short in duration and very high voltage (for example; 1 kV, 100 ns), whereas an EOS event is long duration and lower voltage (for example; 50 V, 100 ms). The ESD diodes are designed for out-of-circuit ESD protection (that is, during assembly, test, and storage of the device before being soldered to the PCB). During an ESD event, the ESD signal is passed through the ESD steering diodes to an absorption circuit (labeled ESD power-supply circuit). The ESD absorption circuit clamps the supplies to a safe level.

Although this behavior is necessary for out-of-circuit protection, excessive current and damage is caused if activated in-circuit. A transient voltage suppressors (TVS) can be used to prevent against damage caused by turning on the ESD absorption circuit during an in-circuit ESD event. Using the appropriate current limiting resistors and TVS diodes allows for the use of device ESD diodes to protect against EOS events.


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### 7.3.8 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the OPAx991 is approximately 500 ns.

### 7.3.9 Typical Specifications and Distributions

Designers often have questions about a typical specification of an amplifier in order to design a more robust circuit. Due to natural variation in process technology and manufacturing procedures, every specification of an amplifier will exhibit some amount of deviation from the ideal value, like an amplifier's input offset voltage. These deviations often follow *Gaussian* ("bell curve"), or *normal* distributions, and circuit designers can leverage this information to guardband their system, even when there is not a minimum or maximum specification in セクション 6.7.

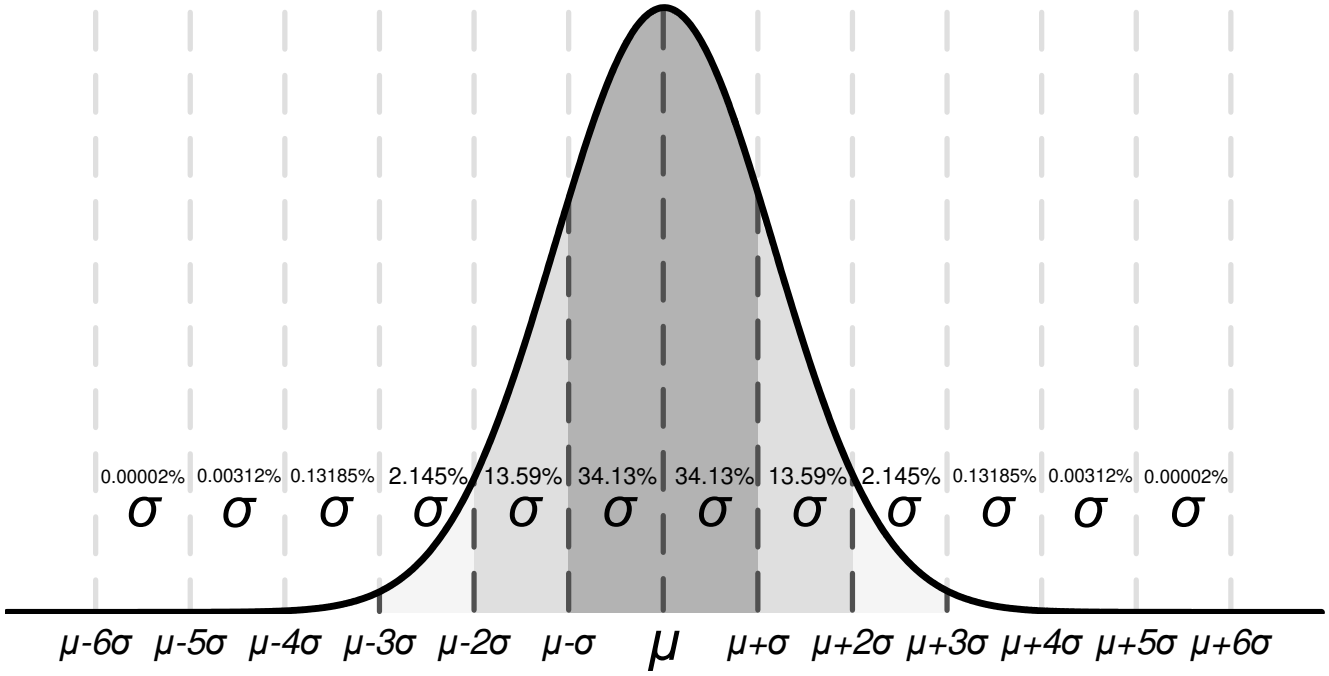


**図 7-11. Ideal Gaussian Distribution**

図 7-11 shows an example distribution, where *μ*, or *mu*, is the mean of the distribution, and where *σ*, or *sigma*, is the standard deviation of a system. For a specification that exhibits this kind of distribution, approximately two-thirds (68.26%) of all units can be expected to have a value within one standard deviation, or one sigma, of the mean (from *μ–σ* to *μ+σ*).

Depending on the specification, values listed in the *typical* column of セクション 6.7 are represented in different ways. As a general rule of thumb, if a specification naturally has a nonzero mean (for example, like gain bandwidth), then the typical value is equal to the mean (μ). However, if a specification naturally has a mean near zero (like input offset voltage), then the typical value is equal to the mean plus one standard deviation (μ + σ) in order to most accurately represent the typical value.

You can use this chart to calculate approximate probability of a specification in a unit; for example, for OPAx991, the typical input voltage offset is 125 μV, so 68.2% of all OPAx991 devices are expected to have an offset from –

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125 µV to 125 µV. At 4 σ (±500 µV), 99.9937% of the distribution has an offset voltage less than ±500 µV, which means 0.0063% of the population is outside of these limits, which corresponds to about 1 in 15,873 units.

Specifications with a value in the minimum or maximum column are assured by TI, and units outside these limits will be removed from production material. For example, the OPAx991 family has a maximum offset voltage of 675 µV at 25°C, and even though this corresponds to about 5 σ (≈1 in 1.7 million units), which is extremely unlikely, TI assures that any unit with larger offset than 675 µV will be removed from production material.

For specifications with no value in the minimum or maximum column, consider selecting a sigma value of sufficient guardband for your application, and design worst-case conditions using this value. For example, the 6-σ value corresponds to about 1 in 500 million units, which is an extremely unlikely chance, and could be an option as a wide guardband to design a system around. In this case, the OPAx991 family does not have a maximum or minimum for offset voltage drift, but based on 図 6-2 and the typical value of 0.3 µV/°C in セクション 6.7, it can be calculated that the 6-σ value for offset voltage drift is about 1.8 µV/°C. When designing for worst-case system conditions, this value can be used to estimate the worst possible offset across temperature without having an actual minimum or maximum value.

However, process variation and adjustments over time can shift typical means and standard deviations, and unless there is a value in the minimum or maximum specification column, TI cannot assure the performance of a device. This information should be used only to estimate the performance of a device.

### 7.3.10 Packages With an Exposed Thermal Pad

The OPAx991 family is available in the WSON-8 (DSG) package which features an exposed thermal pad. Inside the package, the die is attached to this thermal pad using an electrically conductive compound. For this reason, when using a package with an exposed thermal pad, the thermal pad must either be connected to V– or left floating. Attaching the thermal pad to a potential other than V– is not allowed, and performance of the device is not assured when doing so.

### 7.3.11 Shutdown

The OPAx991S devices feature one or more shutdown pins (SHDN) that disable the op amp, placing it into a low-power standby mode. In this mode, the op amp typically consumes about 30 µA. The SHDN pins are active high, meaning that shutdown mode is enabled when the input to the SHDN pin is a valid logic high. The amplifier is enabled when the input to the SHDN pin is a valid logic low.

The SHDN pins are referenced to the negative supply rail of the op amp. The threshold of the shutdown feature lies around 800 mV (typical) and does not change with respect to the supply voltage. Hysteresis has been included in the switching threshold to ensure smooth switching characteristics. To ensure optimal shutdown behavior, the SHDN pins should be driven with valid logic signals. A valid logic low is defined as a voltage between V– and V– + 0.2 V. A valid logic high is defined as a voltage between V– + 1.1 V and V– + 20 V or V+, whichever is lower. The shutdown pin circuitry includes a pull-down resistor, which will inherently pull the voltage of the pin to the negative supply rail if not driven. Thus, to enable the amplifier, the SHDN pins should either be left floating or driven to a valid logic low. To disable the amplifier, the SHDN pins must be driven to a valid logic high. The maximum voltage allowed at the SHDN pins is V– + 20 V or V+, whichever is lower. Exceeding V– + 20 V or V+, whichever is lower, will damage the device.

The SHDN pins are high-impedance CMOS inputs. Channels of single and dual op amp packages are independently controlled, and channels of quad op amp packages are controlled in pairs. For battery-operated applications, this feature may be used to greatly reduce the average current and extend battery life. The typical enable time out of shutdown is 8 µs; disable time is 3 µs. When disabled, the output assumes a high-impedance state. This architecture allows the OPAx991S family to operate as a gated amplifier, multiplexer, or programmable-gain amplifier. Shutdown time ($t_{OFF}$) depends on loading conditions and increases as load resistance increases. To ensure shutdown (disable) within a specific shutdown time, the specified 10-kΩ load to midsupply ($V_S$ / 2) is required. If using the OPAx991S without a load, the resulting turnoff time significantly increases.


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## 7.4 Device Functional Modes

The OPAx991 has a single functional mode and is operational when the power-supply voltage is greater than 2.7 V (±1.35 V). The maximum power supply voltage for the OPAx991 is 40 V (±20 V).

The OPAx991S devices feature a shutdown pin, which can be used to place the op amp into a low-power mode. See セクション 7.3.11 for more information.

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# 8 Application and Implementation

**Note**

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## 8.1 Application Information

The OPAx991 family offers excellent DC precision and AC performance. These devices operate up to 40-V supply rails and offer true rail-to-rail input/output, low offset voltage and offset voltage drift, as well as 4.5-MHz bandwidth and high output drive. These features make the OPAx991 a robust, high-performance operational amplifier for high-voltage industrial applications.

## 8.2 Typical Applications

### 8.2.1 Low-Side Current Measurement

図 8-1 shows the OPA991 configured in a low-side current sensing application. For a full analysis of the circuit shown in 図 8-1 including theory, calculations, simulations, and measured data, see TI Precision Design TIPD129, *0-A to 1-A Single-Supply Low-Side Current-Sensing Solution*.

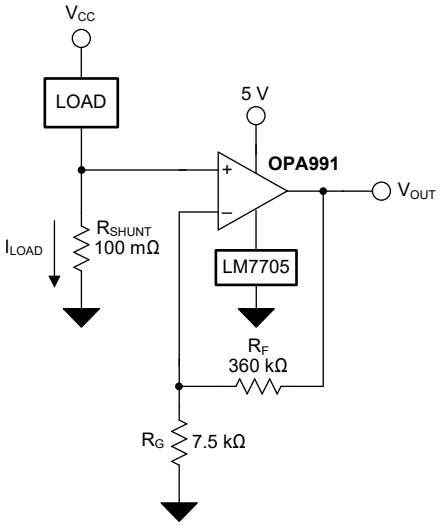


**図 8-1. OPA991 in a Low-Side, Current-Sensing Application**

#### *8.2.1.1 Design Requirements*

The design requirements for this design are:

- Load current: 0 A to 1 A
- Output voltage: 4.9 V
- Maximum shunt voltage: 100 mV


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#### 8.2.1.2 Detailed Design Procedure

The transfer function of the circuit in 図 8-1 is given in 式 1:

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times Gain \tag{1}$$

The load current ($I_{LOAD}$) produces a voltage drop across the shunt resistor ($R_{SHUNT}$). The load current is set from 0 A to 1 A. To keep the shunt voltage below 100 mV at maximum load current, the largest shunt resistor is defined using 式 2:

$$R_{SHUNT} = \frac{V_{SHUNT_MAX}}{I_{LOAD_MAX}} = \frac{100mV}{1A} = 100m\Omega \tag{2}$$

Using 式 2, $R_{SHUNT}$ is calculated to be 100 mΩ. The voltage drop produced by $I_{LOAD}$ and $R_{SHUNT}$ is amplified by the OPA991 to produce an output voltage of 0 V to 4.9 V. The gain needed by the OPA991 to produce the necessary output voltage is calculated using 式 3:

$$Gain = \frac{\left(V_{OUT_MAX} - V_{OUT_MIN}\right)}{\left(V_{IN_MAX} - V_{IN_MIN}\right)} \tag{3}$$

Using 式 3, the required gain is calculated to be 49 V/V, which is set with resistors $R_F$ and $R_G$. 式 4 is used to size the resistors, $R_F$ and $R_G$, to set the gain of the OPA991 to 49 V/V.

$$Gain = 1 + \frac{\left(R_F\right)}{\left(R_G\right)} \tag{4}$$

Choosing $R_F$ as 360 kΩ, $R_G$ is calculated to be 7.5 kΩ. $R_F$ and $R_G$ were chosen as 360 kΩ and 7.5 kΩ because they are standard value resistors that create a 49:1 ratio. Other resistors that create a 49:1 ratio can also be used. 図 8-2 shows the measured transfer function of the circuit shown in 図 8-1.

#### 8.2.1.3 Application Curves

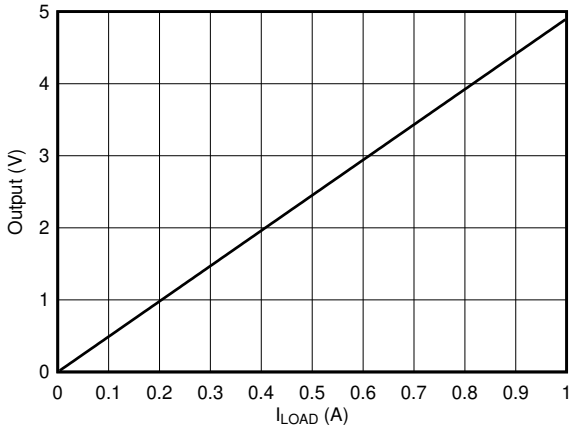


**図 8-2. Low-Side, Current-Sense, Transfer Function**

# 9 Power Supply Recommendations

The OPAx991 is specified for operation from 2.7 V to 40 V (±1.35 V to ±20 V); many specifications apply from –40°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in セクション 6.8.

**CAUTION**

Supply voltages larger than 40 V can permanently damage the device; see セクション 6.1.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to セクション 10.

# 10 Layout

## 10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in 図 10-2, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.


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## 10.2 Layout Example

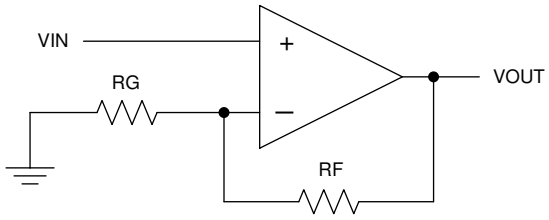


**図 10-1. Schematic Representation**

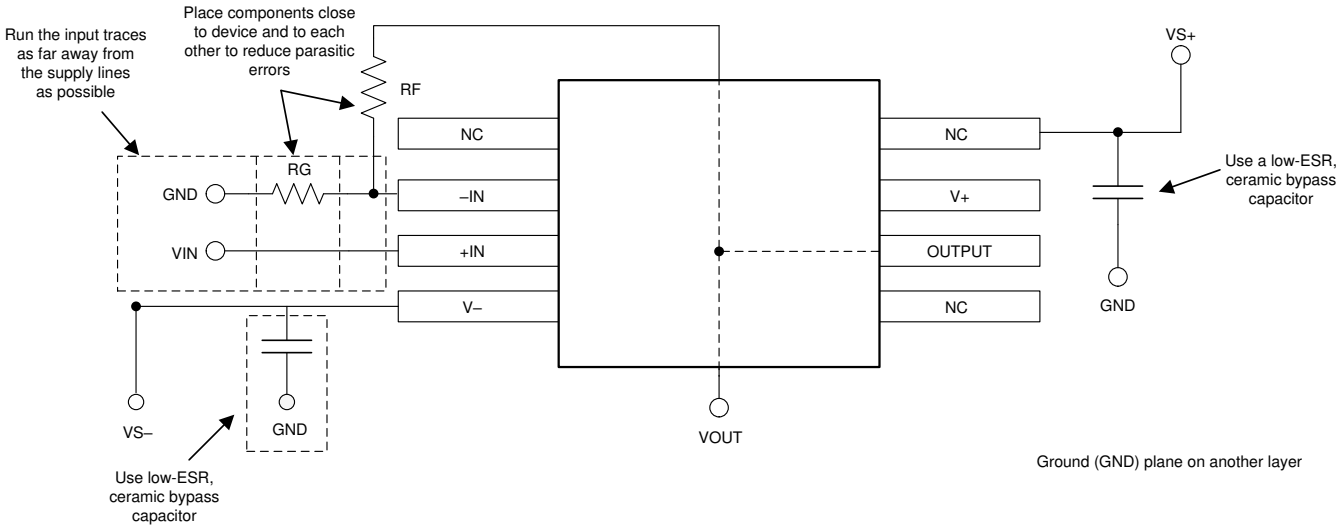


**図 10-2. Operational Amplifier Board Layout for Noninverting Configuration**

# 11 Device and Documentation Support

## 11.1 Device Support

### 11.1.1 Development Support

#### *11.1.1.1 TINA-TI™ (Free Software Download)*

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

**Note**

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

#### *11.1.1.2 TI Precision Designs*

The OPAx991 is featured in several TI Precision Designs, available online at http://www.ti.com/ww/en/analog/precision-designs/. TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits.

## 11.2 Documentation Support

### 11.2.1 Related Documentation

For related documentation, see the following:

Texas Instruments, *Analog Engineer's Circuit Cookbook: Amplifiers* solution guide

Texas Instruments, *AN31 Amplifier Circuit Collection* application note

Texas Instruments, *MUX-Friendly Precision Operational Amplifiers* application brief

Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers* application report

Texas Instruments, *Op Amps With Complementary-Pair Input Stages* application note

## 11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.4 サポート・リソース

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## 11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.7 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| OPA2991IDDFR | ACTIVE | SOT-23-THIN | DDF | 8 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | O91F | Samples |
| OPA2991IDGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | 26UT | Samples |
| OPA2991IDR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | OP2991 | Samples |
| OPA2991IDSGR | ACTIVE | WSON | DSG | 8 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | O91G | Samples |
| OPA2991IPWR | ACTIVE | TSSOP | PW | 8 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | O2991P | Samples |
| OPA2991SIRUGR | ACTIVE | X2QFN | RUG | 10 | 3000 | RoHS & Green | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | GFF | Samples |
| OPA4991IDR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | OPA4991D | Samples |
| OPA4991IDYYR | ACTIVE | SOT-23-THIN | DYY | 14 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | OPA4991I | Samples |
| OPA4991IPWR | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU \| SN | Level-2-260C-1 YEAR | -40 to 125 | (OP4991, OP4991PW) | Samples |
| OPA4991IRUCR | ACTIVE | QFN | RUC | 14 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | I4F | Samples |
| OPA991IDBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | O91V | Samples |
| OPA991IDCKR | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | SN | Level-2-260C-1 YEAR | -40 to 125 | 1HB | Samples |
| OPA991SIDBVR | ACTIVE | SOT-23 | DBV | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | O91S | Samples |
| OPA991TIDCKR | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | SN | Level-2-260C-1 YEAR | -40 to 125 | 1JE | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF OPA2991, OPA4991, OPA991 :**

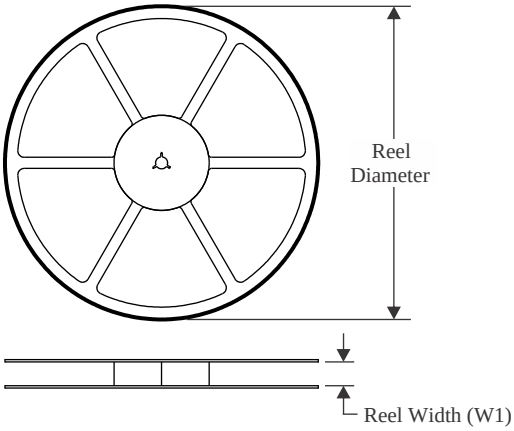
- Automotive : OPA2991-Q1, OPA4991-Q1, OPA991-Q1
- Enhanced Product : OPA4991-EP

NOTE: Qualified Version Definitions:

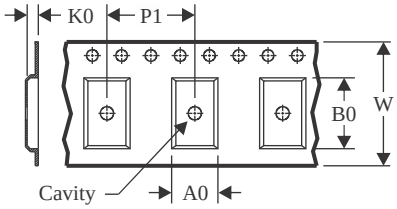
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

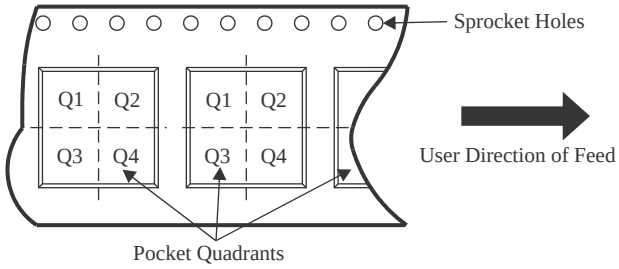



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

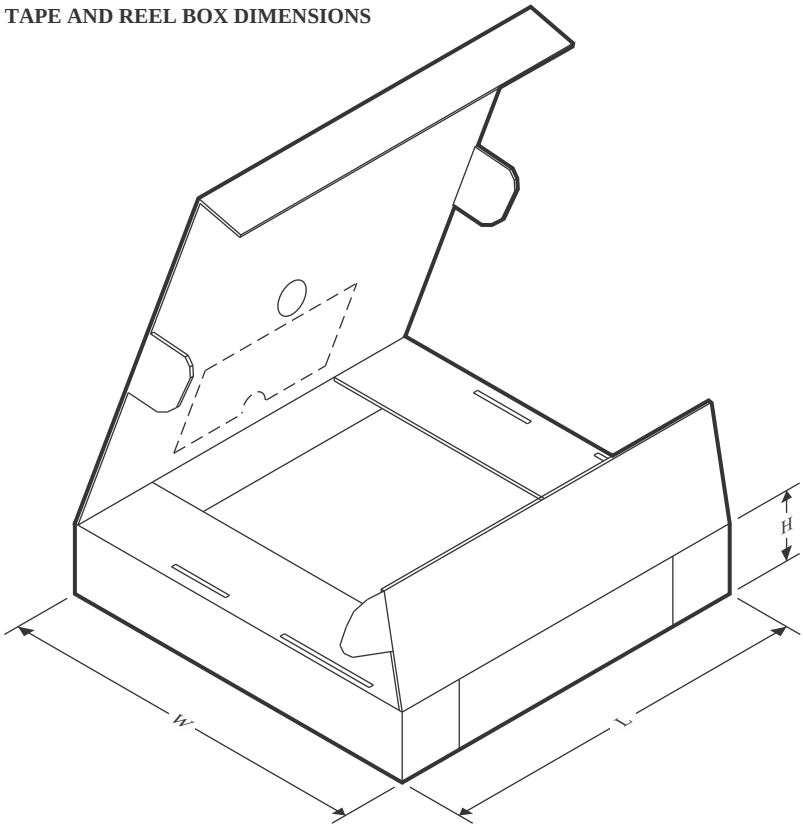
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OPA2991IDDFR | SOT-23-THIN | DDF | 8 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| OPA2991IDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| OPA2991IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| OPA2991IDSGR | WSON | DSG | 8 | 3000 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |
| OPA2991IPWR | TSSOP | PW | 8 | 2000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |
| OPA2991SIRUGR | X2QFN | RUG | 10 | 3000 | 178.0 | 8.4 | 1.75 | 2.25 | 0.56 | 4.0 | 8.0 | Q1 |
| OPA4991IDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| OPA4991IDYYR | SOT-23-THIN | DYY | 14 | 3000 | 330.0 | 12.4 | 4.8 | 3.6 | 1.6 | 8.0 | 12.0 | Q3 |
| OPA4991IPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| OPA4991IRUCR | QFN | RUC | 14 | 3000 | 180.0 | 9.5 | 2.16 | 2.16 | 0.5 | 4.0 | 8.0 | Q2 |
| OPA991IDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| OPA991IDCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| OPA991SIDBVR | SOT-23 | DBV | 6 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| OPA991TIDCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

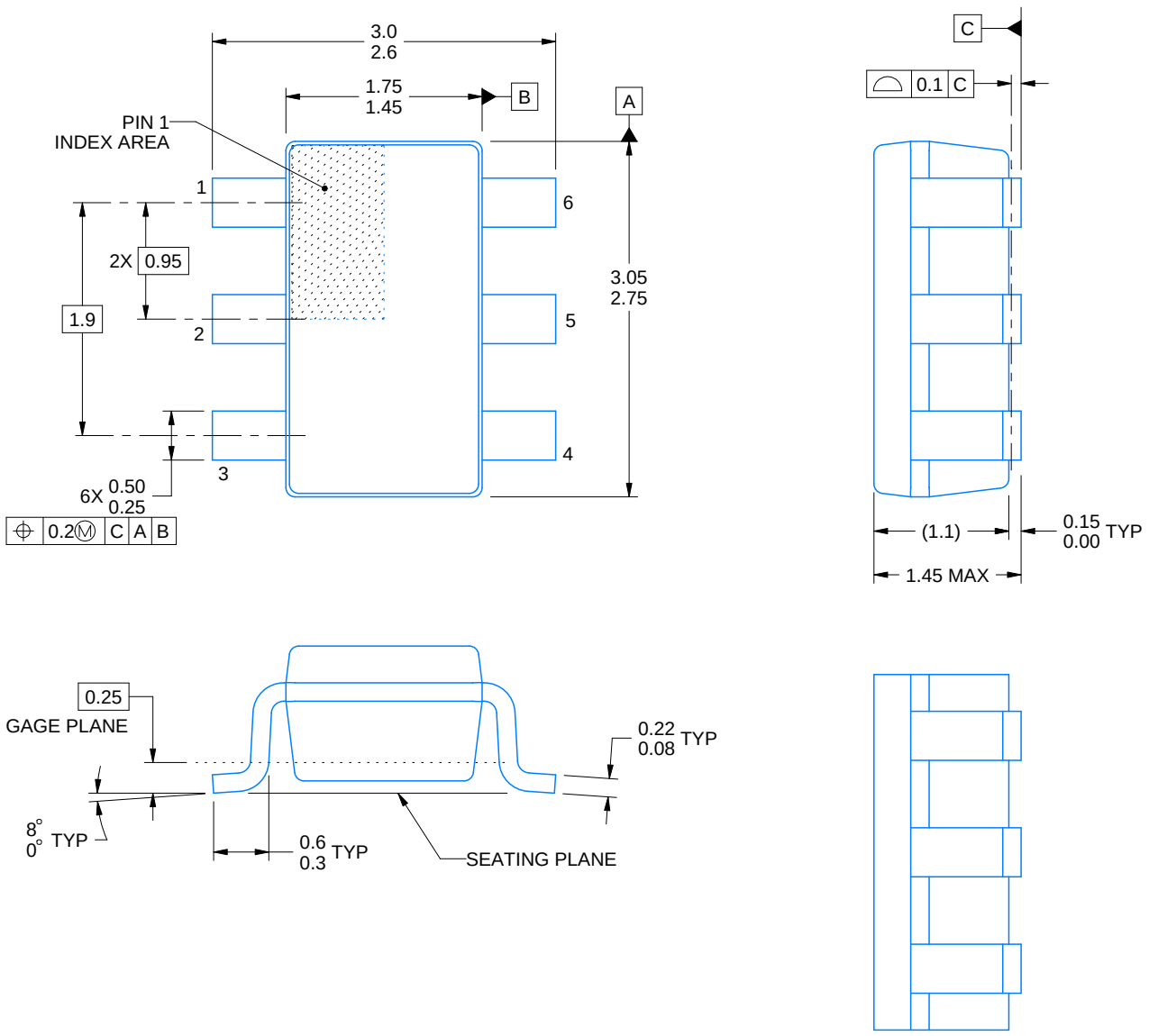
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| OPA2991IDDFR | SOT-23-THIN | DDF | 8 | 3000 | 210.0 | 185.0 | 35.0 |
| OPA2991IDGKR | VSSOP | DGK | 8 | 2500 | 366.0 | 364.0 | 50.0 |
| OPA2991IDR | SOIC | D | 8 | 2500 | 356.0 | 356.0 | 35.0 |
| OPA2991IDSGR | WSON | DSG | 8 | 3000 | 210.0 | 185.0 | 35.0 |
| OPA2991IPWR | TSSOP | PW | 8 | 2000 | 356.0 | 356.0 | 35.0 |
| OPA2991SIRUGR | X2QFN | RUG | 10 | 3000 | 205.0 | 200.0 | 33.0 |
| OPA4991IDR | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| OPA4991IDYYR | SOT-23-THIN | DYY | 14 | 3000 | 336.6 | 336.6 | 31.8 |
| OPA4991IPWR | TSSOP | PW | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| OPA4991IRUCR | QFN | RUC | 14 | 3000 | 205.0 | 200.0 | 30.0 |
| OPA991IDBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| OPA991IDCKR | SC70 | DCK | 5 | 3000 | 190.0 | 190.0 | 30.0 |
| OPA991SIDBVR | SOT-23 | DBV | 6 | 3000 | 210.0 | 185.0 | 35.0 |
| OPA991TIDCKR | SC70 | DCK | 5 | 3000 | 190.0 | 190.0 | 30.0 |

# PACKAGE OUTLINE

## DBV0006A

## SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

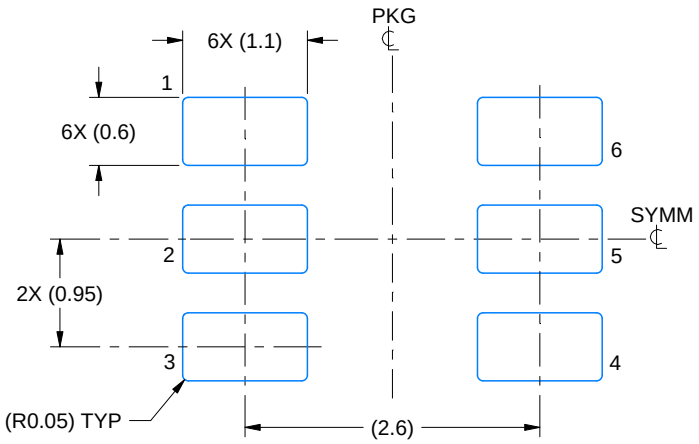



ALTERNATIVE PACKAGE SINGULATION VIEW

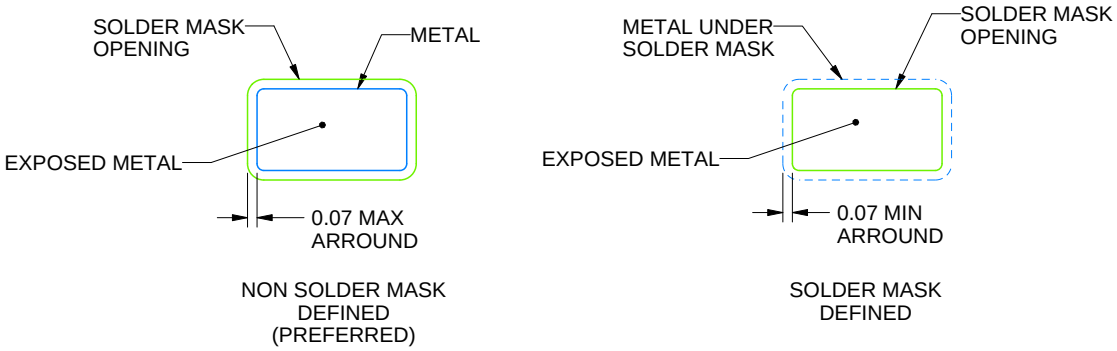
4214840/E 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

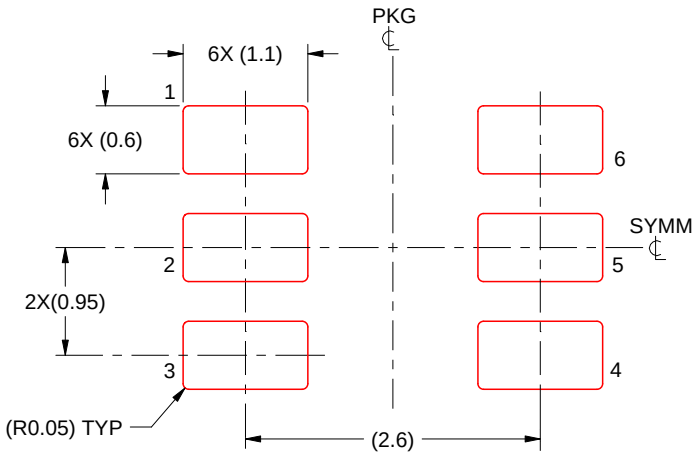



SOLDER MASK DETAILS

4214840/E 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/E 02/2024

NOTES: (continued)

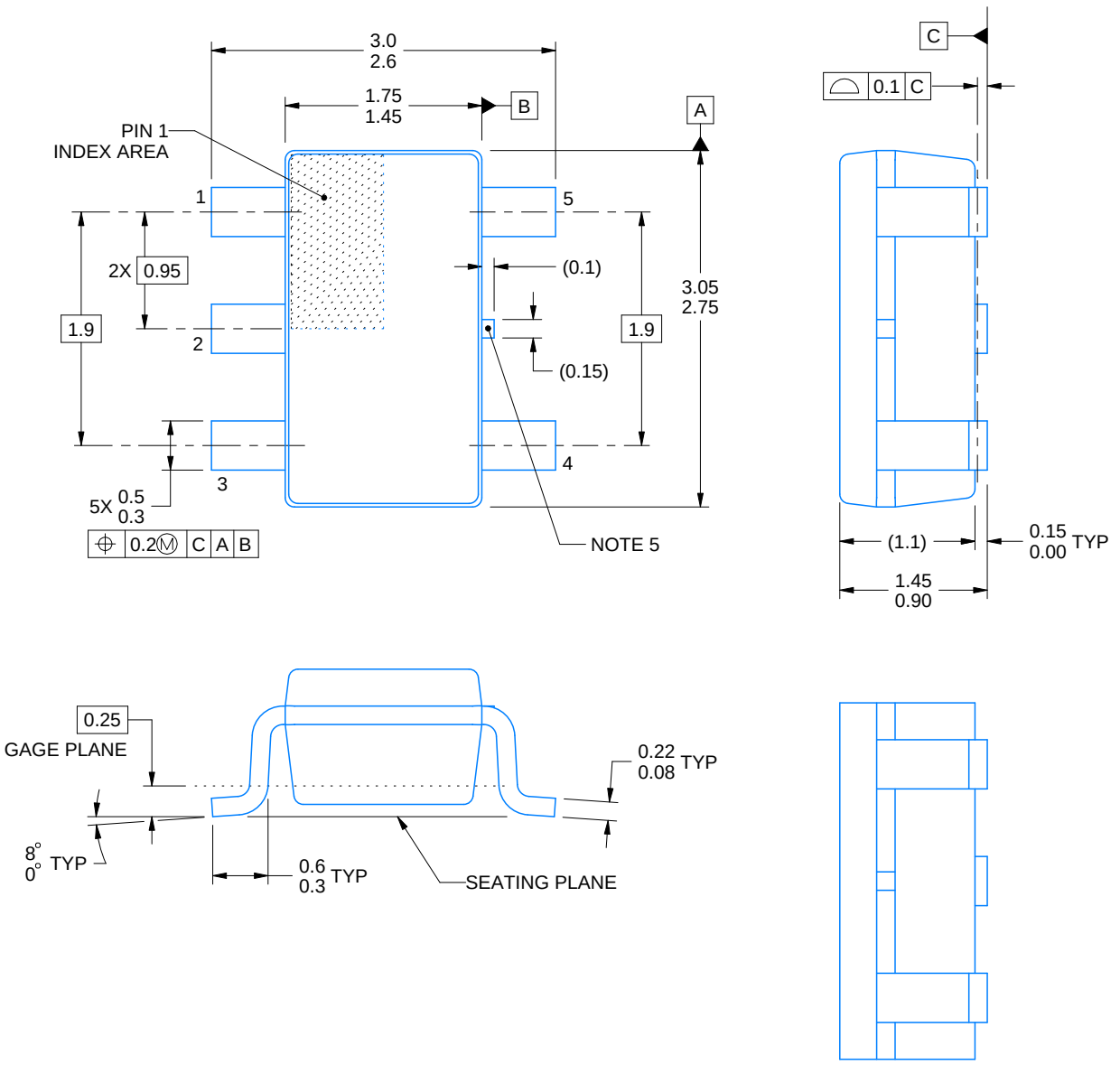
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DBV0005A

## SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

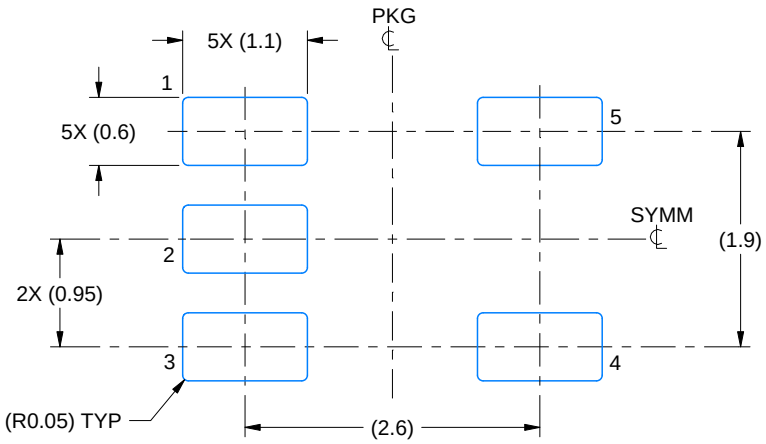



ALTERNATIVE PACKAGE SINGULATION VIEW

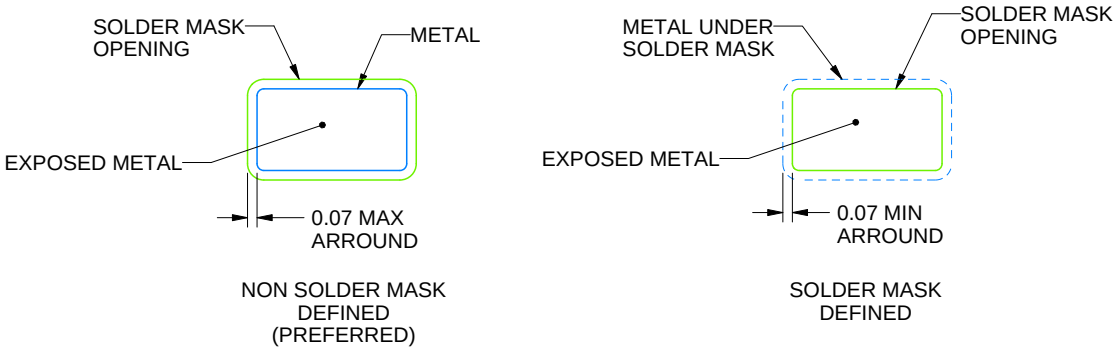
4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

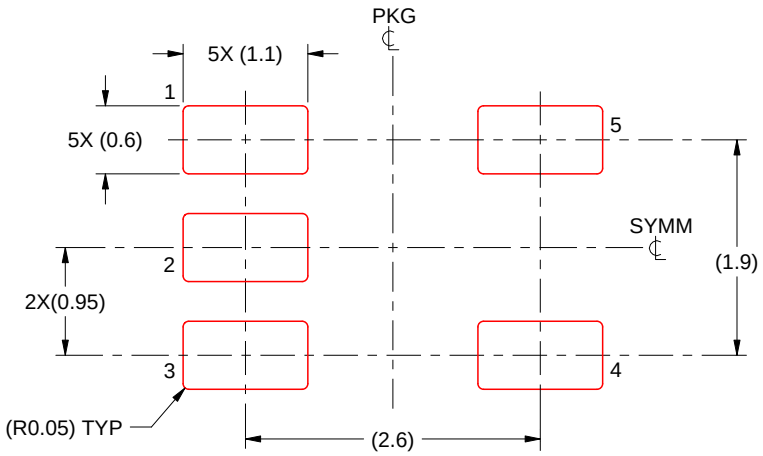



SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

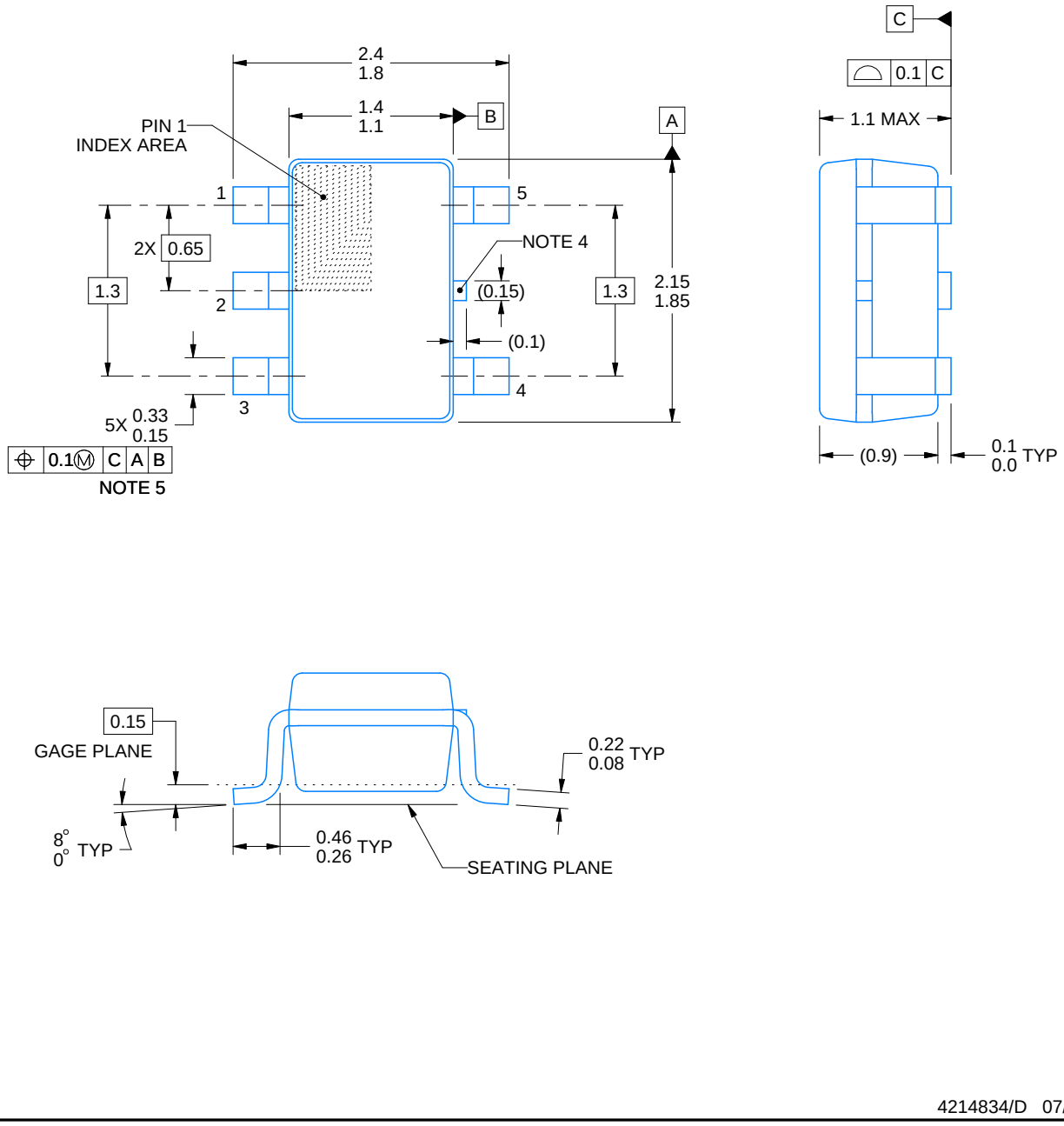
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DCK0005A

## SOT - 1.1 max height

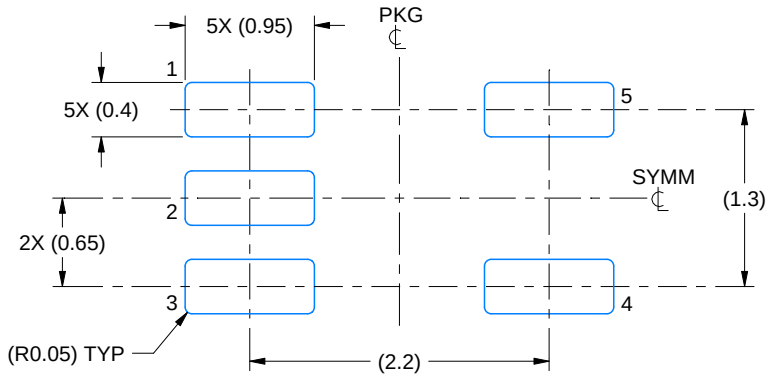
SMALL OUTLINE TRANSISTOR



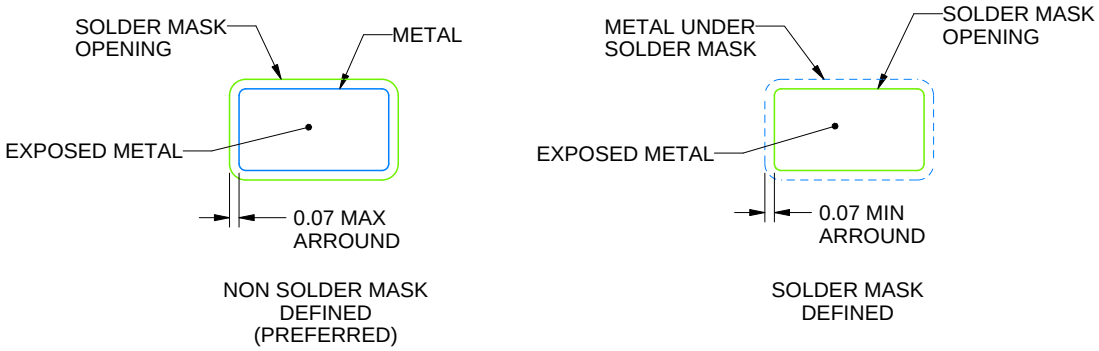

4214834/D 07/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

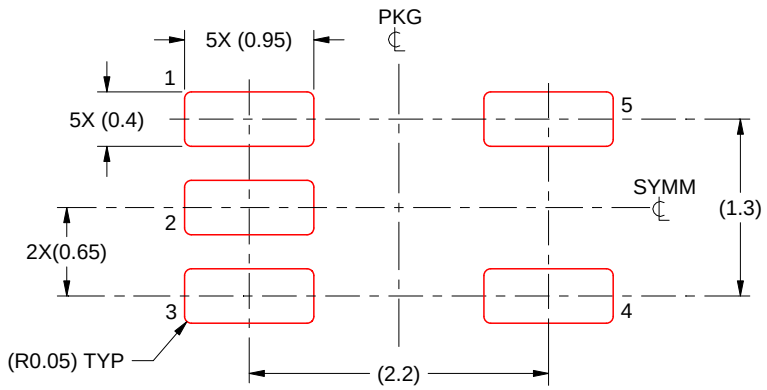



SOLDER MASK DETAILS

4214834/D 07/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



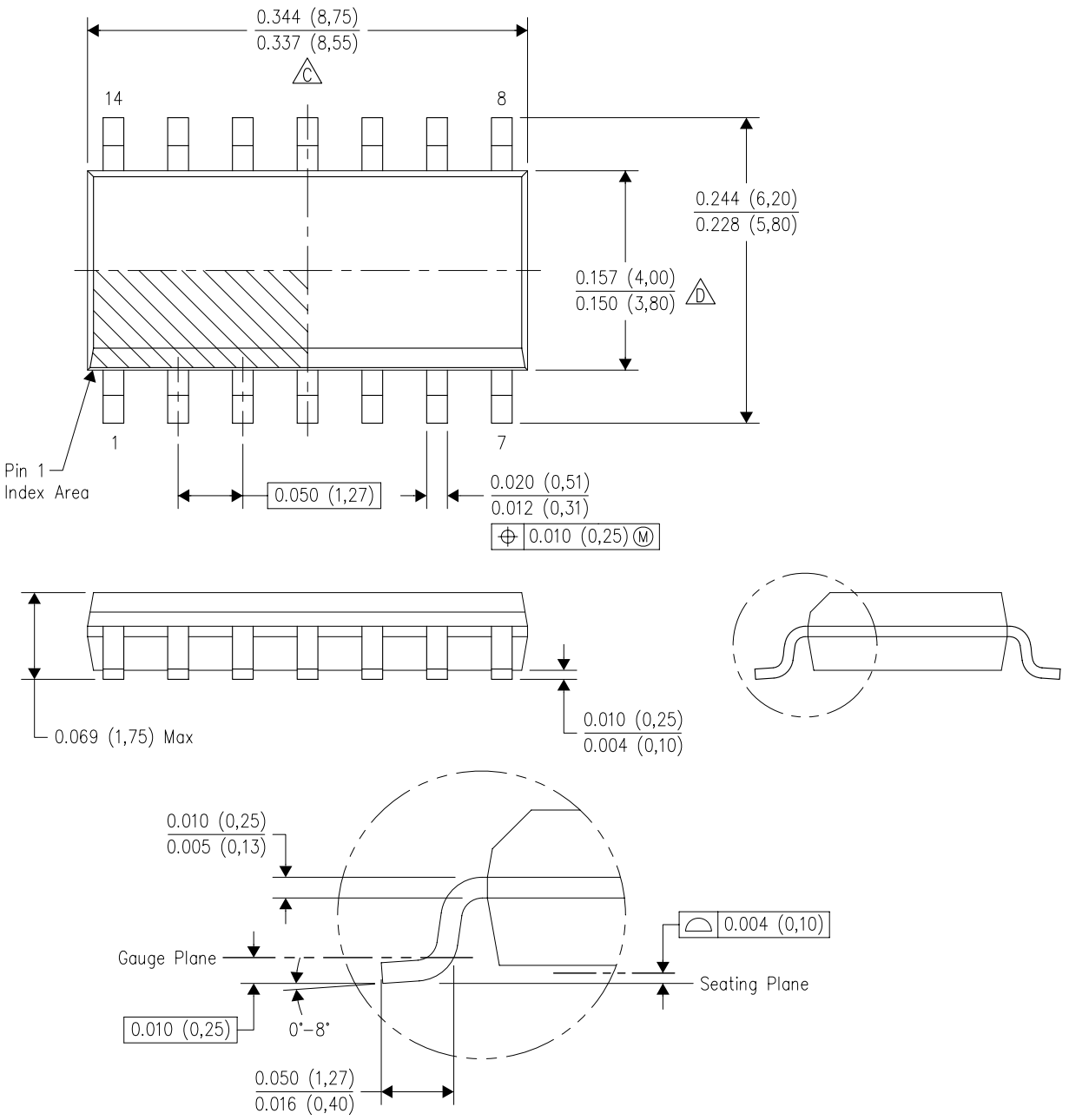

SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/D 07/2023

NOTES: (continued)

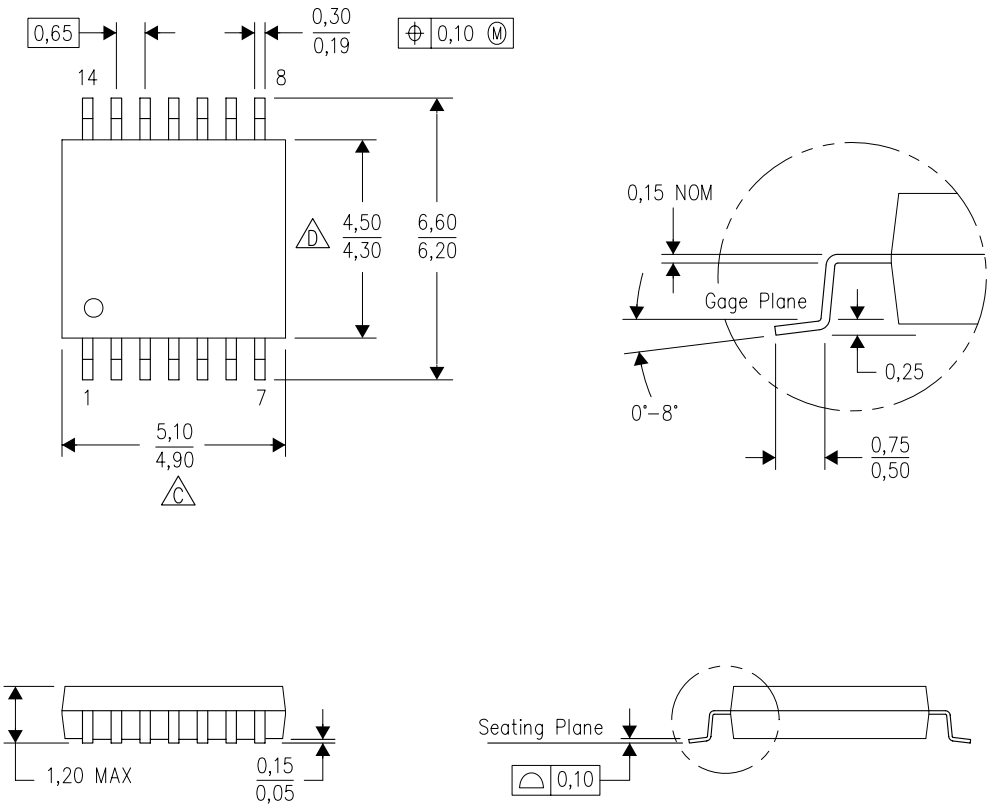
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

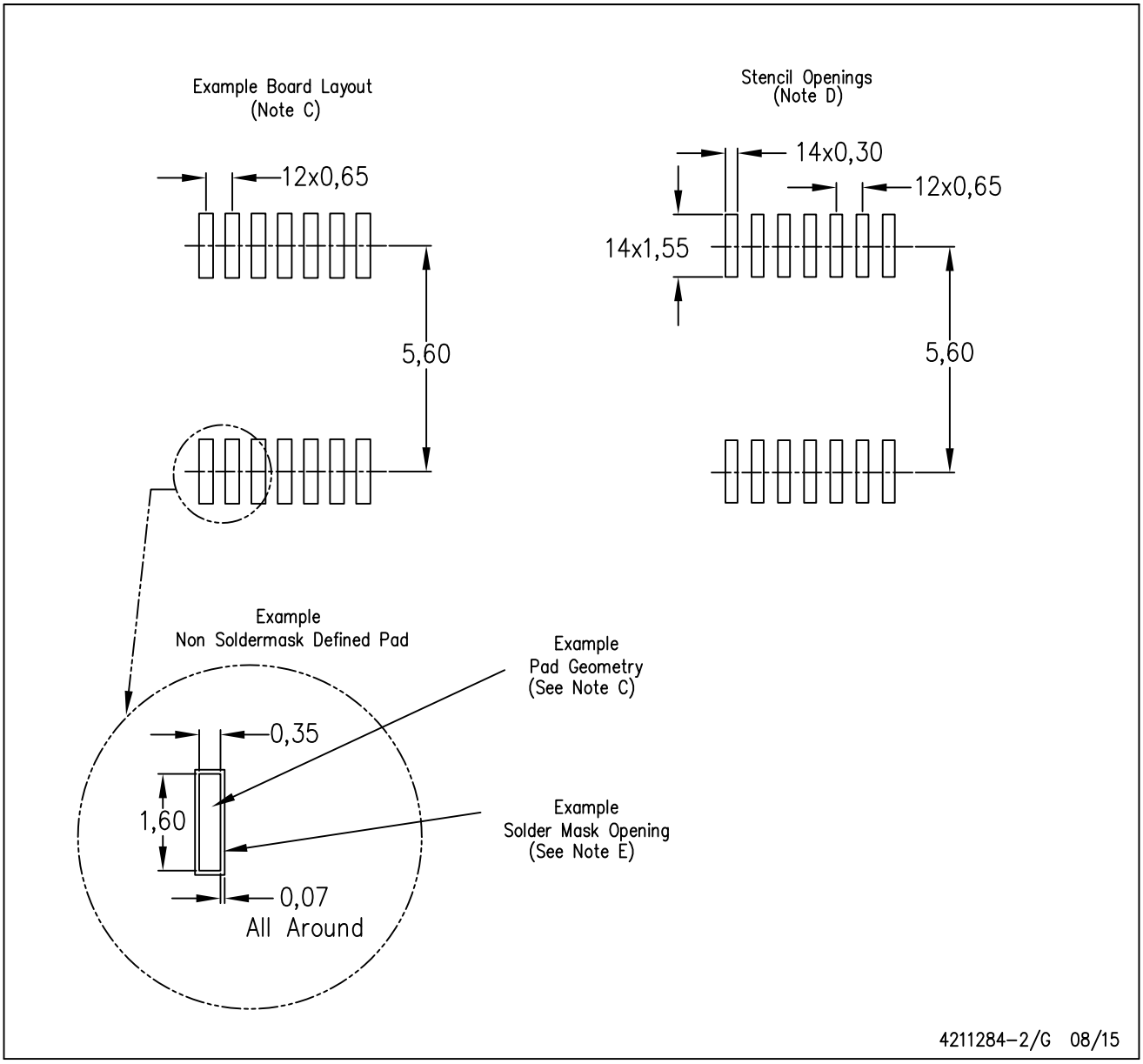
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE




4040064–3/G 02/11

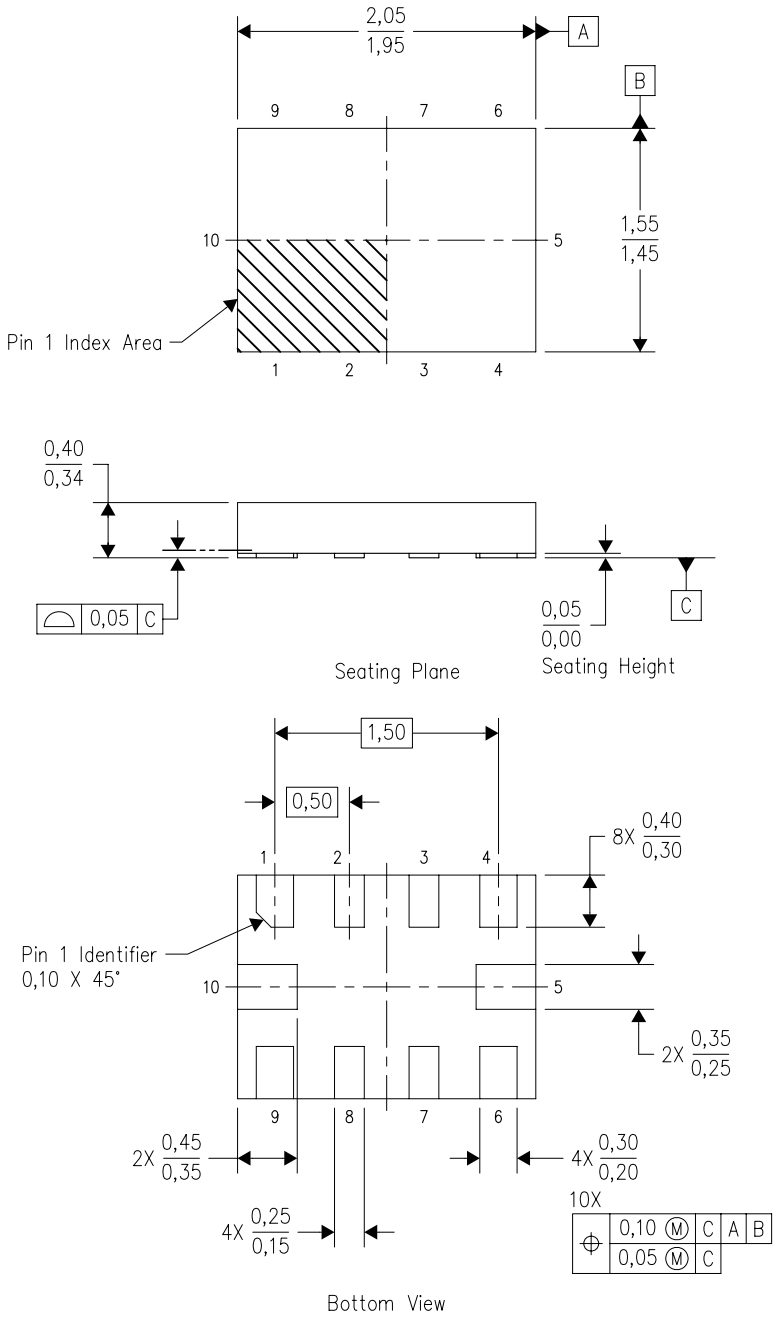
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

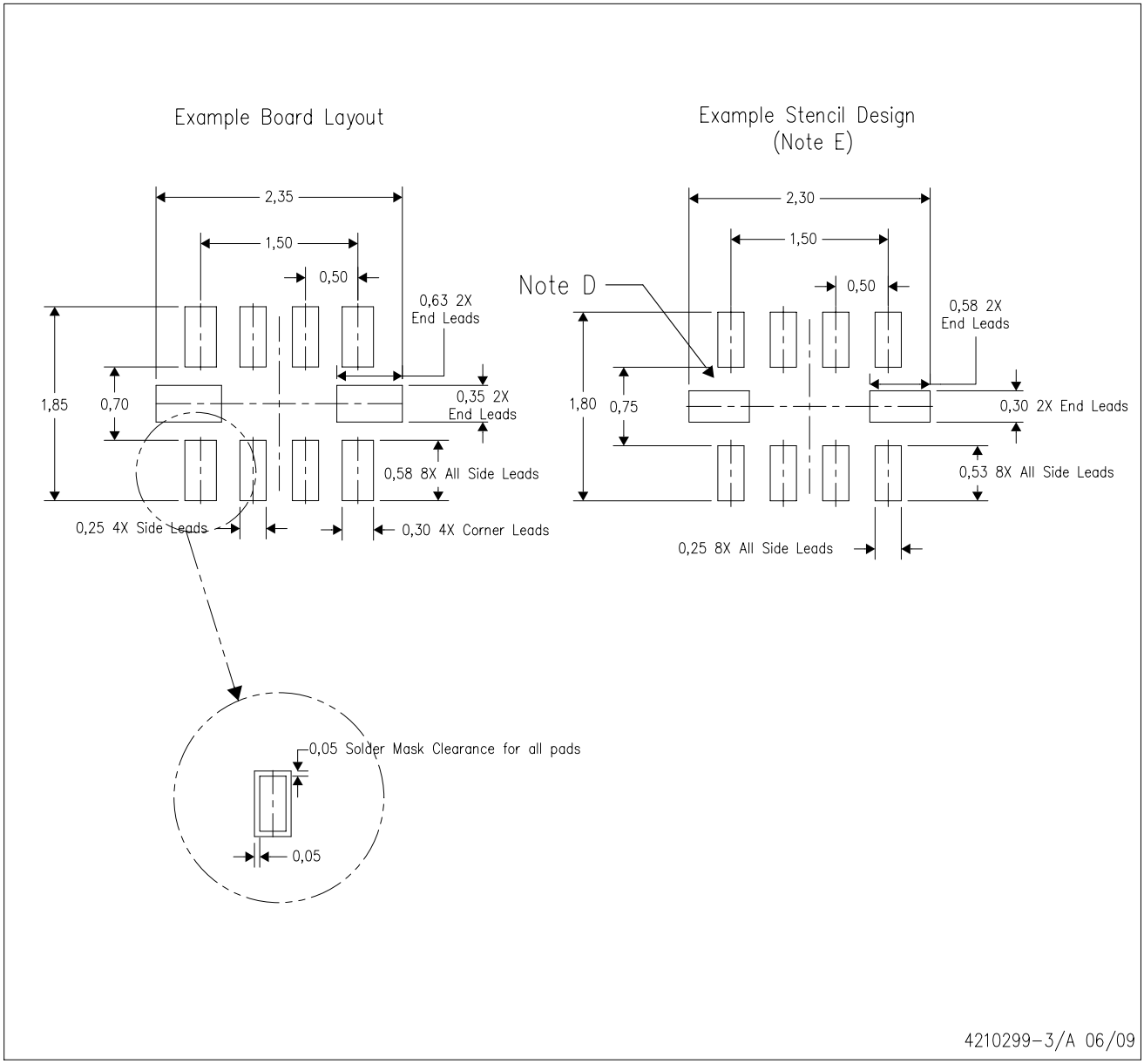
RUG (R–PQFP–N10) PLASTIC QUAD FLATPACK



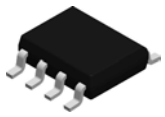

4208528–3/B 04/2008

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. This package complies to JEDEC MO–288 variation X2EFD.

RUG (R–PQFP–N10)




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

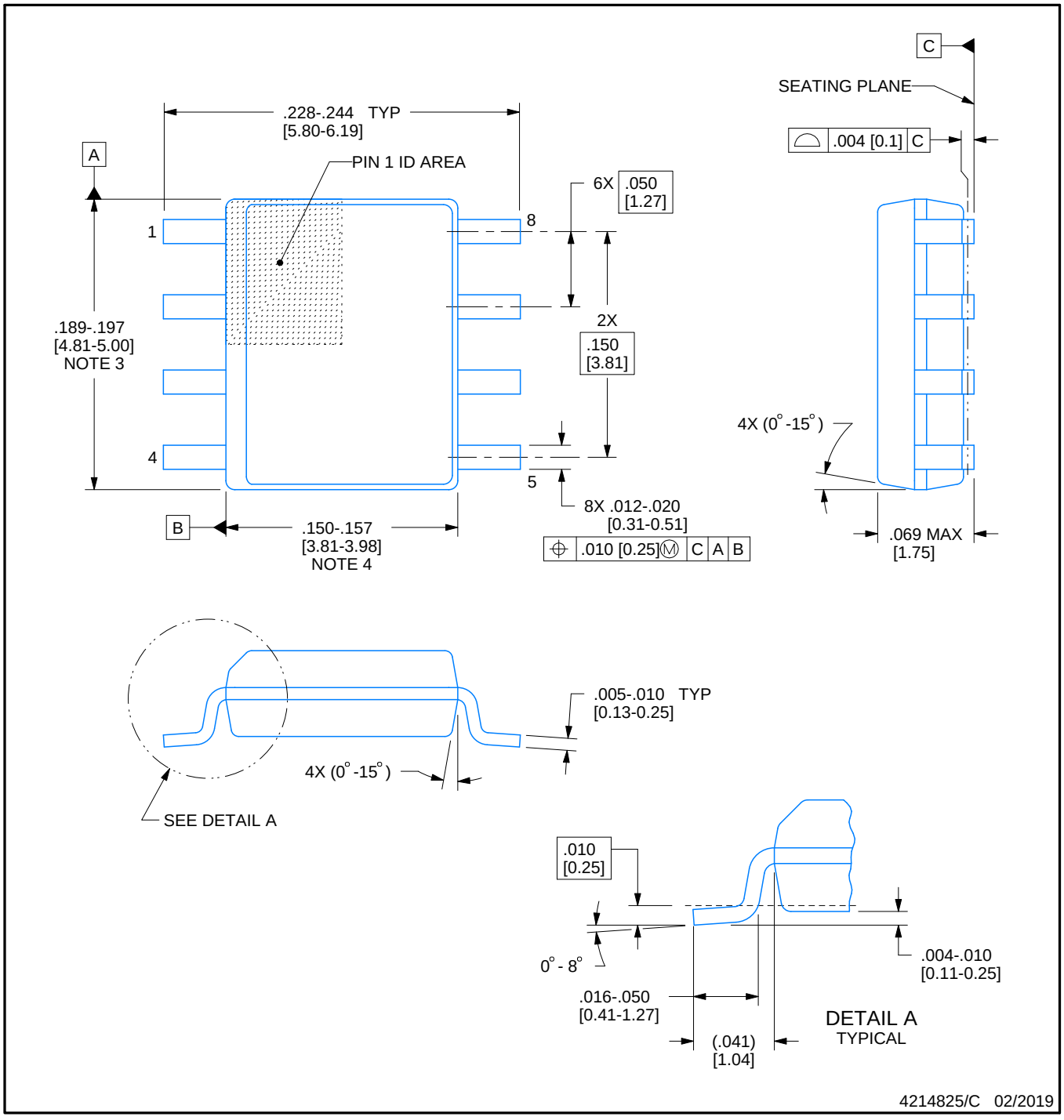


# PACKAGE OUTLINE

## D0008A

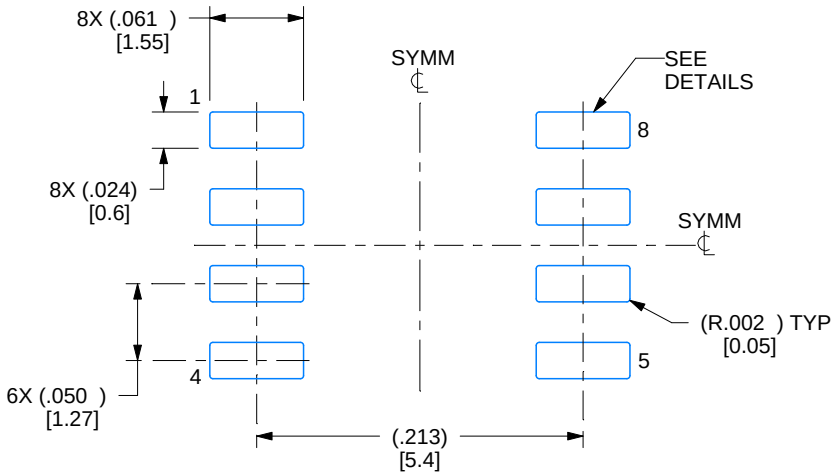
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

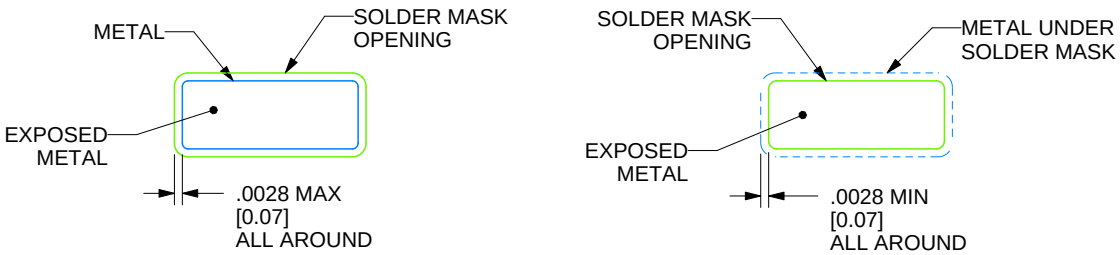



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

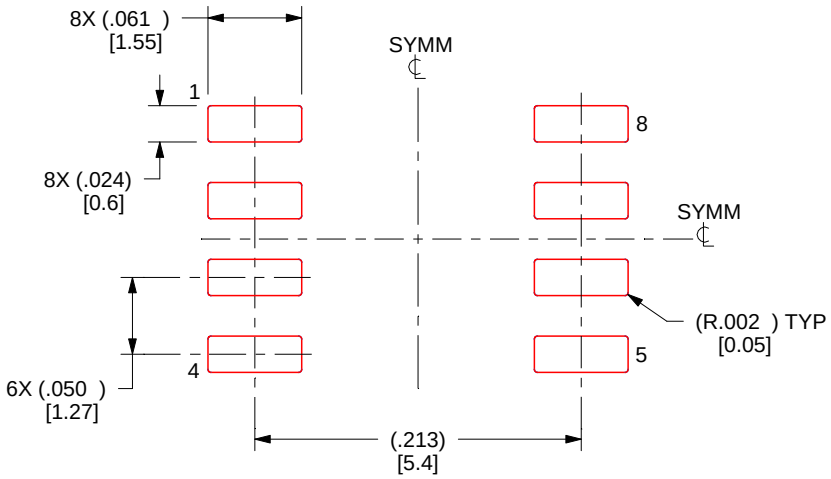
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

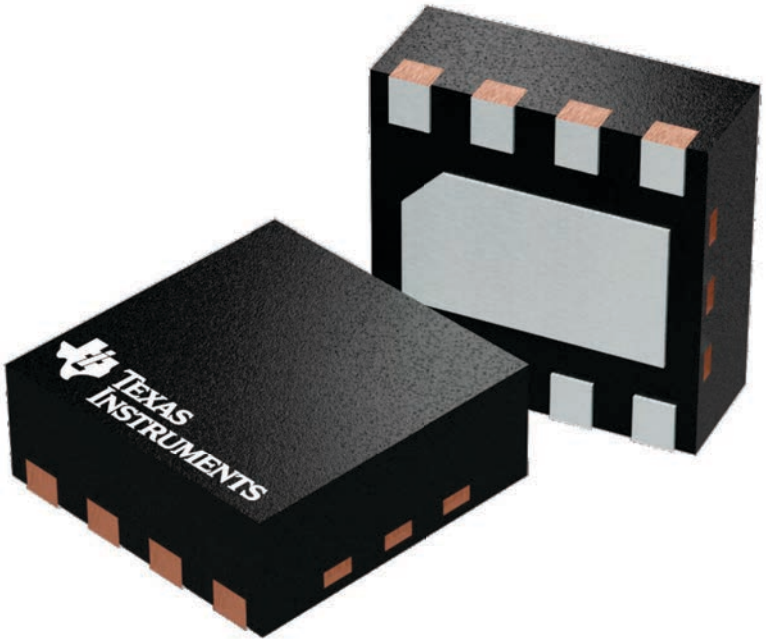
## DSG 8

## WSON - 0.8 mm max height

**2 x 2, 0.5 mm pitch**

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



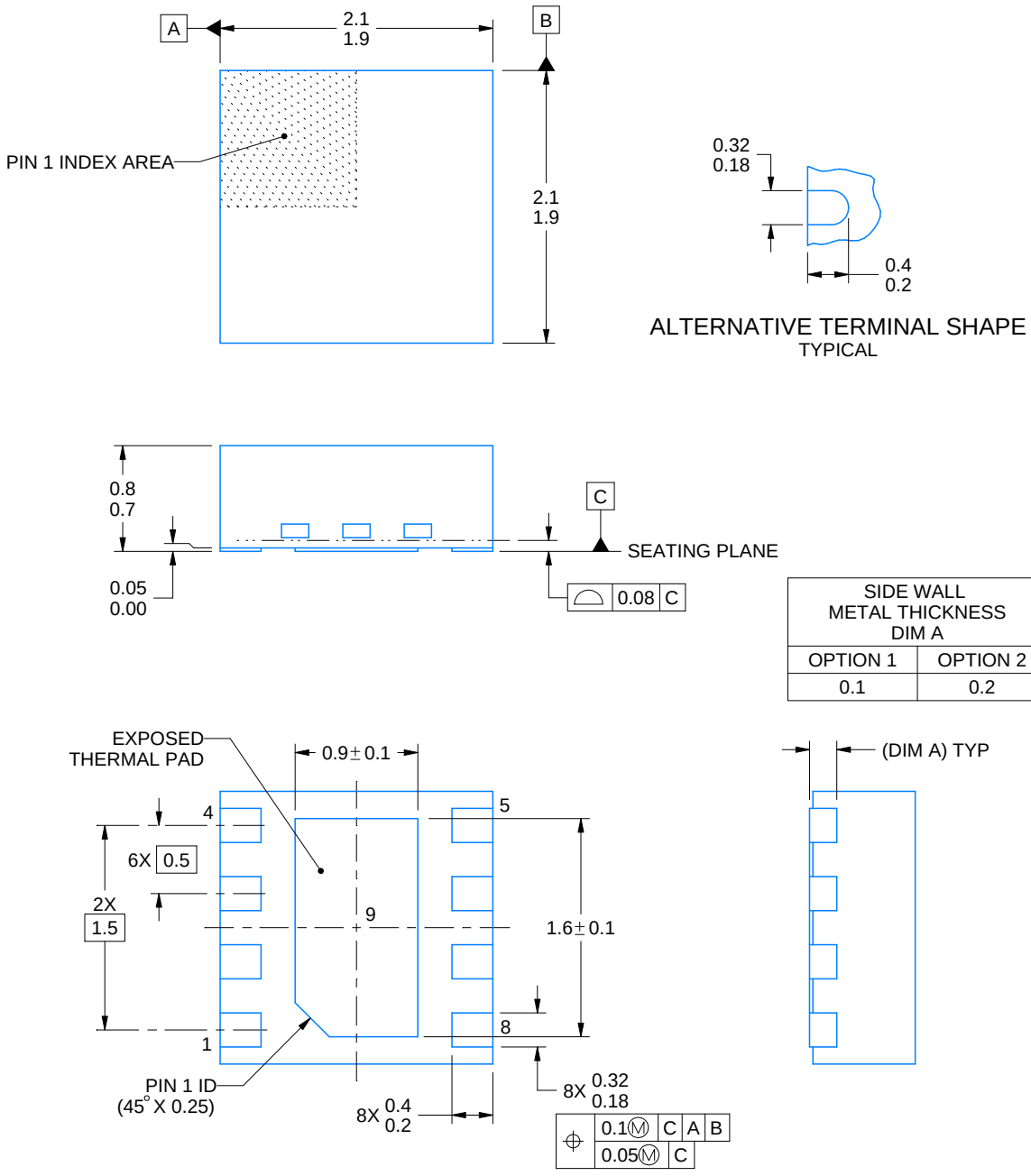

4224783/A

# DSG0008A

# PACKAGE OUTLINE

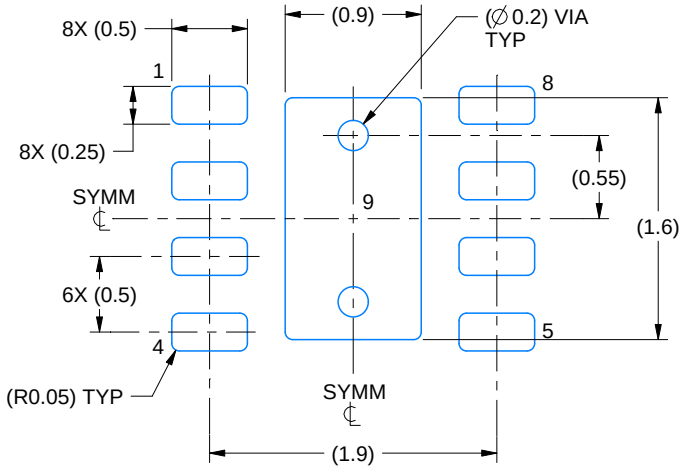
## WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

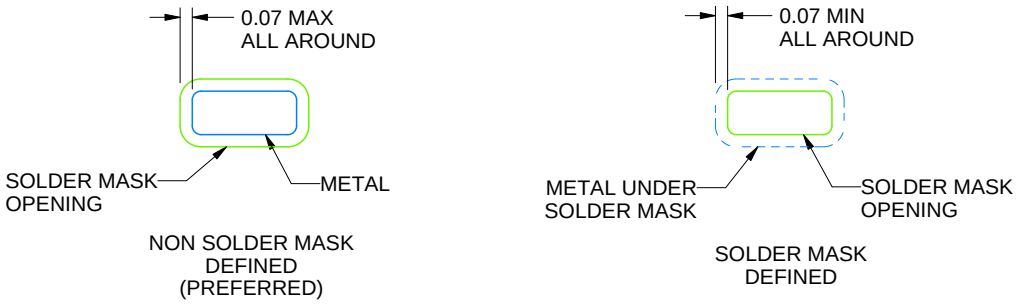



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
SCALE:20X

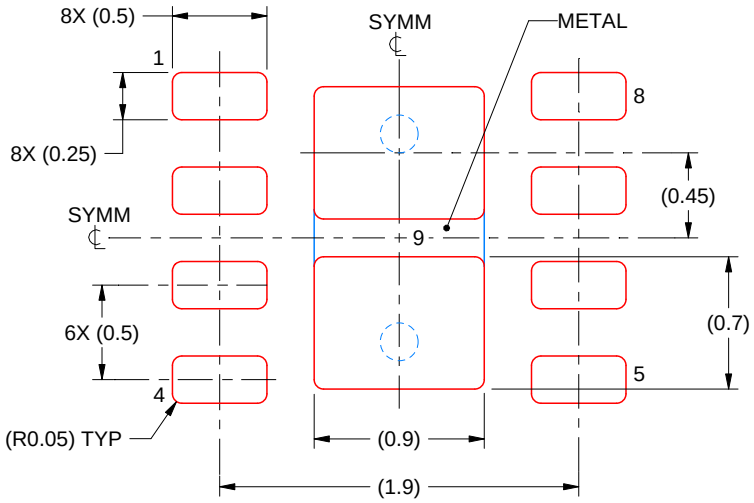



SOLDER MASK DETAILS

4218900/E 08/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

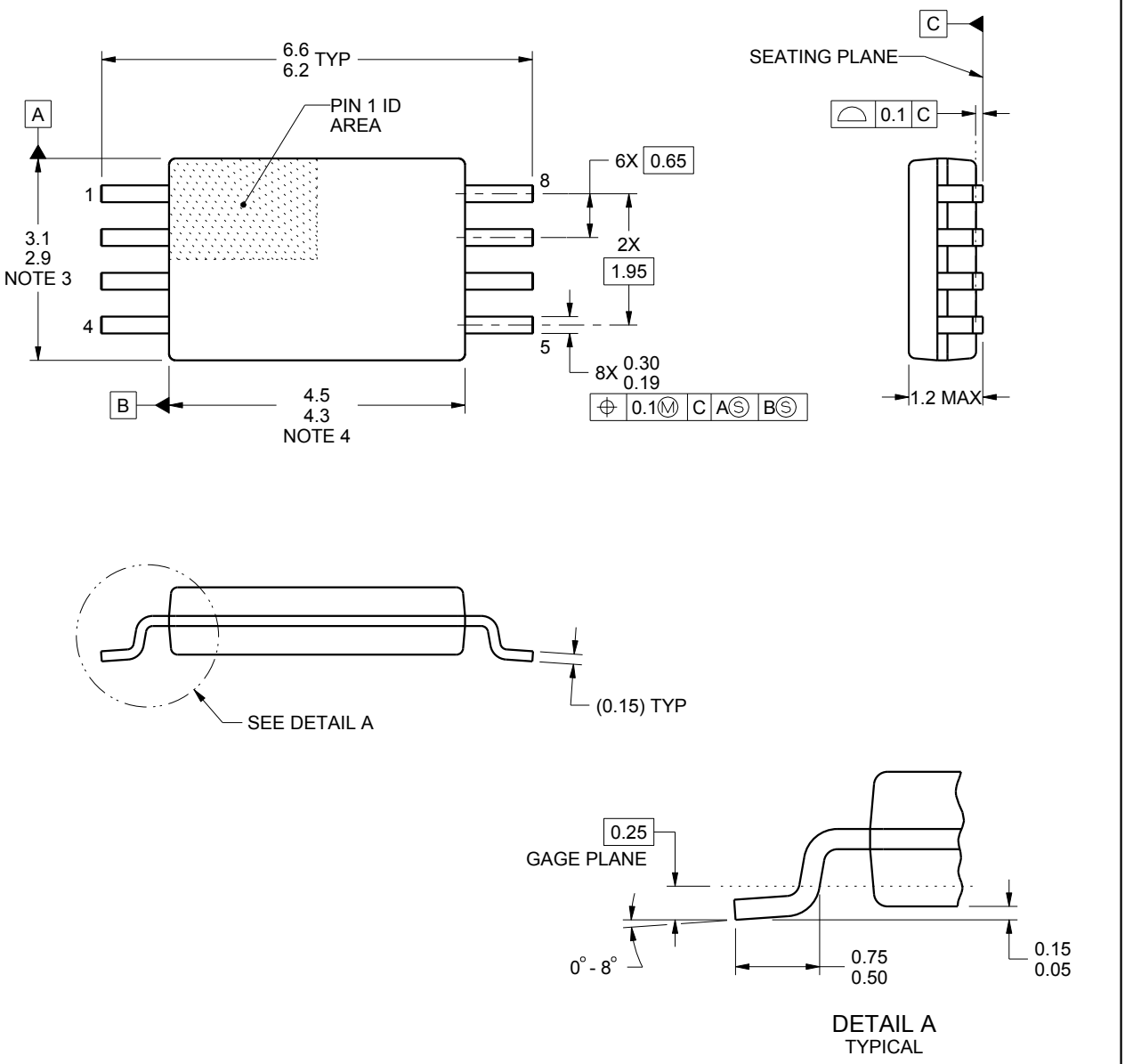
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# PACKAGE OUTLINE

## PW0008A

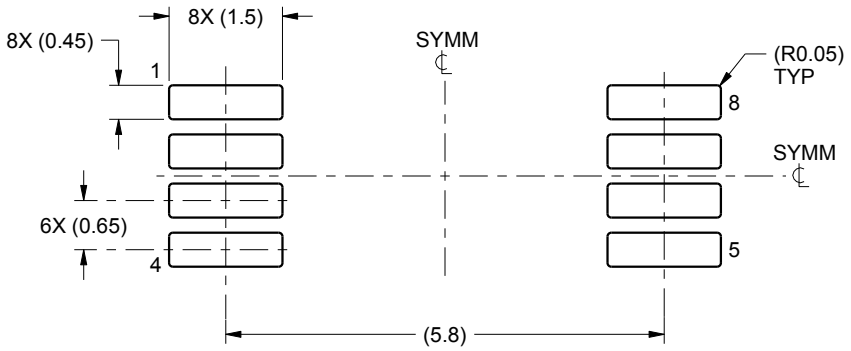
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

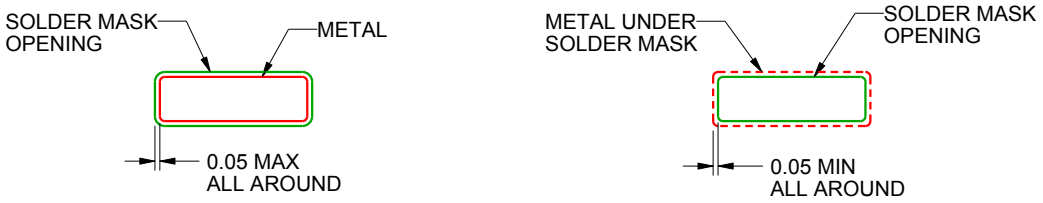



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.




LAND PATTERN EXAMPLE
SCALE:10X

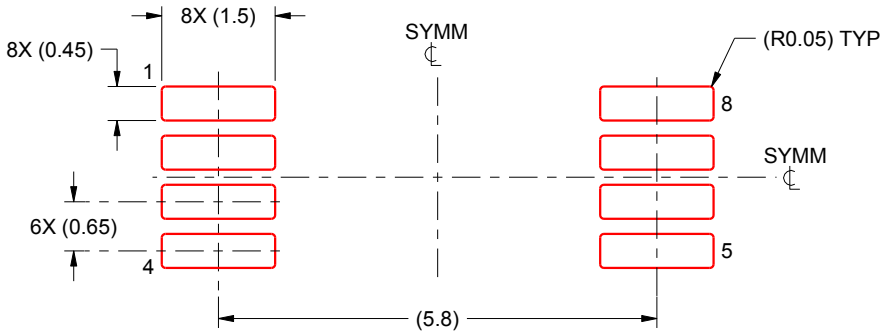



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

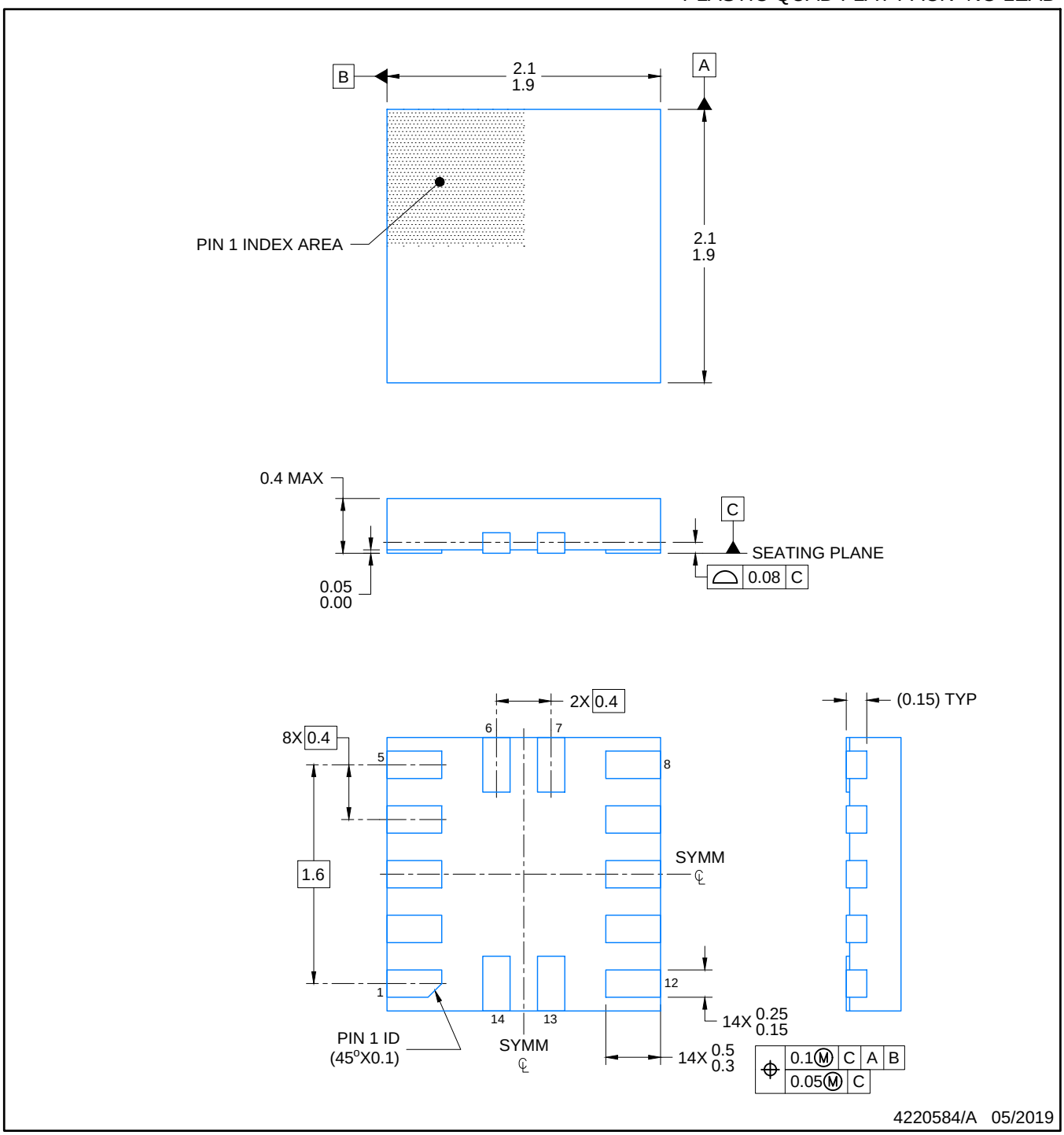
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## RUC0014A

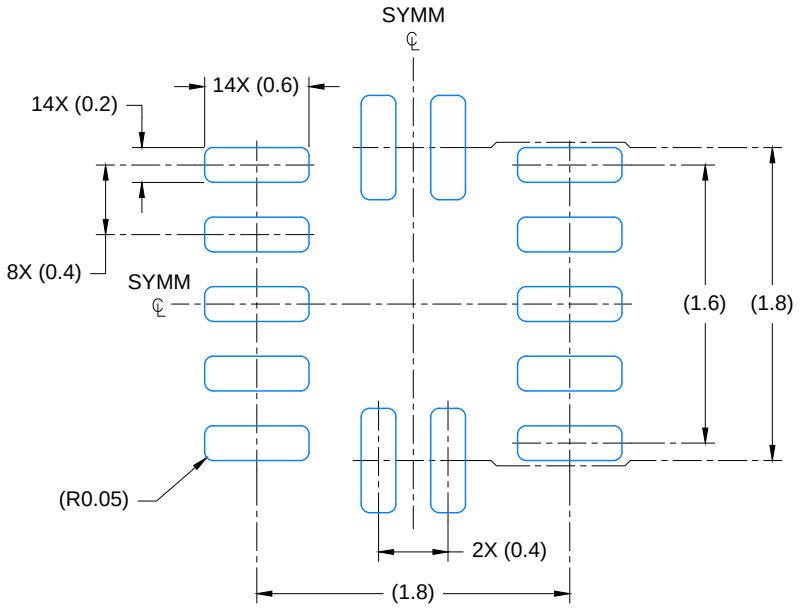
## X2QFN - 0.4 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD

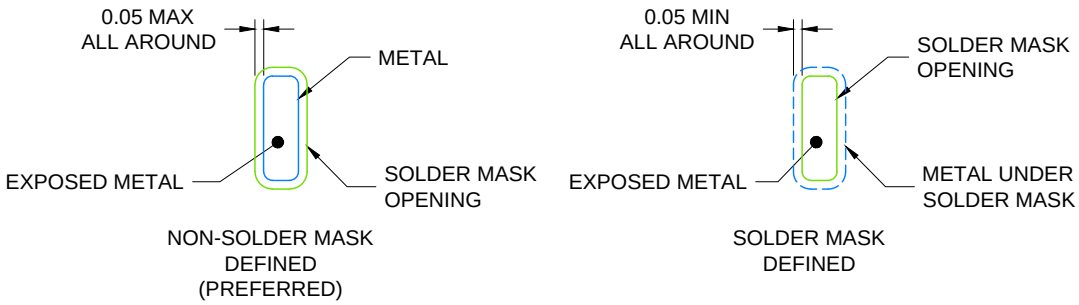



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 23X

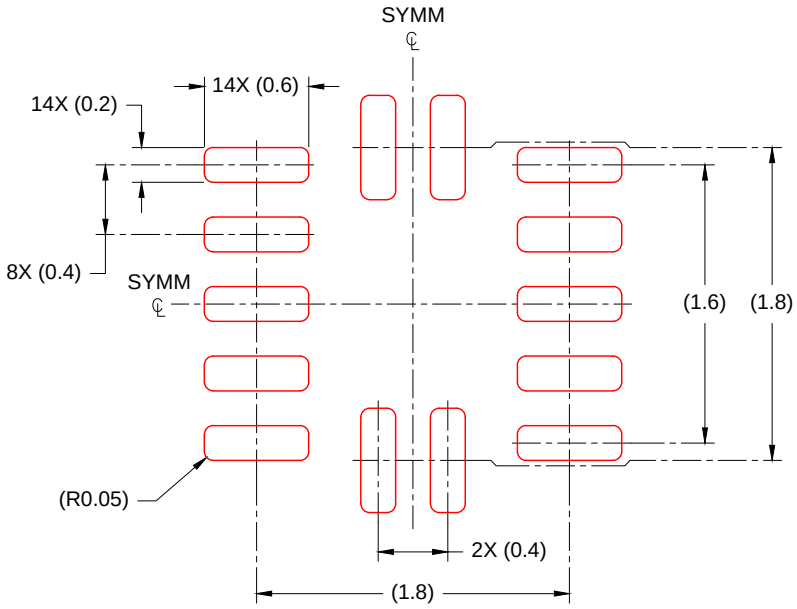



SOLDER MASK DETAILS

4220584/A 05/2019

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).




SOLDER PASTE EXAMPLE
BASED ON 0.100mm THICK STENCIL
SCALE: 23X

4220584/A 05/2019

NOTES: (continued)

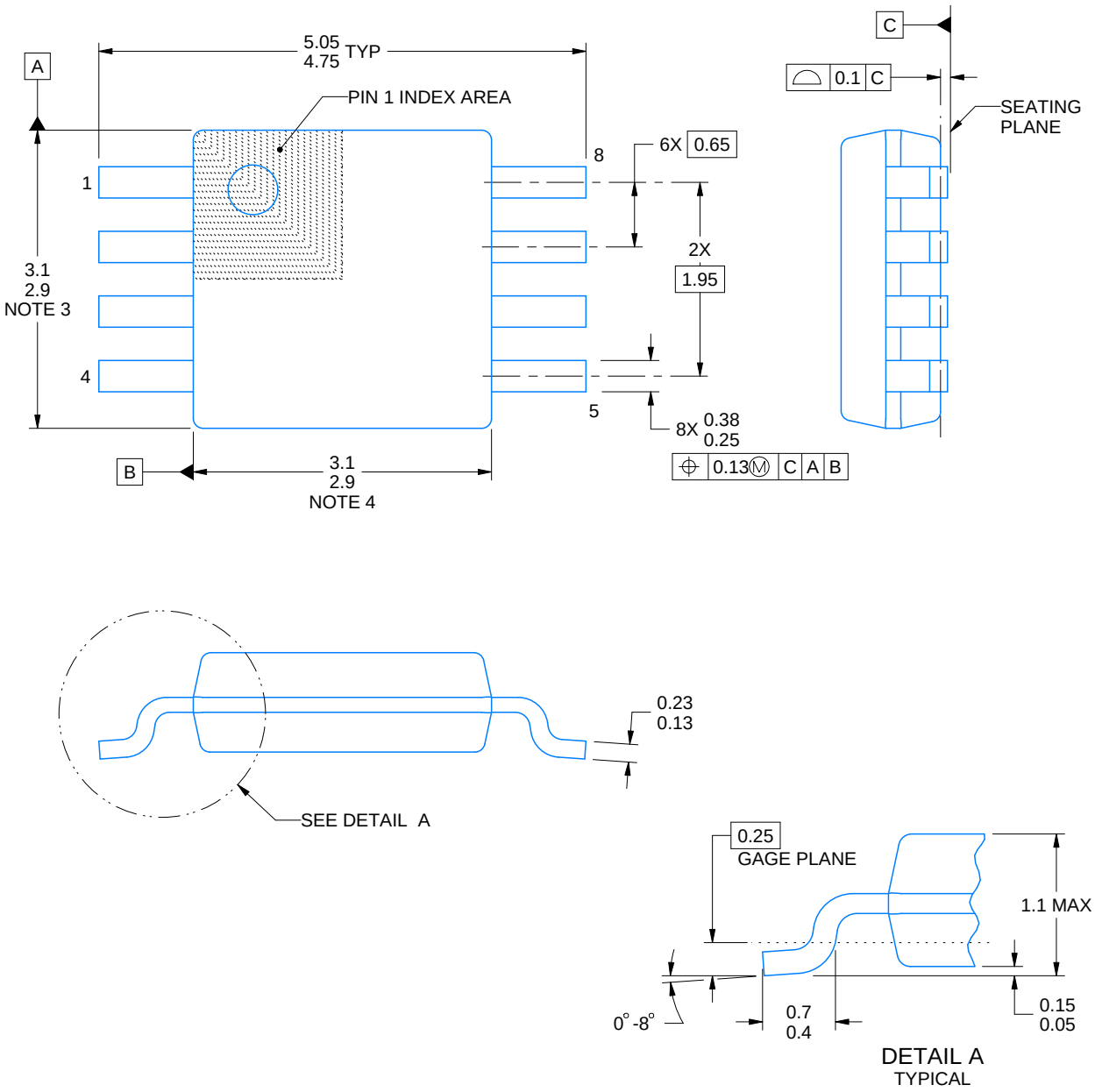
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# PACKAGE OUTLINE

## DGK0008A

## VSSOP - 1.1 mm max height

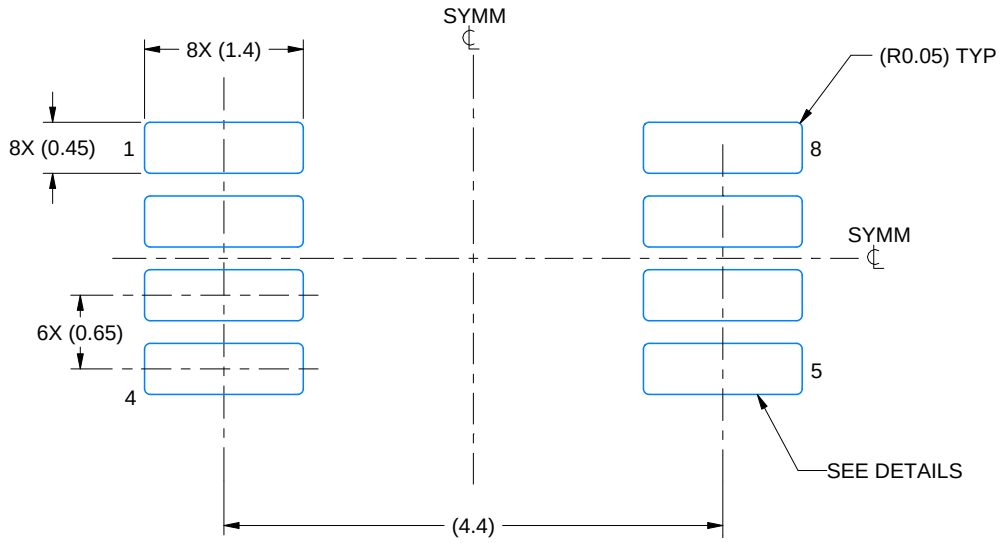
SMALL OUTLINE PACKAGE



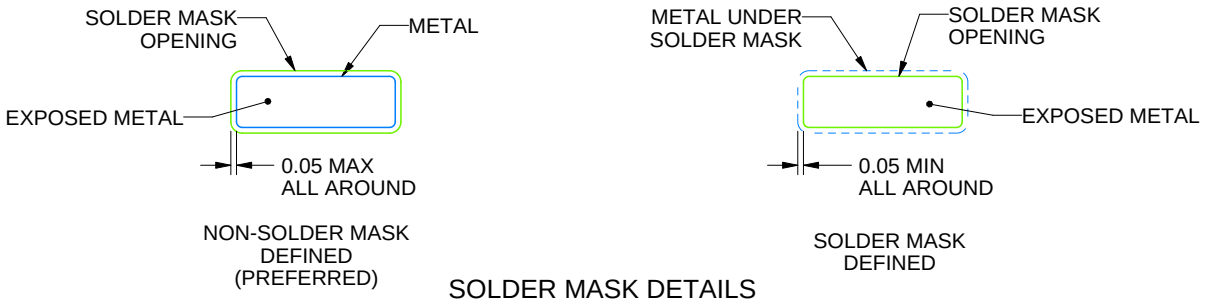

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

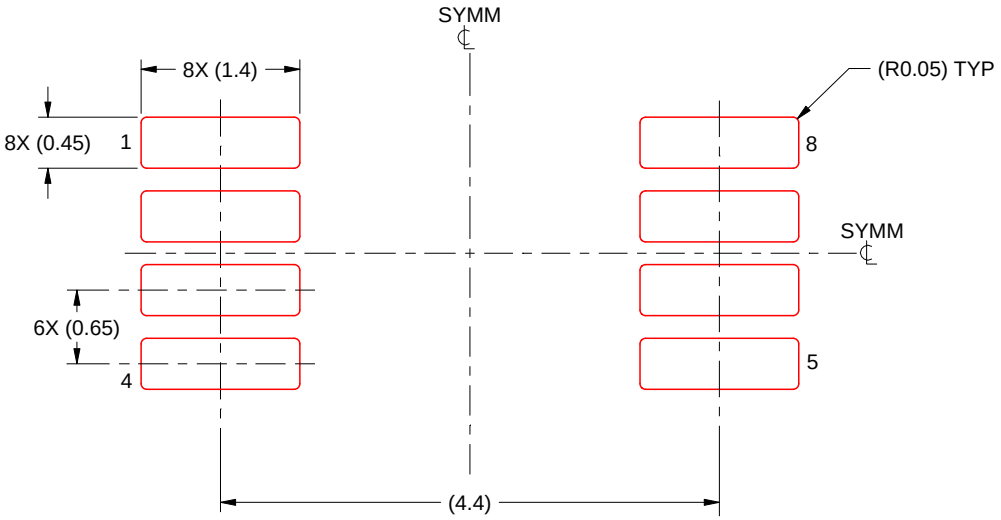



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.




SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

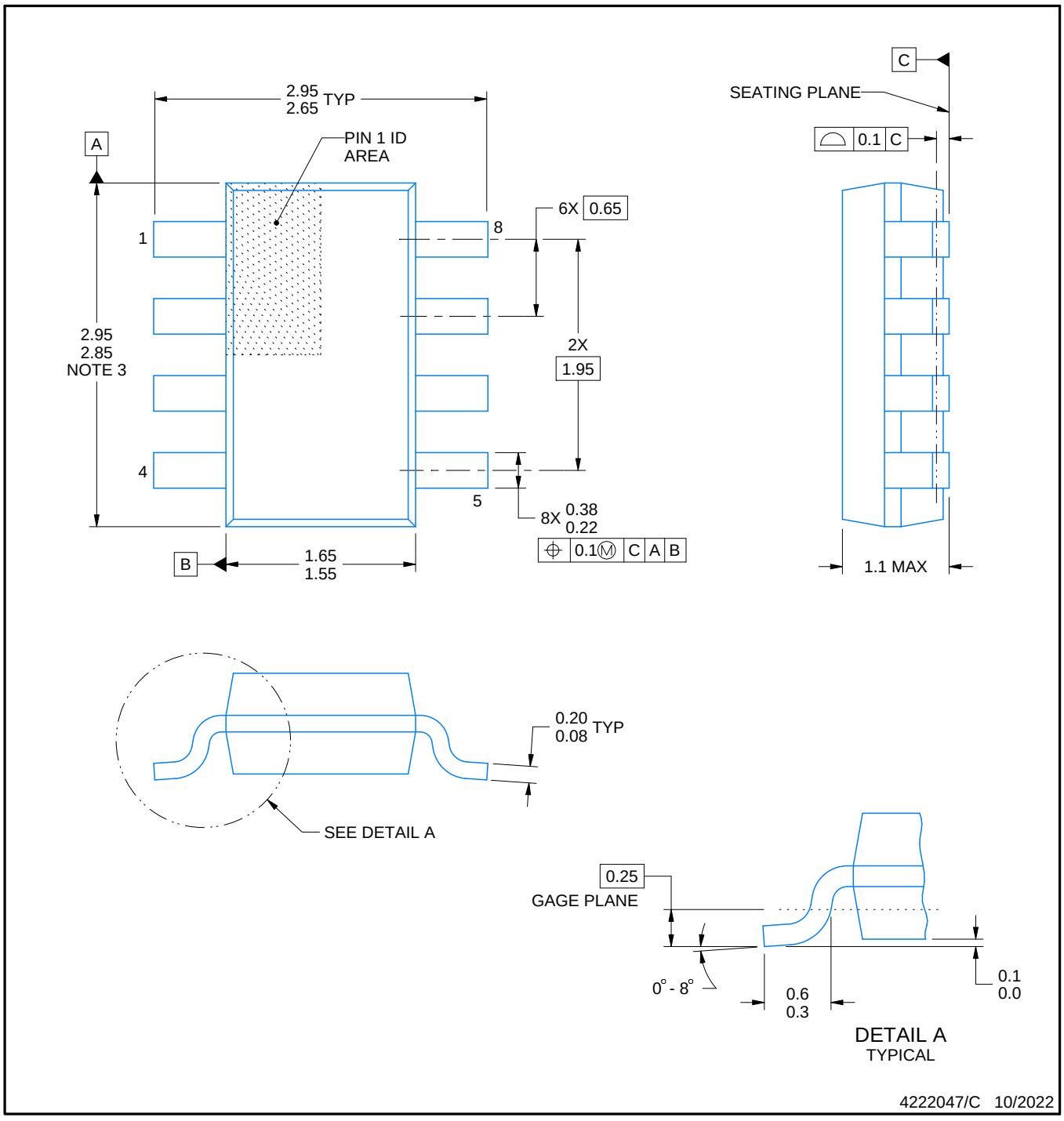
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DDF0008A

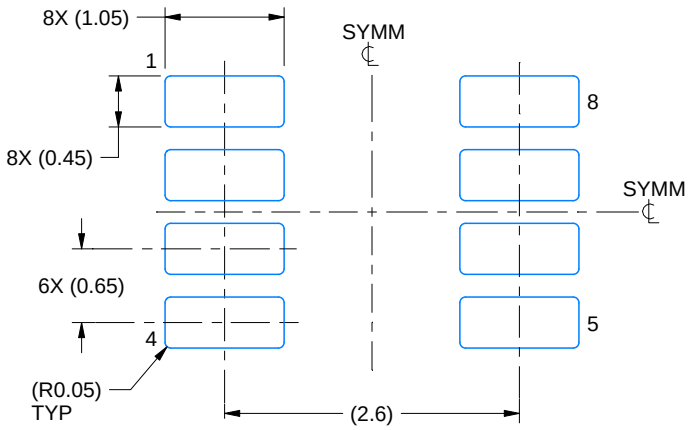
## SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE

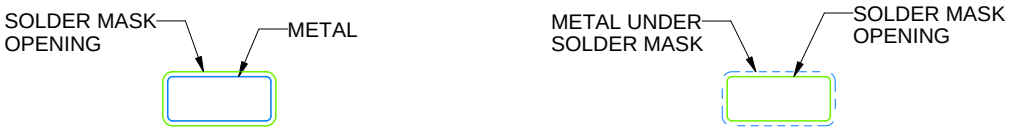



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.




LAND PATTERN EXAMPLE
SCALE:15X




NON SOLDER MASK
DEFINED

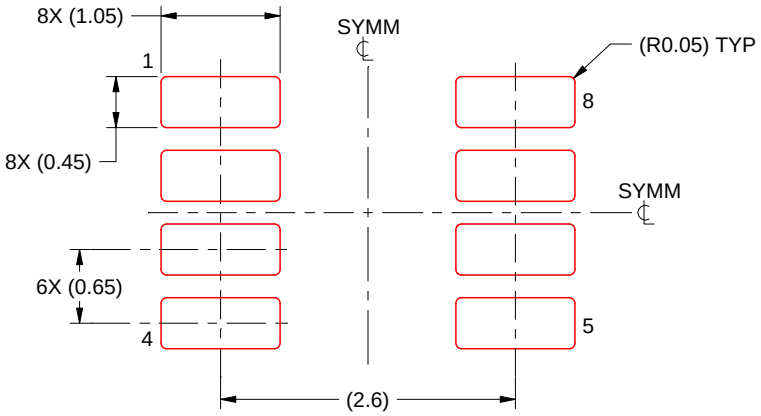
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222047/C 10/2022

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/C 10/2022

NOTES: (continued)

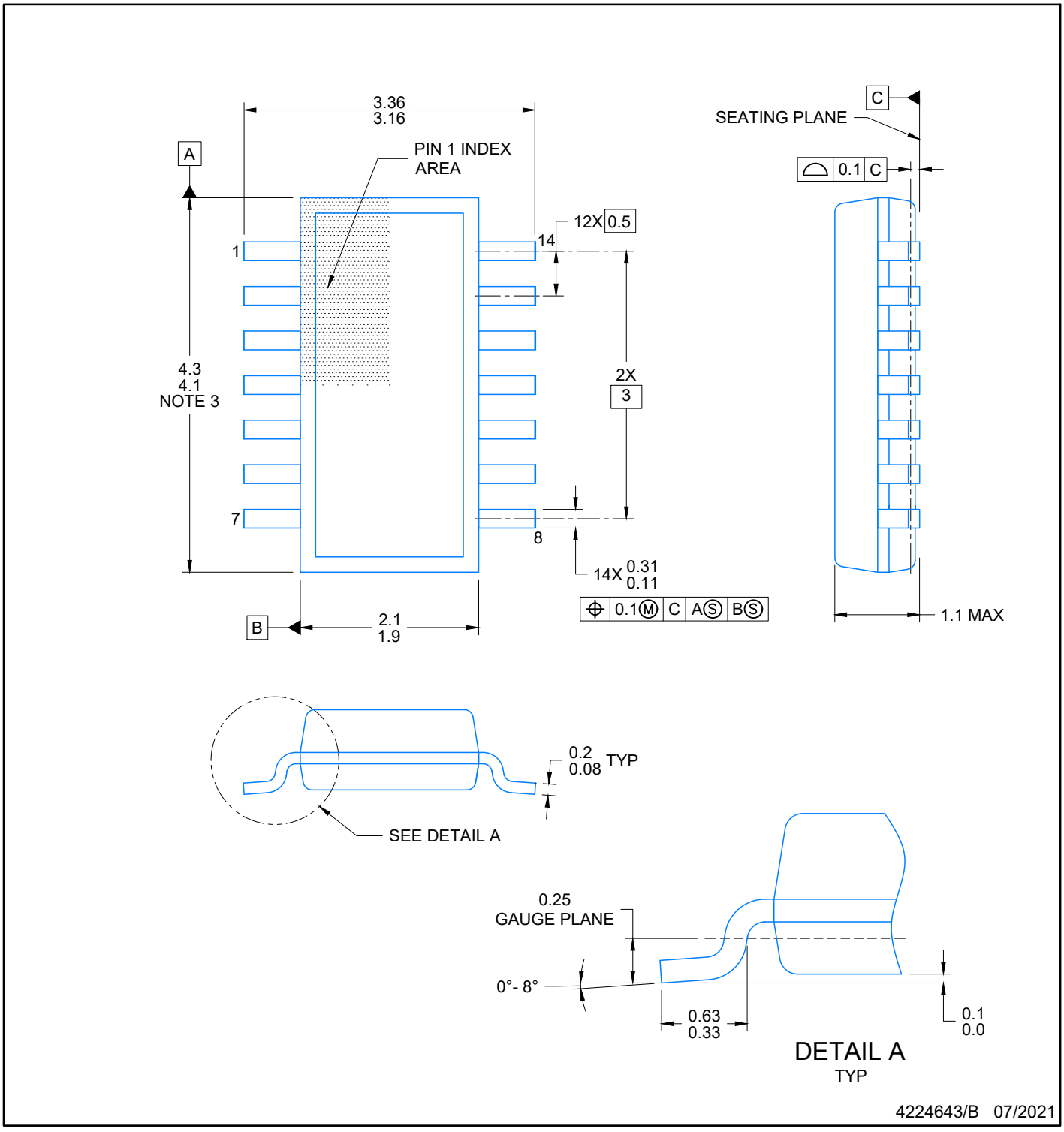
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DYY0014A

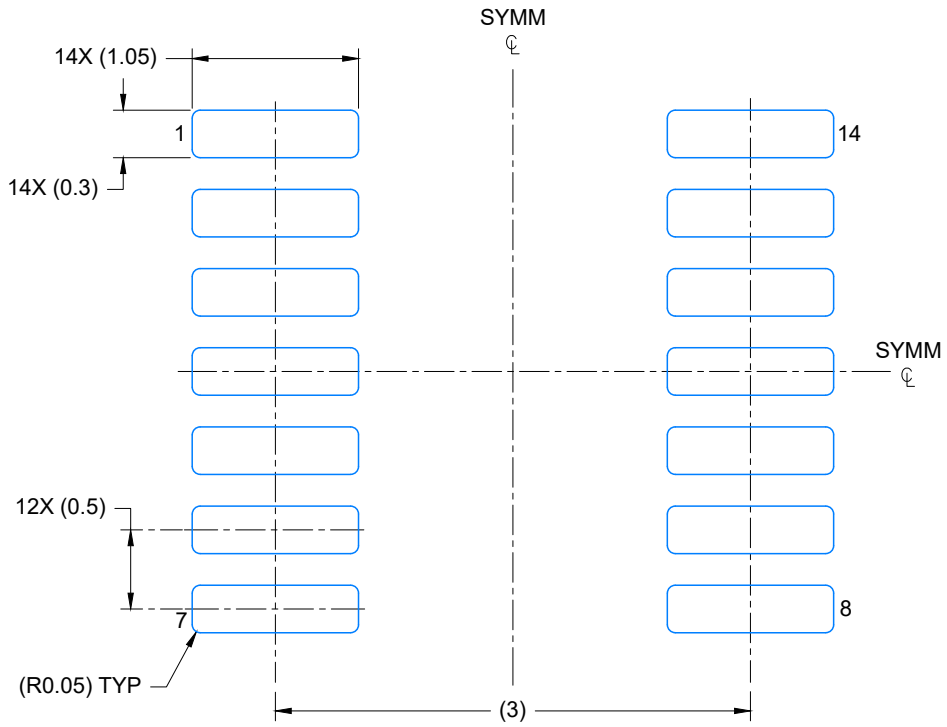
## SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

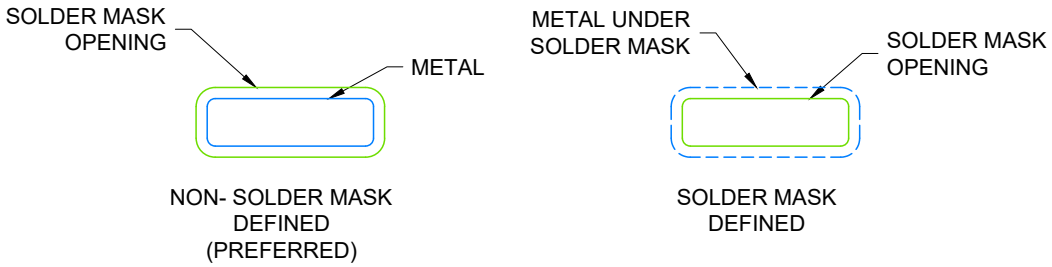



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X




SOLDER MASK DETAILS

4224643/B 07/2021

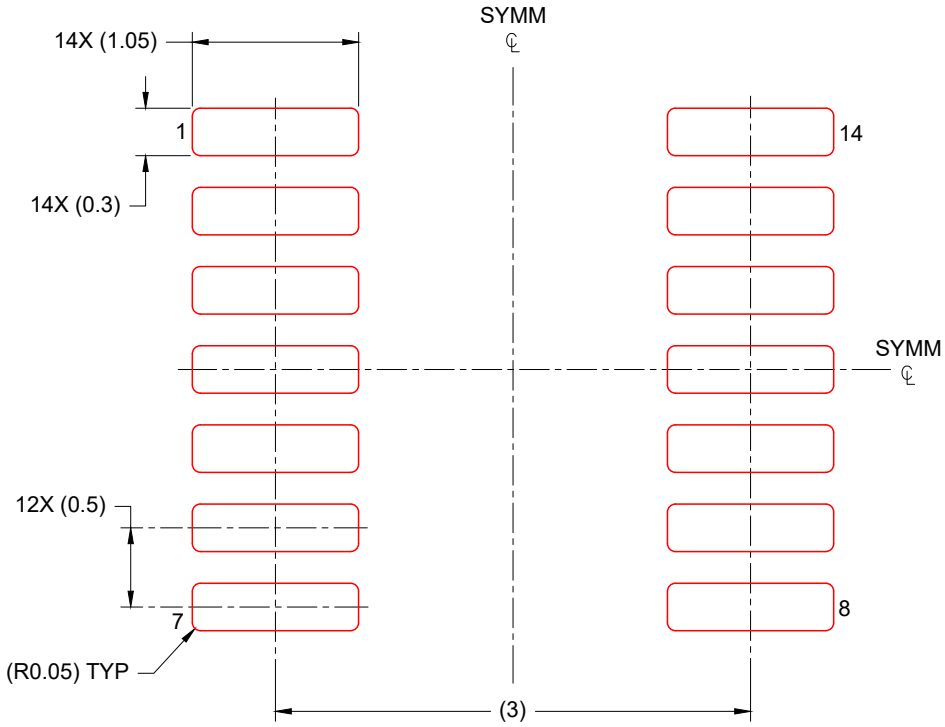
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224643/B 07/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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