TEXAS INSTRUMENTS
LMK3H0102
JAJSS15 – NOVEMBER 2023

LMK3H0102 リファレンスレス、2 差動または 5 シングルエンド出力、PCIe Gen 1～6 準拠、プログラマブル BAW クロック ジェネレータ

1 特長

- BAW 共振器を内蔵、外部リファレンスは不要
- フレキシブルな周波数生成：
  - 2 チャネル分圧器：2.5MHz～400MHz の範囲で最大 3 つの異なる出力周波数
  - 最大 200MHz までの LVCMOS 出力をサポート：1.8V、2.5V、または 3.3V
  - OUT0 ピンおよび OUT1 ピン上で AC-LVDS、DC-LVDS、LP-HCSL、LVCMOS の組み合わせ
  - 追加の LVCMOS 出力により最大 5 つの LVCMOS クロックを生成可能
- 総出力周波数安定性：±25ppm
- 2 つの機能モード：I²C または事前にプログラムされた OTP
  - 完全に構成可能な I²C アドレス
- 周囲温度：-40℃～85℃
- PCIe Gen 1～Gen 6 準拠：共通クロック (SSC、SRNS、SRIS あり / なし)
- 非常に小さい PCIe ジッタ：
  - PCIe Gen 3 の共通クロックのジッタ：140fs 以下 (PCIe の上限は 1ps)
  - PCIe Gen 4 の共通クロックのジッタ：140fs 以下 (PCIe の上限は 500fs)
  - PCIe Gen 5 の共通クロックのジッタ：45fs 以下 (PCIe の上限は 150fs)
  - PCIe Gen 6 の共通クロックのジッタ：45fs 以下 (PCIe の上限は 100fs)
- SSC 出力モードと非 SSC 出力モードの混合をサポート、PCIe Gen 1～Gen 6 のすべてに準拠
  - 2 つの SSC 出力、2 つの非 SSC 出力、または 1 つの SSC 出力と 1 つの非 SSC 出力
- プログラム可能な SSC 変調深度
  - 事前プログラム済み：-0.1%、-0.25%、-0.3%、および -0.5% のダウン スプレッド
  - 抵抗によるプログラミングが可能：-0.1%～-3% のダウン スプレッド、または ±0.05%～±1.5% のセンター スプレッド
- VDD = VDDO = 1.8V/2.5V/3.3V±5%
- 両方の出力が LP-HCSL の場合、消費電流が 60mA まで低下
- LP-HCSL 出力において、500kHz のスイッチング ノイズで -93.1dBc の PSNR を提供する内蔵 LDO
- スタートアップ時間：<5ms
- 出力間スキュー：<50ps
- フェイルセーフ 入力および VDD ピン

2 アプリケーション

- PCIe Gen 1～Gen 6 のクロック生成
- サーバー・マザーボード
- NIC、SmartNIC
- ハードウェア・アクセラレータ
- PCIe SSD
- アドイン カード、PCIe 拡張カード
- 複合機 (マルチファンクション プリンタ)

3 概要

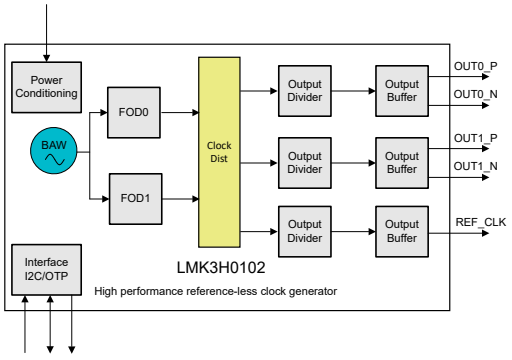
LMK3H0102 は、スペクトラム拡散クロック (SSC) をサポートする、2 出力 PCIe Gen 1～Gen 6 準拠のリファレンスレス クロック ジェネレータです。このデバイスは、テキサス・インスツルメンツ独自のバルク弾性波 (BAW) 技術に基づいており、水晶振動子や外部クロック リファレンスを用いずに、±25ppm のクロック出力を供給します。このデバイスは、2 つの SSC クロック、2 つの非 SSC クロック、または 1 つの SSC クロックと 1 つの非 SSC クロックを同時に供給できます。このデバイスは、SSC ありまたは SSC なしの共通クロック、SRNS (Separate Reference No Spread)、SRIS (Separate Reference Independent Spread) など、Gen 1 から Gen 6 までの PCIe に完全準拠しています。

このデバイスは、GPIO ピンや I²C インターフェイスを介して簡単に構成できます。デバイスへの電力供給には、外付けの DC/DC 回路を使用できます。電源のフィルタ処理と DC/DC 回路からの電源供給に関する詳細なガイドラインについては、「電源に関する推奨事項」 を参照してください。

パッケージ情報

部品番号	パッケージ (1)	パッケージ・サイズ (2)
LMK3H0102	RER (TQFN、16)	3.0mm × 3.0mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



概略ブロック図

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4 Pin Configuration and Functions

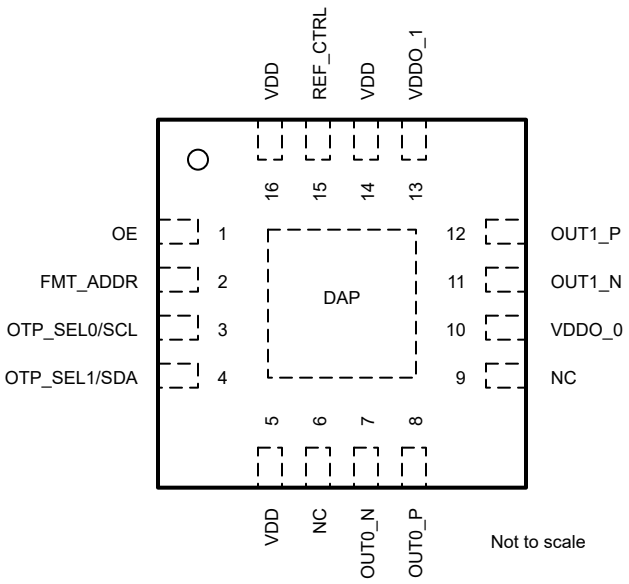

図 4-1. LMK3H0102 16-Pin TQFN Top View

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
OUT0_P, OUT0_N	8, 7	O	Clock output 0. Supports LP-HCSL (85 Ω or 100 Ω), LVDS or 1.8-V/2.5-V/3.3-V LVCMOS.
OUT1_P, OUT1_N	12, 11	O	Clock output 1. Supports LP-HCSL (85 Ω or 100 Ω), LVDS or 1.8-V/2.5-V/3.3-V LVCMOS.
REF_CTRL (REF_CLK)	15	I/O	Multifunctional pin. At power up, the state of this pin is latched to select the functionality of Pin 2, Pin 3 and Pin 4. Pull low or leave floating for I2C mode or high for OTP mode prior to power-up. After power-up, this pin can be programmed as an additional LVCMOS output (REF_CLK), active-high CLK_READY signal (default), or disabled. See REF_CTRL Operation for more details. This pin has an 880-kΩ internal pulldown resistor.
OE	1	I	Global Output Enable. Active low. 2-state logic input pin. This pin has a 75-kΩ internal pulldown resistor. See Output Enable for more details. • Low/Floating: OUT0 and OUT1 enabled • High: OUT0 and OUT1 disabled
FMT_ADDR	2	I	Multifunctional pin. Functionality is determined by REF_CTRL (pin 15) at power up. See OTP Mode and I2C Mode for more details. This pin has an 880-kΩ internal pulldown resistor. • I2C Mode: This pin selects the I2C address. • OTP Mode: This pin sets the output format.
OTP_SEL0/SCL, OTP_SEL1/SDA	3, 4	I, I/O	Multifunctional pin. Functionality is determined by REF_CTRL (pin 15) at power up. See OTP Mode and I2C Mode for details. These pins have 880-kΩ internal pulldown resistors. • I2C Mode: These pins are the I2C clock and data connections. • OTP Mode: These pins select the OTP page.

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表 4-1. Pin Functions (続き)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
VDD	5, 14, 16	P	1.8-V, 2.5-V or 3.3-V device power supply. A 0.1-µF capacitor must be placed as close to each of the pins as possible.
VDDO_0, VDDO_1	10, 13	P	1.8-V, 2.5-V or 3.3-V OUT0 and OUT1 power supply. If VDD is 1.8 V or 2.5 V, the VDDO pins must be the same voltage as VDD. A 0.1-µF capacitor must be placed as close to each of the pins as possible.
NC	6, 9	N/A	No connect. Pins can be connected to GND, VDD, or otherwise tied to any potential within the Supply Voltage range stated in the *Absolute Maximum Ratings*.
DAP	17	G	GND

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

表 4-2. BLOT

NAME	NO.	TYPE(1)	DESCRIPTION
OUT0_N	7	O	Clock output 0. Supports LP-HCSL (85 Ω or 100 Ω), LVDS or 1.8-V/2.5-V/3.3-V LVCMOS.
OUT0_P	8	O	Clock output 0. Supports LP-HCSL (85 Ω or 100 Ω), LVDS or 1.8-V/2.5-V/3.3-V LVCMOS.
OUT1_N	11	O	Clock output 1. Supports LP-HCSL (85 Ω or 100 Ω), LVDS or 1.8-V/2.5-V/3.3-V LVCMOS.
OUT1_P	12	O	Clock output 1. Supports LP-HCSL (85 Ω or 100 Ω), LVDS or 1.8-V/2.5-V/3.3-V LVCMOS.
REF_CTRL	15	I/O	Multifunctional pin. At power up, the state of this pin is latched to select the functionality of Pin 2, Pin 3 and Pin 4. Pull low or leave floating for I2C mode or high for OTP mode prior to power-up. After power-up, this pin can be programmed as an additional LVCMOS output (REF_CLK), active-high CLK_READY signal (default), or disabled. See REF_CTRL Operation for more details. This pin has an 880-kΩ internal pulldown resistor.
OE	1	I	Global Output Enable. Active low. 2-state logic input pin. This pin has a 75-kΩ internal pulldown resistor. See Output Enable for more details. • Low/Floating: OUT0 and OUT1 enabled • High: OUT0 and OUT1 disabled
FMT_ADDR	2	I	Multifunctional pin. Functionality is determined by REF_CTRL (pin 15) at power up. See *OTP Mode* and *I²C Mode* for more details. This pin has a 75-kΩ internal pulldown resistor. • I2C Mode: This pin selects the I2C address. • OTP Mode: This pin sets the output format.
OTP_SEL0/SCL,	3	I	Multifunctional pin. Functionality is determined by REF_CTRL (pin 15) at power up. See *OTP Mode* and *I²C Mode* for more details. • I2C Mode: These pins are the I2C clock and data connections. • OTP Mode: These pins select the OTP page.
OTP_SEL1/SDA	4	I/O	Multifunctional pin. Functionality is determined by REF_CTRL (pin 15) at power up. See *OTP Mode* and *I²C Mode* for more details. • I2C Mode: These pins are the I2C clock and data connections. • OTP Mode: These pins select the OTP page.
VDD	5	P	1.8-V, 2.5-V or 3.3-V device power supply. A 0.1-µF capacitor must be placed as close to each of the pins as possible.
VDD	14	P	1.8-V, 2.5-V or 3.3-V device power supply. A 0.1-µF capacitor must be placed as close to each of the pins as possible.
VDD	16	P	1.8-V, 2.5-V or 3.3-V device power supply. A 0.1-µF capacitor must be placed as close to each of the pins as possible.

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表 4-2. BLOT (続き)

NAME	NO.	TYPE(1)	DESCRIPTION
VDDO_0	10	P	1.8-V, 2.5-V or 3.3-V OUT0 and OUT1 power supply. If VDD is 1.8 V or 2.5 V, the VDDO pins must be the same voltage as VDD. A 0.1-µF capacitor must be placed as close to each of the pins as possible.
VDDO_1	13	P	1.8-V, 2.5-V or 3.3-V OUT0 and OUT1 power supply. If VDD is 1.8 V or 2.5 V, the VDDO pins must be the same voltage as VDD. A 0.1-µF capacitor must be placed as close to each of the pins as possible.
NC	6	N/A	No connect. Pins can be connected to GND, VDD, or otherwise tied to any potential within the Supply Voltage range stated in the *Absolute Maximum Ratings*.
NC	9	N/A	No connect. Pins can be connected to GND, VDD, or otherwise tied to any potential within the Supply Voltage range stated in the *Absolute Maximum Ratings*.
DAP	–	G	GND

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD}	Device supply voltage	–0.3	3.9	V
V_{DDO}	Output supply voltage	–0.3	3.9	V
V_{IN}	Logic input voltage (V_{DD} = V_{DDO} = -0.3 to 3.9 V)	–0.3	3.9	V
V_{OUT}	Voltage applied to OUTx_P and OUTx_N pins (when outputs are high or low)	–0.3	V_{DDO_x} + 0.3	V
	Voltage applied to OUTx_P and OUTx_N pins (when outputs are LVCMOS tri-state)	–0.3	1.89	V
	Voltage applied to OUTx_P and OUTx_N pins (when outputs are LP-HCSL or LVDS tri-state)	–0.3	1.5	V
T_J	Junction temperature		105	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

V_{DD} = V_{DDO} = 1.8 V, 2.5 V or 3.3 V ± 5%, T_A = $T_{A,min}$ to $T_{A,max}$

		MIN	NOM	MAX	UNIT
V_{DD}	Device supply voltage	1.71	1.8	1.89	V
		2.375	2.5	2.625	V
		3.135	3.3	3.465	V
V_{DDO}	Output supply voltage	1.71	1.8	1.89	V
		2.375	2.5	2.625	V
		3.135	3.3	3.465	V
T_A	Ambient temperature	–40		85	°C
T_J	Junction temperature	–40		125	°C
t_{ramp}	Power supply ramp time. V_{DD} = 1.8 V	0.05		5	ms
t_{ramp}	Power supply ramp time. V_{DD} = 2.5 V or 3.3 V	0.05		5	ms

5.4 Thermal Information

THERMAL METRIC(1)		DEVICE PKG DES (PKG FAM) PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	TBD	°C/W

THERMAL METRIC(1)		DEVICE	UNIT
		PKG DES (PKG FAM)	
		PINS	
$R_{\theta JB}$	Junction-to-board thermal resistance	TBD	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	TBD	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	TBD	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

V_{DD} = V_{DDO} = 1.8 V, 2.5 V or 3.3 V ± 5%, T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FREQUENCY STABILITY						
Δf_{total}	Total frequency stability		–25		25	ppm
Δf_{init}	Initial frequency stability	T_A = 25°C	–1		1	ppm
Δf_{temp}	Frequency stability due to temperature	Over Recommended Operating Condition, dT/dt < 10°K/min	–10		10	ppm
Δf_{aging}	Frequency stability due to aging	10 years at 25°C	TBD		TBD	ppm
LP-HCSL CLOCK OUTPUT CHARACTERISTICS						
f_{out}	Output frequency		2.5		400	MHz
V_{min}	Output low voltage (undershoot included)		–60		25	mV
$V_{overshoot}$	Overshoot voltage. V_{max} - V_{OH}				150	mV
$V_{OH,2.5/3.3}$	Output high voltage. VDD = 2.5 V or 3.3 V	code = 0	594	625	656	mV
		code = 1	614	647	679	mV
		code = 2	635	668	702	mV
		code = 3	656	690	725	mV
		code = 4	676	712	747	mV
		code = 5	697	733	770	mV
		code = 6 (default)	717	755	793	mV
		code = 7	738	777	816	mV
		code = 8	758	798	838	mV
		code = 9	779	820	861	mV
		code = 10	800	842	884	mV
		code = 11	820	863	907	mV
		code = 12	841	885	929	mV
		code = 13	861	907	952	mV
		code = 14	882	928	975	mV
		code = 15	903	950	998	mV

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V_{DD} = V_{DDO} = 1.8 V, 2.5 V or 3.3 V ± 5%, T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH,1.8}$	Output high voltage. VDD = 1.8 V	code = 0	563	625	688	mV
		code = 1	582	647	712	mV
		code = 2	601	668	735	mV
		code = 3	621	690	759	mV
		code = 4	641	712	783	mV
		code = 5	660	733	806	mV
		code = 6 (default)	680	755	831	mV
		code = 7	699	777	855	mV
		code = 8	718	798	878	mV
		code = 9	738	820	902	mV
		code = 10	758	842	926	mV
		code = 11	777	863	949	mV
		code = 12	797	885	974	mV
		code = 13	816	907	998	mV
		code = 14	835	928	1021	mV
		code = 15	855	950	1045	mV
Z_{diff}	LP-HCSL static differential impedance		80.75	85	91.25	Ω
			95	100	105	Ω
dV/dt	Output slew rate (rising and falling edge)	Measured from –150 mV to +150 mV on the differential waveform, centered on the zero crossing point. OUTx_SLEW_RATE = 0 (TBD)(1)	2.1		3.1	V/ns
		Measured from –150 mV to +150 mV on the differential waveform, centered on the zero crossing point. OUTx_SLEW_RATE = 0(1)	2.3		3.5	V/ns
		Measured from –150 mV to +150 mV on the differential waveform, centered on the zero crossing point. OUTx_SLEW_RATE = 1(1)	2		3.2	V/ns
		Measured from –150 mV to +150 mV on the differential waveform, centered on the zero crossing point. OUTx_SLEW_RATE = 2(1)	1.7		2.8	V/ns
		Measured from –150 mV to +150 mV on the differential waveform, centered on the zero crossing point. OUTx_SLEW_RATE = 3(1)	1.4		2.7	V/ns
ΔdV/dt	Rising edge rate to falling edge rate matching	See(1)			3	%
ODC	Output duty cycle	See(1)	49.9		50.3	%
		f_{out} ≤ 325 MHz	48.8		50.8	%
		325 MHz < f_{out} ≤ 400 MHz	48.6		51.8	%
t_{skew}	Output to output skew	Same FOD, LP-HCSL output			50	ps
V_{cross}	Absolute crossing point voltage	See(1)	280		480	mV
ΔV_{cross}	Variation of V_{cross} over all clock edges	See(1)			30	mV
$\|V_{RB}\|$	Absolute value of ring back voltage	See(1)	100			mV
t_{stable}	Time before V_{RB} is allowed	See(1)	500			ps
$J_{cycle-to-cycle}$	Cycle to cycle jitter, Common Clock no SSC	See(1)			150	ps

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V_{DD} = V_{DDO} = 1.8 V, 2.5 V or 3.3 V ± 5%, T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$J_{cycle-to-cycle}$	Cycle to cycle jitter, Common Clock, -0.5% SSC	See(1)			150	ps
t_{period_abs}	Absolute period including jitter and SSC	See(1)	9.949	10	10.101	ns
$t_{period\_avg\_CC}$	Average clock period accuracy, Common Clock	See(1)	–100		2600	ppm
$t_{period\_avg\_SRIS}$	Average clock period accuracy, SRIS	See(1)	–100		1600	ppm
LVDS CLOCK OUTPUT CHARACTERISTICS						
f_{out}	Output frequency		2.5		400	MHz
$\|V_{OD}\|$	Steady-state magnitude of the differnetial output voltage $\|V_{OUTP} - V_{OUTN}\|$	100 Ω external termination	250	350	450	mV
$\Delta V_{pp-diff}$	Change in differential output voltage swing between complementary output states	100 Ω external termination			50	mV
V_{OS}	Output offset voltage (common mode voltage)	V_{DDO} = 3.3 V, 100 Ω external termination	1.12	1.2	1.365	V
		V_{DDO} = 2.5 V, 100 Ω external termination	1.1	1.2	1.345	V
		V_{DDO} = 1.8 V, 100 Ω external termination	0.8		0.97	V
ΔV_{OS}	Change in V_{OS} between complementary output states				50	mV
I_{SA}, I_{SB}	Short-circuit current. Magnitude of current with the generator output terminals short-circuited to the generator circuit common		–24		24	mA
I_{SAB}	Short-circuit current. Magnitude of current with generator output terminals short-circuited to each other		–12		12	mA
t_R, t_F	20% to 80% differential rise/fall time	PADCAP_CHx = 0	195		315	ps
		PADCAP_CHx = 1	250		440	ps
		PADCAP_CHx = 2	270		610	ps
		PADCAP_CHx = 3	280		800	ps
t_{skew}	Output to output skew	Same FOD, LVDS output			50	ps
ODC	Output duty cycle		49		51.1	%
LVCMOS CLOCK OUTPUT CHARACTERISTICS						
f_{out}	Output frequency		2.5		200	MHz
dV/dt	Output slew rate	V_{DDO} = 3.3 V ± 5%, measured from 20% to 80%, 4.7 pF load	2.6		4.7	V/ns
		V_{DDO} = 2.5 V ± 5%, measured from 20% to 80%, 4.7 pF load	2.6		3.7	V/ns
		V_{DDO} = 1.8 V ± 5%, measured from 20% to 80%, 4.7 pF load	1		3.2	V/ns
V_{OH}	Output high voltage	I_{OH} = –15 mA at 3.3 V	0.8 x V_{DDO}		V_{DDO}	V
		I_{OH} = –12 mA at 2.5 V				
		I_{OH} = –8 mA at 1.8 V				
V_{OL}	Output low voltage	I_{OL} = 15 mA at 3.3 V			0.4	V
		I_{OL} = 12 mA at 2.5 V				
		I_{OL} = 8 mA at 1.8 V				
I_{leak}	Output leakage current	Output tri-stated. V_{DD} = V_{DDO} = 3.465 V	–5	0	5	µA
R_{out}	Output impedance			17		Ω
ODC	Output duty cycle	f_{out} ≤ 156.25 MHz	45		55	%
		f_{out} > 156.25 MHz	40		60	%

ADVANCE INFORMATION

V_{DD} = V_{DDO} = 1.8 V, 2.5 V or 3.3 V ± 5%, T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{skew}	Output-to-output skew	Same FOD, LVCMOS output			50	ps
C_{load}	Maximum load capacitance				15	pF
LVCMOS REFCLK CHARATERISTICS						
f_{out}	Output frequency	See(2)	12.5(3)		200	MHz
dV/dt	Output slew rate	V_{DDO} = 3.3 V ± 5%, measured from 20% to 80%, 4.7 pF load(2)	2.6		6.7	V/ns
		V_{DDO} = 2.5 V ± 5%, measured from 20% to 80%, 4.7 pF load(2) (4)	1.8		4.5	V/ns
		V_{DDO} = 1.8 V ± 5%, measured from 20% to 80%, 4.7 pF load(2) (4)	1		3.2	V/ns
I_{leak}	Output leakage current	Output tri-stated. V_{DD} = V_{DDO} = 3.465 V(2) (4)	–5		5	µA
R_{out}	Output impedance			17		Ω
ODC	Output duty cycle	f_{out} ≤ 156.25 MHz(2)	45		55	%
ODC	Output duty cycle	f_{out} > 156.25 MHz(2)	40		60	%
C_{load}	Maximum load capacitance	See(2)			15	pF
RJ	Random jitter	12 kHz to 20 MHz integrated jitter at 50 MHz(2)			0.5	ps
SSC CHARACTERISTICS						
f_{out}	Output frequency range that supports SSC (any output format)		2.5		200	MHz
f_{SSC}	SSC modulation frequency		30	31.5	33	kHz
$f_{SSC-deviation}$	SSC deviation (modulation depth)	Down spread (programmable)	–3		–0.1	%
		Center spread (programmable)	±0.05		±1.5	%
$f_{SSC-deviation-accuracy}$	SSC deviation accuracy	f_{out} ≤ 100 MHz, down spread	0		0.01	%
		100 MHz < f_{out} ≤ 200 MHz, down spread	0		0.05	%
		f_{out} ≤ 100 MHz, center spread	0		0.01	%
		100 MHz < f_{out} ≤ 200 MHz, center spread	0		0.05	%
df/dt	max SSC frequency slew rate	0 < $f_{SSC-deviation}$ ≤ –0.5%			1250	ppm/us
JITTER CHARACTERISTICS						
$J_{PCIe1-cc-SSC\_off}$	PCIe Gen 1 Common Clock jitter, SSC is off (jitter limit = 86 ps)	SSC disabled on both outputs			0.4	ps
$J_{PCIe1-cc-SSC\_on}$	PCIe Gen 1 Common Clock jitter, –0.5% ≤ SSC < 0% (jitter limit = 86 ps)	SSC enabled on both outputs			0.7	ps
$J_{PCIe2-cc-SSC\_off}$	PCIe Gen 2 Common Clock jitter, SSC is off (jitter limit = 3 ps)	SSC disabled on both outputs		0.1	0.2	ps
$J_{PCIe2-cc-SSC\_on}$	PCIe Gen 2 Common Clock jitter, –0.5% ≤ SSC < 0% (jitter limit = 3 ps)	SSC enabled on both outputs		0.2	0.35	ps
$J_{PCIe2-SRNS}$	PCIe Gen 2 SRNS jitter	SSC disabled on both outputs		0.1	0.26	ps
$J_{PCIe2-SRIS}$	PCIe Gen 2 SRIS jitter, –0.3% ≤ SSC < 0%	SSC enabled on both outputs		0.2	0.36	ps
$J_{PCIe3-cc-SSC\_off}$	PCIe Gen 3 Common Clock jitter, SSC is off (jitter limit = 1 ps)	SSC disabled on both outputs		32.8	60	fs
$J_{PCIe3-cc-SSC\_on}$	PCIe Gen 3 Common Clock jitter, –0.5% ≤ SSC < 0% (jitter limit = 1 ps)	SSC enabled on both outputs		55.4	109	fs
$J_{PCIe3-SRNS}$	PCIe Gen 3 SRNS jitter	SSC disabled on both outputs		35.9	67	fs
$J_{PCIe3-SRIS}$	PCIe Gen 3 SRIS jitter, –0.3% ≤ SSC < 0%	SSC enabled on both outputs		155.6	317	fs

ADVANCE INFORMATION

V_{DD} = V_{DDO} = 1.8 V, 2.5 V or 3.3 V ± 5%, T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$J_{PCIe4\text{-}cc\text{-}SSC\_off}$	PCIe Gen 4 Common Clock jitter, SSC is off (jitter limit = 500 fs)	SSC disabled on both outputs		32.8	60	fs
$J_{PCIe4\text{-}cc\text{-}SSC\_on}$	PCIe Gen 4 Common Clock jitter, –0.5% ≤ SSC < 0% (jitter limit = 500 fs)	SSC enabled on both outputs		55.4	110	fs
$J_{PCIe4\text{-}SRNS}$	PCIe Gen 4 SRNS jitter	SSC disabled on both outputs		35.9	68	fs
$J_{PCIe4\text{-}SRIS}$	PCIe Gen 4 SRIS jitter, –0.3% ≤ SSC < 0%	SSC enabled on both outputs		86.4	164	fs
$J_{PCIe5\text{-}cc\text{-}SSC\_off}$	PCIe Gen 5 Common Clock jitter, SSC is off (jitter limit = 150 fs)	SSC disabled on both outputs		11.1	26	fs
$J_{PCIe5\text{-}cc\text{-}SSC\_on}$	PCIe Gen 5 Common Clock jitter, –0.5% ≤ SSC < 0% (jitter limit = 150 fs)	SSC enabled on both outputs		20.3	47	fs
$J_{PCIe5\text{-}SRNS}$	PCIe Gen 5 SRNS jitter	SSC disabled on both outputs		12.7	30	fs
$J_{PCIe5\text{-}SRIS}$	PCIe Gen 5 SRIS jitter, –0.3% ≤ SSC < 0%	SSC enabled on both outputs		22.9	51	fs
$J_{PCIe6\text{-}cc\text{-}SSC\_off}$	PCIe Gen 6 Common Clock jitter, SSC is off (jitter limit = 100 fs)	SSC disabled on both outputs		7.9	16	fs
$J_{PCIe6\text{-}cc\text{-}SSC\_on}$	PCIe Gen 6 Common Clock jitter, –0.5% ≤ SSC < 0% (jitter limit = 100 fs)	SSC enabled on both outputs		13.5	28	fs
$J_{PCIe6\text{-}SRNS}$	PCIe Gen 6 SRNS jitter	SSC disabled on both outputs		11.2	24	fs
$J_{PCIe6\text{-}SRIS}$	PCIe Gen 6 SRIS jitter, –0.3% ≤ SSC < 0%	SSC enabled on both outputs		17.7	36	fs
RJ_{RMS}	12 kHz to 20 MHz RMS jitter	f_{out} = 100 MHz		144	200	fs
RJ_{RMS}	12 kHz to 20 MHz RMS jitter	f_{out} = 125 MHz		117.6	150	fs
RJ_{RMS}	12 kHz to 20 MHz RMS jitter	f_{out} = 156.25 MHz		108.5	125	fs
RJ_{RMS}	12 kHz to 20 MHz RMS jitter	f_{out} = 212.5 MHz		107.3	150	fs
RJ_{RMS}	12 kHz to 20 MHz RMS jitter	f_{out} = 312.5 MHz		91.9	115	fs
TIMING CHARACTERISTICS						
$t_{startup}$	Start-up time	V_{DD} = 2.5 V or 3.3 V. Time elapsed from all V_{DD} pins reach 2.1 V until first output clock rising edge. Output clock is always within specification			1	ms
		V_{DD} = 1.8 V. Time elapsed from all V_{DD} pins reach 1.6 V until first output clock rising edge. Output clock is always within specification			1.5	ms
t_{OE}	Output enable time.	After CLOCK_READY status is '1', time elapsed between OE assertion and first output clock rising edge. Output is not tristated when disabled.			7	output clock cycles
t_{OD}	Output disable time.	Time elapsed between OE deassertion and last output clock falling edge.			7	output clock cycles
POWER CONSUMPTION CHARACTERISTICS						

ADVANCE INFORMATION

V_{DD} = V_{DDO} = 1.8 V, 2.5 V or 3.3 V ± 5%, T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Core supply current, not including output drivers	One FOD enabled, 100 MHz ≤ f_{FOD} ≤ 200 MHz		49.1	TBD	mA
		One FOD enabled, 200 MHz < f_{FOD} ≤ 400 MHz		52.7	TBD	mA
		Two FODs enabled, 100 MHz ≤ f_{FOD} ≤ 200 MHz		61.7	TBD	mA
		Two FODs enabled, 200 MHz < f_{FOD} ≤ 400 MHz		68.5	TBD	mA
I_{DDO}	Output supply current, per output channel	LP-HCSL. f_{out} ≤ 100 MHz		10.1	TBD	mA
		LP-HCSL. 100 MHz < f_{out} ≤ 200 MHz		13.2	TBD	mA
		LP-HCSL. 200 MHz < f_{out} ≤ 300 MHz		13.7	TBD	mA
		LP-HCSL. 300 MHz < f_{out} ≤ 400 MHz		14.4	TBD	mA
		LVDS. f_{out} ≤ 100 MHz		6	TBD	mA
		LVDS. 100 MHz < f_{out} ≤ 200 MHz		6.8	TBD	mA
		LVDS. 200 MHz < f_{out} ≤ 300 MHz		7.6	TBD	mA
		LVDS. 300 MHz < f_{out} ≤ 400 MHz		8.4	TBD	mA
		1.8 V LVCMOS. f_{out} = 50 MHz		4.2	TBD	mA
		1.8 V LVCMOS. f_{out} = 200 MHz		11.7	TBD	mA
		2.5 V LVCMOS. f_{out} = 50 MHz		5.6	TBD	mA
		2.5 V LVCMOS. f_{out} = 200 MHz		15.3	TBD	mA
		3.3 V LVCMOS. f_{out} = 50 MHz		6.8	TBD	mA
		3.3 V LVCMOS. f_{out} = 200 MHz		19.2	TBD	mA
I_{DDREF}	REFCLK supply current	1.8 V LVCMOS. f_{out} = 50 MHz		3.4	TBD	mA
		1.8 V LVCMOS. f_{out} = 200 MHz		9.5	TBD	mA
		2.5 V LVCMOS. f_{out} = 50 MHz		4.7	TBD	mA
		2.5 V LVCMOS. f_{out} = 200 MHz		12.8	TBD	mA
		3.3 V LVCMOS. f_{out} = 50 MHz		5.9	TBD	mA
		3.3 V LVCMOS. f_{out} = 200 MHz		16.6	TBD	mA
PSNR CHARACTERISTICS						
$PSNR_{LVCMOS}$	Power Supply Noise Rejection for LVCMOS outputs(4)	10 kHz		–76.7	–61.2	dBc
		50 kHz		–80.9	–60.9	dBc
		100 kHz		–81.8	–60	dBc
		500 kHz		–84.3	–64.9	dBc
		1 MHz		–97.6	–82.1	dBc
		5 MHz		–104.3	–83.1	dBc
		10 MHz		–108.7	–94.2	dBc
$PSNR_{LVDS}$	Power Supply Noise Rejection for LVDS outputs(4)	10 kHz		–79.5	–74.5	dBc
		50 kHz		–83.5	–77	dBc
		100 kHz		–83	–75.3	dBc
		500 kHz		–88.3	–83.1	dBc
		1 MHz		–123.4	–106.6	dBc
		5 MHz		–115	–92.3	dBc
		10 MHz		–123.7	–108.9	dBc

ADVANCE INFORMATION

V_{DD} = V_{DDO} = 1.8 V, 2.5 V or 3.3 V ± 5%, T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$PSNR_{LP-HCSL}$	Power Supply Noise Rejection for LP-HCSL outputs[4]	10 kHz		–80.1	–74.5	dBc
		50 kHz		–84.7	–76.7	dBc
		100 kHz		–84.6	–73.7	dBc
		500 kHz		–93.1	-82.9	dBc
		1 MHz		–124.6	–106.8	dBc
		5 MHz		–114.3	–92.9	dBc
		10 MHz		–123	–109.2	dBc
2-STATE LOGIC INPUT CHARACTERISTICS						
$V_{IH-Pin2}$	Input high voltage for Pin 2		0.7 × V_{DD}		V_{DD}D + 0.3	V
$V_{IL-Pin2}$	Input low voltage for Pin 2		GND – 0.3		0.3 × V_{DD}	V
$V_{IH-Pin1}$	Input high voltage for Pin 1		1.15		V_{DD} + 0.3	V
$V_{IL-Pin1}$	Input low voltage for Pin 1		–0.3		0.65	V
$V_{IH-Pin3,4}$	Input voltage high for Pin 3, 4		0.7 × V_{DD}		V_{DD} + 0.3	V
$V_{IL-Pin3,4}$	Input voltage low for Pin 3, 4		GND - 0.3		0.8	V
$V_{IH-Pin15}$	Input voltage high for Pin 15		0.65 × V_{DD}		V_{DD} + 0.3	V
$V_{IL-Pin15}$	Input voltage low for Pin 15		–0.3		0.4	V
$R_{int-up/down-Pin1,2}$	Internal pullup or pulldown resistor for Pin 1		50	75	105	kΩ
$R_{int-down-Pin3,4,15}$	Internal pulldown resistor for Pin 2, 3, 4, 15		620	880	1200	kΩ
$R_{ext-up/down-Pin1,2}$	Recommended external pullup or pulldown resistor for Pin 1, 2		0	1	10	kΩ
$R_{ext-up/down-Pin3,4,15}$	Recommended external pullup or pulldown resistor for Pin 3, 4, 15		0	10	60	kΩ
t_R/t_F	OE signal rise or fall time				10	ns
C_{in}	Input capacitance				3	pF
ENVIRONMENTAL TESTS						
Sinusoidal Vibration -4g	Frequency drift under sinusoidal vibration. 4g acceleration. x, y, z direction.	10 Hz		TBD		ppb/g
		20 Hz		TBD		ppb/g
		50 Hz		TBD		ppb/g
		100 Hz		TBD		ppb/g
		200 Hz		TBD		ppb/g
		500 Hz		TBD		ppb/g
		1 kHz		TBD		ppb/g
		2 kHz		TBD		ppb/g

ADVANCE INFORMATION

V_{DD} = V_{DDO} = 1.8 V, 2.5 V or 3.3 V ± 5%, T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Sinusoidal Vibration -10g	Frequency drift under sinusoidal vibration. 10g acceleration. x, y, z direction.	50 Hz		TBD		ppb/g
		100 Hz		TBD		ppb/g
		200 Hz		TBD		ppb/g
		500 Hz		TBD		ppb/g
		1 kHz		TBD		ppb/g
		2 kHz		TBD		ppb/g

(1) PCIe test load, 15 dB loss at 4 GHz, f_{out} = 100 MHz, Z_{diff} = 100 Ω
(2) Tested with 10 kΩ external pullup or pulldown resistor
(3) REFCLK can be /2, /4, /8 from either FOD0 or FOD1. Both FODs support 100 to 400 MHz.
(4) All power supply pins are tied together. 0.1 µF capacitor placed close to each power supply pin. Apply 50 mVpp ripple and measure the spur level at the clock output

ADVANCE INFORMATION

5.6 I2C Interface Specification

All timing requirements referred to $V_{IH\text{-}min}$ and $V_{IL\text{-}max}$. Chip V_{DD} = I^2C V_{DD}.

PARAMETER		TEST CONDITIONS	STANDARD MODE		FAST MODE		UNIT
			MIN	MAX	MIN	MAX	
V_{IL}	Input low voltage		–0.3	0.3 × V_{DD}	–0.3	0.3 × V_{DD}	V
V_{IH}	Input high voltage		0.7 × V_{DD}	V_{DD} + 0.3	0.7 × V_{DD}	V_{DD} + 0.3	V
V_{hys}	Hysteresis of Schmitt trigger input				0.05 × V_{DD}		V
V_{OL1}	Low level output voltage 1	At 3 mA sink current. V_{DD} > 2 V	0	0.4	0	0.4	V
V_{OL2}	Low level output voltage 2	At 2 mA sink current. V_{DD} ≤ 2 V			0	0.2 x V_{DD}	V
I_{OL}	Low level output current	V_{OL} = 0.4 V	3		3		mA
		V_{OL} = 0.6 V			6		mA
t_{OF}	Output fall time from VIHmin to VILmax			250	20 × (V_{DD} / 5.5 V)	250	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filter				0	50	ns
I_i	Input current each I/O pin	0.1 × V_{DD} < V_{IN} < 0.9 × V_{DDmax}	–10	10	–10	10	µA
C_i	Capacitance for each I/O pin			10		10	pF
f_{SCL}	SCL clock frequency		0	100	0	400	kHz
$t_{HD\text{-}STA}$	Hold time (repeated) START condition	After this period, the first clock pulse is generated	4		0.6		µs
tlow	Low period of the SCL clock		4.7		1.3		µs
thigh	High period of the SCL clock		4		0.6		µs
$t_{SU\text{-}STA}$	Set-up time for a repeated START condition		4.7		0.6		µs
$t_{HD\text{-}DAT}$	Data hold time	I^2C bus devices	0		0		µs
$t_{SU\text{-}DAT}$	Data set-up time		0.25		0.1		µs
t_R	Rise time of both SDA and SCL signals			1000	20	300	ns
t_F	Fall time of both SDA and SCL signals			1000	20 × (V_{DD} / 5.5 V)	300	ns
$t_{SU\text{-}STO}$	Set-up time for STOP condition		4		0.6		µs

All timing requirements referred to V_{IH-min} and V_{IL-max}. Chip V_{DD} = I^2C V_{DD}.

PARAMETER		TEST CONDITIONS	STANDARD MODE		FAST MODE		UNIT
			MIN	MAX	MIN	MAX	
t_{BUF}	Bus free time between a STOP and START condition		4.7		1.3		µs
C_B	Capacitive load for each bus line			400		400	pF
t_{VD-DAT}	Data valid time			3.45		0.9	µs
t_{VD-ACK}	Data valid acknowledge time			3.45		0.9	µs
V_{NL}	Noise margin at the low level	For each connected device, including hysteresis	0.1 x V_{DD}		0.1 × V_{DD}		V
V_{NH}	Noise margin at the high level	For each connected device, including hysteresis	0.2 x V_{DD}		0.2 × V_{DD}		V

ADVANCE INFORMATION

6 Parameter Measurement Information

6.1 Output Format Configurations

This section describes the characterization test setup of each output format option in the LMK3H0102.

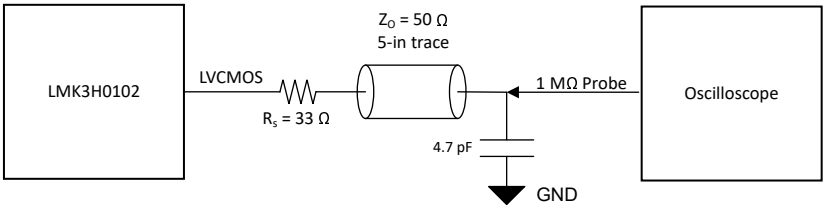

図 6-1. LVCMOS Output Configuration During Device Test

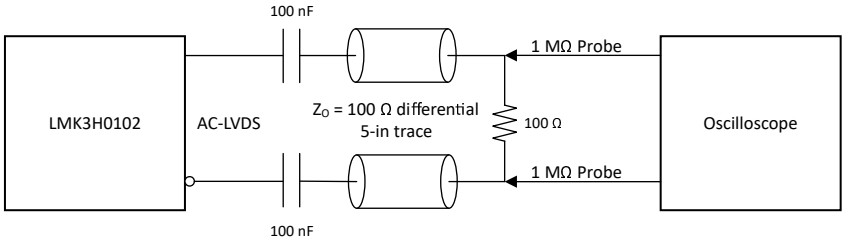

図 6-2. AC-LVDS Output Configuration During Device Test

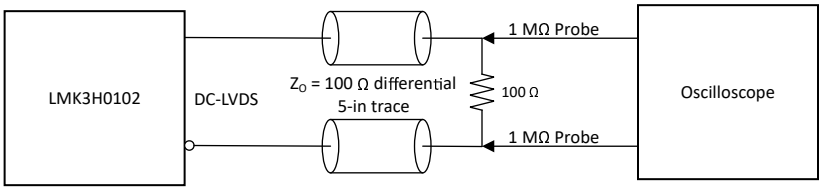

図 6-3. DC-LVDS Output Configuration During Device Test

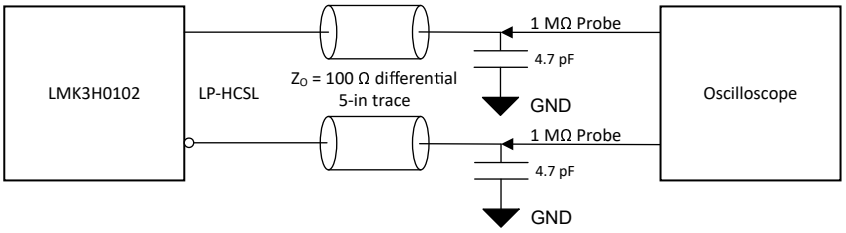

図 6-4. LP-HCSL Output Configuration During Non-PCIe Device Test

ADVANCE INFORMATION

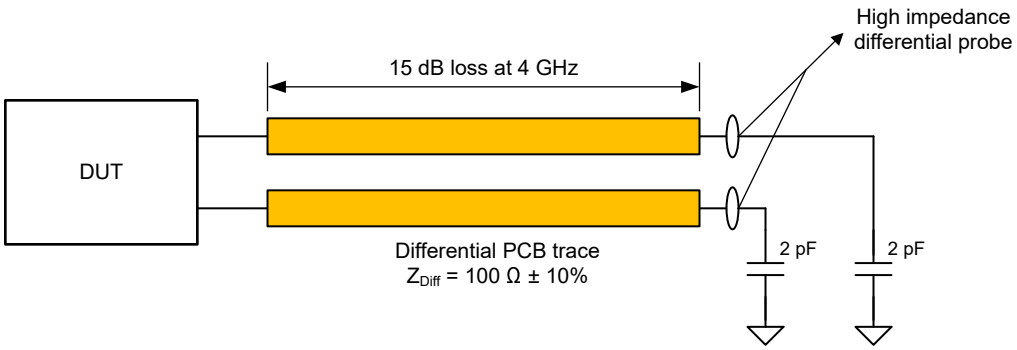

図 6-5. LP-HCSL Output Configuration During PCIe Device Test

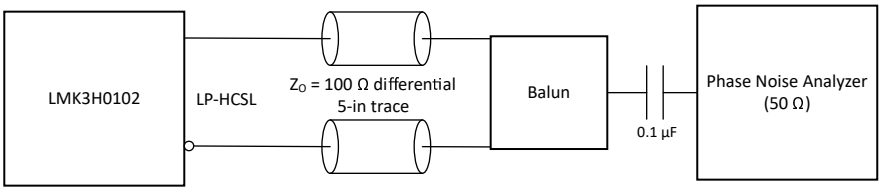

図 6-6. PCIe Test Configuration Using Phase Noise Analyzer

ADVANCE INFORMATION

7 Detailed Description

7.1 Overview

The LMK3H0102 is a dual-channel clock generator primarily used for PCIe Gen 1 to Gen 6 clock generation, either with or without Spread Spectrum Clocking (SSC). The device has an integrated Bulk Acoustic Wave (BAW) resonator and does not require any external crystal or clock reference. The device has four selectable pages of memory, referred to as OTP pages. The collection of these pages in memory is referred to as the EFUSE.

The default output configuration is two 100-MHz clocks, each with a 100-Ω LP-HCSL output format. The LMK3H0102 supports 100-Ω LP-HCSL, 85-Ω LP-HCSL, LVDS and 1.8-V, 2.5-V, or 3.3-V LVCMOS output formats, as well as programmable output frequencies up to 200 MHz for single-ended outputs and 400 MHz for differential outputs.

The LMK3H0102 supports two functional modes determined by the REF_CTRL pin at power-up: One-Time Programming (OTP) mode or I^2C mode.

1. In OTP mode, one out of four OTP pages is selected by pins OTP_SEL0 and OTP_SEL1. The default output frequency across all OTP pages is 100 MHz.
2. In I^2C mode, the LMK3H0102 is configured by modifying the active registers. If a configuration other than the default operation is desired, the registers must be written every time at start-up.

   When using a device with a blank EFUSE, the EFUSE can be permanently programmed through the I^2C.

Refer to *Pin Configuration and Functions* for the detailed descriptions of the device pins.

The LMK3H0102 has flexible SSC configurations, including:

1. SSC disabled on both outputs
2. SSC enabled on both outputs
3. SSC enabled on a single output

The SSC specifications and jitter performance are fully compliant to PCIe Gen 1 to Gen 6. Refer to *Spread-Spectrum Clocking* for SSC and jitter performance details.

ADVANCE INFORMATION

7.2 Functional Block Diagram

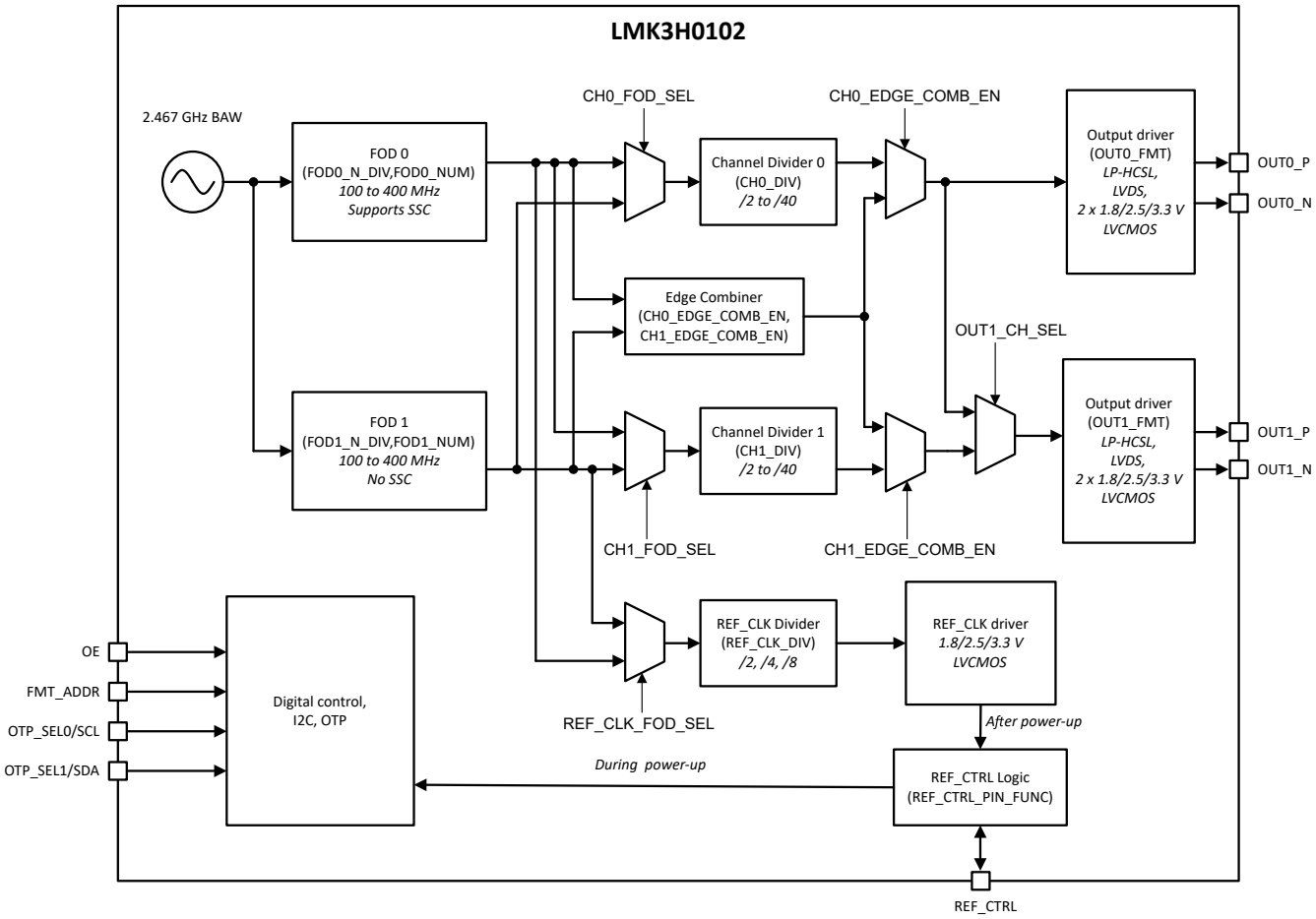

図 7-1. LMK3H0102 Functional Block Diagram

7.3 Feature Description

7.3.1 Device Block-Level Description

The LMK3H0102 is a reference-less clock generator with an integrated BAW oscillator. The BAW frequency, nominally 2467 MHz, is divided down by two fractional output dividers (FODs), each of which is capable of generating frequencies between 100 MHz and 400 MHz. Each FOD can be routed to one of two channel dividers, which divides the FOD frequency down to generate frequencies from 2.5 MHz to 200 MHz. For generating frequencies above 200 MHz, both FODs can be routed to the edge combiner, which combines the uses both FODs to make sure that the output clock maintains a 50% duty cycle. An additional LVCMOS clock, with a voltage corresponding with VDD, can be configured using the REF_CTRL pin. By default, this pin is configured as a CLK_READY signal, which is high when the output clocks are active.

7.3.2 Device Configuration Control

図 7-2 shows the relationships between device states, the configuration pins, device initialization, and device operational modes. OTP mode is entered when the REF_CTRL pin is pulled high at start-up. I^2C mode is entered when the REF_CTRL pin is pulled low at start-up. In OTP mode, the state of the OTP_SEL0/SCL and OTP_SEL1/SDA pins determines the OTP page that is loaded into the active registers. In I^2C mode, the state of the FMT_ADDR pin determines the I^2C address of the device, with the OTP_SEL0/SCL and OTP_SEL1/SDA pins re-purposed as I^2C clock and data pins, respectively. In I^2C mode, the host can update the active device registers, and can program a desired configuration into the EFUSE. The device is one-time programmable, meaning that the register settings can be stored into the internal EFUSE of the device a single time.

ADVANCE INFORMATION

The device can be transitioned from OTP to I^2C mode, or vice versa, by changing the state of the REF_CTRL pin, then triggering a device power cycle by pulling VDD low, then high again. Alternatively, instead of toggling the VDD pin, the PDN bit (R10[1]) can be set to '1' then '0', or the DEV_IDLE_STATE_SEL bit (R10[4]) can be set to '1' then '0'. 表 7-1 lists the functionality of the configuration pins during OTP and I^2C modes.

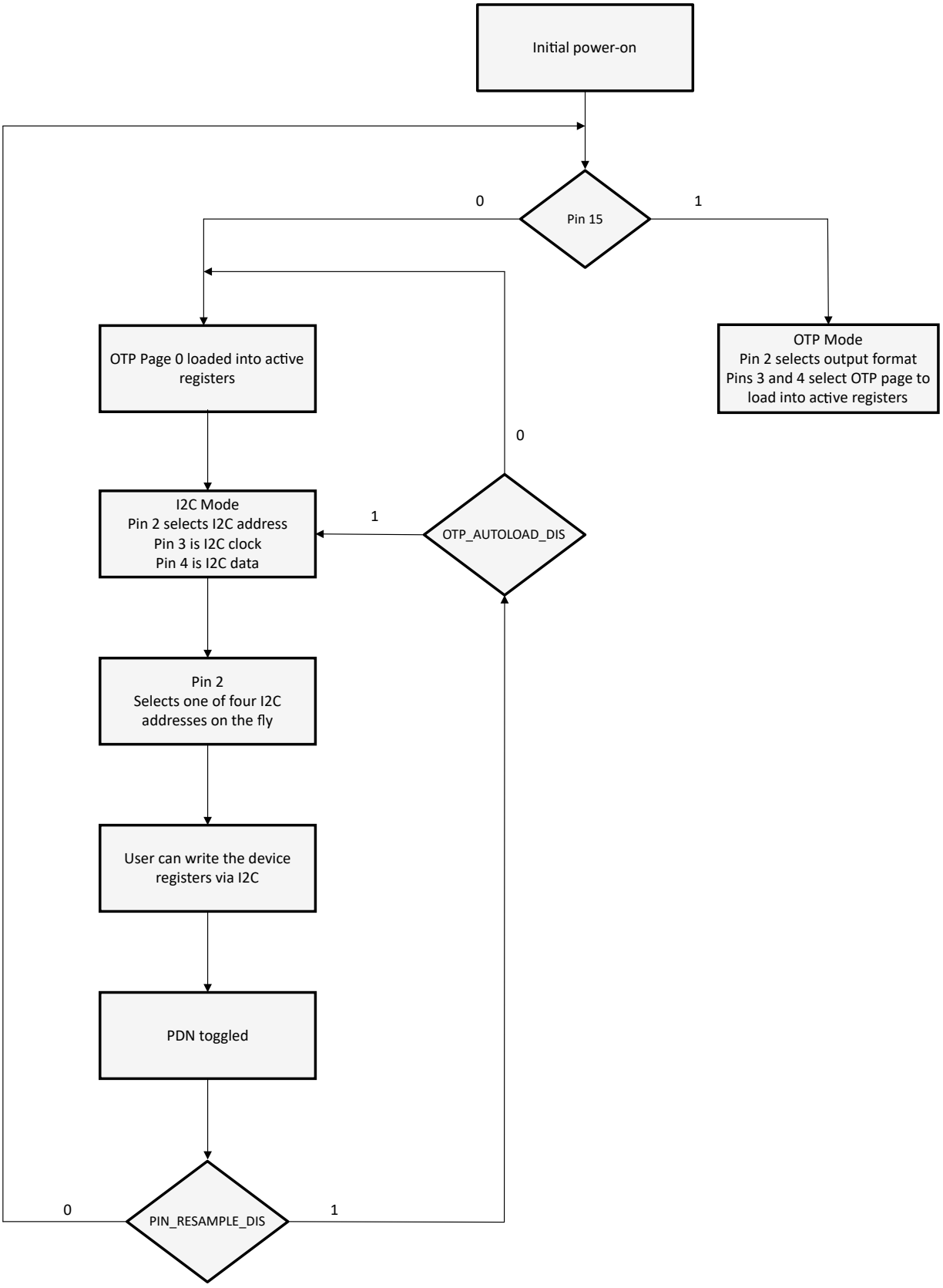

図 7-2. LMK3H0102 Simplified Programming Flow

ADVANCE INFORMATION

表 7-1. Pin Configuration for I2C and OTP Mode

PIN NAME	I²C MODE		OTP MODE	
	Function	Pin States	Function	Pin States
FMT_ADDR	Output Buffer Selection	2	I2C Address Selection	4
OTP_SEL0/SCL	OTP Page Selection	2	I2C Clock Pin	2
OTP_SEL1/SDA	OTP Page Selection	2	I2C Data Pin	2

In I²C Mode, the device default registers are from the contents of OTP Page 0. In OTP mode, these values come from one of the four OTP pages, selectable based on the state of the OTP_SELx pins on start-up. 図 7-3 shows interface and control blocks within the LMK3H0102, with the arrows referring to read and write access from the different embedded memories.

ADVANCE INFORMATION

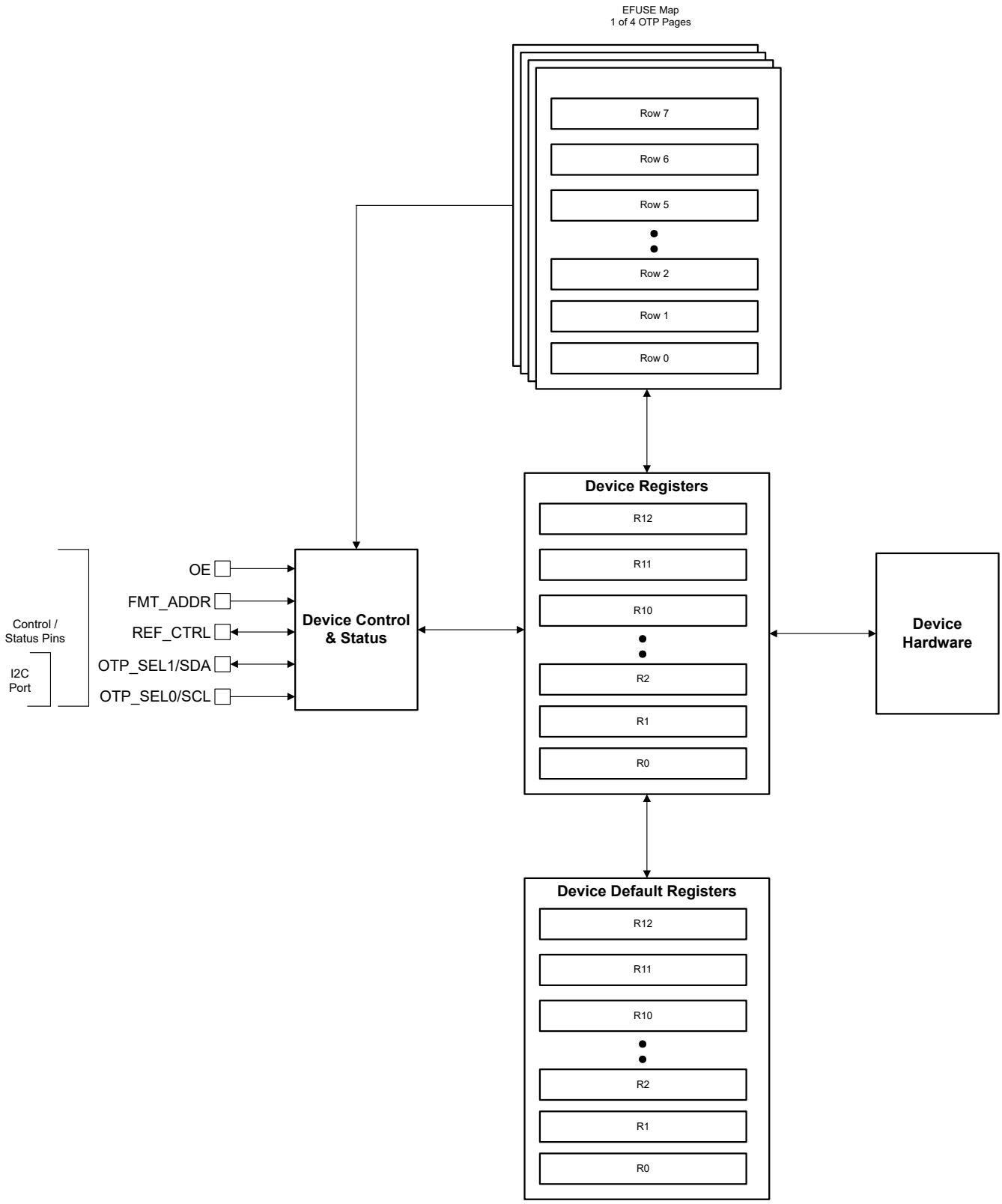

図 7-3. LMK3H0102 Interface and Control Blocks

ADVANCE INFORMATION

7.3.3 OTP Mode

In this mode, the configuration pins allow for selection of one of four one-time programmable (OTP) pages, as well as output format selection. I²C is not enabled in this mode, as the I²C pins are repurposed for OTP page selection. 表 7-2 shows the OTP page selected based on the state of the OTP_SEL0 and OTP_SEL1 pins. In OTP mode, the FMT_ADDR pin is ignored by default. This is overridden if R9[8] = 1 is burnt into the OTP in the configuration. Otherwise, the output format is determined by 表 7-3.

表 7-2. OTP Page Selection in OTP Mode

OTP_SEL1 Pin	OTP_SEL0 Pin	OTP Page
Low	Low	0
Low	High	1
High	Low	2
High	High	3

表 7-3. FMT_ADDR Output Format Options

R9[8]	FMT_ADDR Pin	Output Format
0	X	Set by R6[2:0] / R7[4:2]
1	GND	LP-HCSL 100 Ω Termination
1	VDD	LP-HCSL 85 Ω Termination

The EFUSE of the devices is permanently programmed and has R0[0] = 1. If a new configuration is desired, the configuration must be loaded through I²C on each start-up.

The following fields can be unique between the four OTP pages. All other register settings are shared between the OTP pages:

- SSC_EN: Enable or disable SSC
- OE_0: Enable or disable OUT0
- OE_1: Enable or disable OUT1
- OP_TYPE_CH0: OUT0 output format type, see *Output Format Types*.
- OP_TYPE_CH1: OUT1 output format type, see *Output Format Types*.
- SSC_SETTING: SSC modulation type, see *Spread Spectrum Clocking*.

7.3.4 I²C Mode

In this mode, I²C is enabled and the SCA and SDL pins function as the I²C clock and I²C data pins, respectively. 表 7-4 shows the four default I²C addresses selectable by the FMT_ADDR pin. The 0xD0, 0xD2, 0xD4, and 0xD8 addresses are with the R/W bit included. The 5 MSBs of the I²C address are set in R12[14:8].

If R12[15] = 1, then the FMT_ADDR pin is ignored, and the I²C address is solely determined by R12[14:8].

表 7-4. I²C Address Selection

REF_CTRL PIN	FMT_ADDR PIN	I²C ADDRESS
High	X	N/A (I2C disabled)
Low	0	0x68 / 0xD0
Low	1	0x69 / 0xD2
Low	Tied to SDA	0x6A / 0xD4
Low	Tied to SCL	0x6B / 0xD8

When changing the registers of the device, first set PDN = 1 (R10[1] = 1), write to the device registers, then set PDN = 0 (R10[1] = 0).図 7-4 shows this process.

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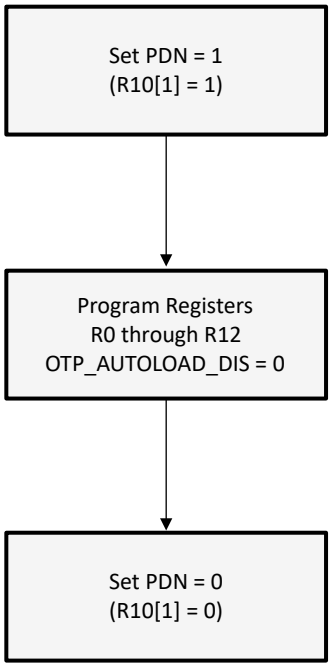

図 7-4. LMK3H0102 Programming Sequence

7.4 Device Functional Modes

7.4.1 Fail-Safe Inputs

The LMK3H0102 is designed to support fail-safe input operation, with the exception of the REF_CTRL pin. This feature allows the user to drive the device inputs before VDD is applied without damaging the device. Refer to *セクション 5.1*for more information on the maximum input voltages supported by the device.

7.4.2 Fractional Output Dividers

The LMK3H0102 contains two fractional output dividers. If all outputs are able to be generated by a single FOD, TI recommends disabling FOD1 to conserve power and improve performance. If no output channels select FOD1, then FOD1 is disabled.

7.4.2.1 FOD Operation

The internal BAW resonator is divided down by one or two Fractional Output Dividers (FODs). FOD 0 has an SSC generator and FOD 1 does not have an SSC generator. If both OUT0 and OUT1 must be SSC clocks, the two clocks must be sourced by FOD 0. If one SSC clock and one non-SSC clock are required at the same time, then FOD0 is enabled for the SSC clock and FOD1 is enabled for the non-SSC clock. If neither output clock requires SSC, then either FOD can be used.

注

TI recommends that FOD0 be used as the default FOD if only one FOD is needed for an application. If both FODs are in use, TI recommends using FOD0 with OUT0 and FOD1 with OUT1.

The maximum frequency that can be generated at the clock outputs by a single FOD is 200 MHz, as the minimum channel divider value is a divide by two. To generate a greater than 200 MHz output, the edge combiner is used, bypassing the channel dividers. This requires that both FODs are enabled and have the same integer divider and fractional numerator values, and the same gain calibration values. When one of the outputs exceeds 200 MHz, the other output can only select the shared FOD frequency divided by one of the channel divider values, or be the FOD frequency. Below 200 MHz, the two FODs can be configured independently so that

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OUT0 and OUT1 can have different frequencies. TI recommends sourcing from a single FOD whenever possible to make sure that OUT0 and OUT1 have a deterministic phase relationship.

The FODs in the LMK3H0102 can be configured to accommodate various output frequencies through I2C programming, or in the absence of programming, the one-time programmed (OTP) settings. The FODs can be configured by setting the integer (FODx_N_DIV) and fractional (FODx_NUM) divide values. 表 7-5 shows the register locations for these fields for each FOD.

表 7-5. FOD Integer and Numerator Divide Locations

Field	Register
FOD0_N_DIV	R0[9:3]
FOD0_NUM[23:16]	R1[15:8]
FOD0_NUM[15:0]	R2[15:0]
FOD1_N_DIV	R3[15:9]
FOD1_NUM[23:16]	R6[12:5]
FOD1_NUM[15:0]	R8[15:0]

An example of how to set the integer and numerator divide values is shown in 式 1 and 式 2.

$$FODx\_N\_DIV = floor(F_{BAW}/F_{FOD}) \quad (1)$$

where:

- FODx_N_DIV: Integer portion of the FOD divide value (7 bits, 6 to 24)
- F_{BAW}: BAW frequency, 2467 MHz plus offset, described in further detail below
- F_{FOD}: Desired FOD frequency (100 MHz to 400 MHz)

$$FODx\_NUM = int(((F_{BAW}/F_{FOD}) - FODx\_N\_DIV) \times 2^{24}) \quad (2)$$

where FODx_NUM is the fractional portion of the FOD divide value (24 bits, that is 0 to 16777215).

The output frequency (F_{OUT}) is related to the FOD frequency as given in 式 3, or is equal to the FOD frequency when the edge combiner is enabled. OUTDIV can be 2, 4, 6, 8, 10, 20, or 40.

$$F_{OUT} = F_{FOD}/OUTDIV \quad (3)$$

Use 式 4 to calculate the actual value of the BAW frequency for a device. Users can find the value of BAWFREQ_OFFSET_FIXEDLUT by reading R238, which is a signed 16-bit value.

$$F_{BAW} = 2467\ MHz \times (1 + (BAWFREQ\_OFFSET\_FIXEDLUT \times 128E\text{-}9)) \quad (4)$$

7.4.2.2 Edge Combiner

Enable the edge combiner to generate output frequencies greater than 200 MHz. To use the edge combiner, both FODs must operate at the same exact frequency (that is, the divide values must match). Using the edge combiner bypasses the channel dividers, meaning that the output of both channels comes directly from the edge combiner. When the edge combiner is enabled, FOD0 and FOD1 become 180 degrees out of phase. The edge combiner functions similarly to an SR flip flop, where the rising edge of FOD0 is the "Set" signal, and the rising edge of FOD1 is the "Reset" signal. SSC on FOD0 is not supported when using the edge combiner. Either of the FODs can still generate the LVCMOS REF_CLK output.

For edge combiner operation, the following conditions must be true:

- R0[9:3] and R3[15:9] (integer portion of the FODs) must match.
- R1[15:8] and R6[12:5] (MSB of the fractional numerators) must match.
- R2[15:0] and R8[15:0] (LSBs of the fractional denominators) must match.
- R3[3] or R3[7] (dual FOD enable) must be set to '1'.

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- The gain calibration codes for both FODs must be averaged. For example, if DTC1_GAIN_RT = 200, and DTC2_GAIN_RT = 220, then both of these fields must be written to 210. See R146, R147, and R148 for more information.
- If the edge combiner is used for OUT1 **only**, R3[4] (Channel Divider 0 input selection) must **always** be set to '0' (FOD0), regardless of the disable state of OUT0.

7.4.2.3 Digital State Machine

The digital state machine of the LMK3H0102 has a clock that originates from FOD0. This clock must run as close to 45 MHz as is allowed by the frequency of FOD0. The divider value used to set this clock is equal to the value stored in R0[9:3]. As an example, if the frequency of FOD0 is 200 MHz, then R0[9:3] must be set to 0x04, as 200 MHz divided by 4 is 50 MHz.

7.4.2.4 Spread-Spectrum Clocking

FOD0 supports spread-spectrum clocking (SSC). SSC can be used to reduce peak radiated emissions by modulating the output frequency. When SSC is enabled (R4[0] = 1), any outputs that are sourced from FOD0 have SSC. Both down-spread modulation (R4[1] = 0) and center-spread modulation (R4[1] = 1) are available. The LMK3H0102 has four built-in down-spread SSC options, as well as a custom SSC option. 表 7-6 details the register settings for the pre-configured SSC options. If Custom SSC is selected, then Registers R4 and R5 must be configured to set the modulation depth. If the edge combiner is used, then spread-spectrum clocking must be disabled.

表 7-6. Predefined SSC Configurations

R9[11:9]	Down-spread SSC Depth
0x0	Custom, based on R4 and R5
0x1	–0.10%
0x2	–0.25%
0x3	–0.30%
0x4	–0.50%
All other values	Reserved

Use 式 5 and 式 6 to determine the SSC_STEPS (R4[14:2]) register settings, and use 式 7 to determine the SSC_STEP_SIZE (R5) settings.

$$\text{Down-spread: SSC\_STEPS} = (F_{FOD0}/F_{MOD})/2 \quad (5)$$

$$\text{Center-spread: SSC\_STEPS} = (F_{FOD0}/F_{MOD})/4 \quad (6)$$

where:

- F_{FOD0}: FOD0 Frequency
- F_{MOD}: Modulation frequency, fixed at 31.5 kHz

$$SSC\_STEP\_SIZE = (F\_BAW/F\_FOD0 * (1/(1 - SSC\_DEPTH) - 1))/(SSC\_STEPS) * DEN \quad (7)$$

where:

- SSC_STEP_SIZE: Numerator increment value per step for SSC
- F_{BAW}: BAW frequency, 2467 MHz
- SSC_DEPTH: Modulation depth, expressed as a positive value. If –0.5% depth is used, this value is 0.005
- SSC_STEPS: Result from 式 5 for down-spread or 式 6 for center-spread
- DEN: Fractional denominator, 2^{24}

If using a mix of SSC on one output and no SSC on a different output, there can be crosstalk between the two outputs. Contact TI to request measurement data for a specific configuration when configuring SSC on only a single output.

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7.4.2.5 Integer Boundary Spurs

When the decimal portion of the FOD divide value is near an integer boundary, integer boundary spurs can occur. In general, this "integer boundary" is when the decimal portion is between 0.9 and 1, or 0 and 0.1. For example, if the BAW frequency is 2467 MHz, and an output of 122.88 MHz, then the FOD must run at 245.76 MHz. 2467 MHz divided by 245.76 MHz is approximately 10.038. The decimal portion of the divide value is 0.038, which falls between 0 and 0.1, and thus means that generating a 122.88 MHz output can result in spurs in the 12 kHz to 20 MHz band on the output clock. In some cases, proper frequency planning can account for this by increasing the FOD frequency and the channel divider value. For any concerns about integer boundary spurs for a specific frequency plan, contact TI.

7.4.3 Output Behavior

7.4.3.1 Output Format Selection

This device supports LP-HCSL (both 85-Ω and 100-Ω internal termination), LVDS, and LVCMOS. For LVCMOS outputs,VDDO can be 1.8 V, 2.5 V or 3.3 V if the VDD is 3.3 V. Otherwise, the VDDO must be the same voltage as VDD.

表 7-7. Output Format via Registers

R6[2:0] / R7[4:2]	Description
0x0	LP-HCSL 100 Ω Termination (default)
0x1	LP-HCSL 85 Ω Termination
0x2	AC-coupled LVDS
0x3	DC-coupled LVDS
0x4	LVCMOS enabled on OUTx_P LVCMOS disabled on OUTx_N
0x5	LVCMOS disabled on OUTx_P LVCMOS enabled on OUTx_N
0x6	LVCMOS enabled on OUTx_P LVCMOS enabled on OUTx_N 180 degrees out of phase (1)
0x7	LVCMOS enabled on OUTx_P LVCMOS enabled on OUTx_N OUTx_P and OUTx_N in phase

(1) For best output performance, TI recommends using 180 degree out of phase LVCMOS if both OUTx_P and OUTx_N traces are required.

7.4.3.1.1 Output Format Types

図 7-5 through 図 7-8 display how to connect the LMK3H0102 outputs based on the output format selected.

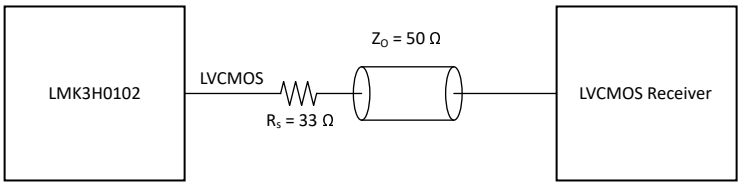

図 7-5. Interfacing LMK3H0102 LVCMOS Output With an LVCMOS Receiver

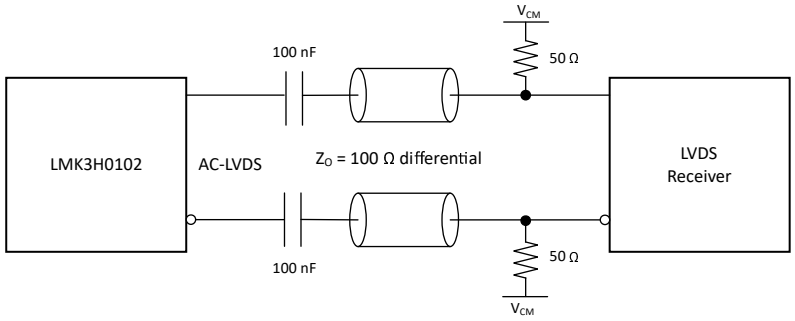

図 7-6. Interfacing LMK3H0102 LVCMOS Output With an AC-LVDS Receiver

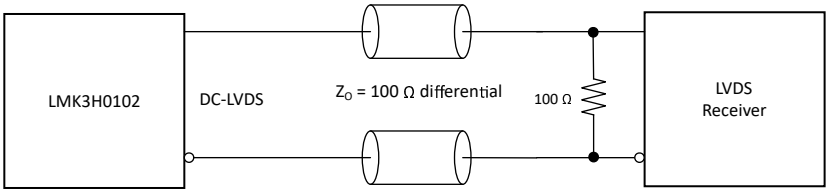

図 7-7. Interfacing LMK3H0102 LVCMOS Output With a DC-LVDS Receiver

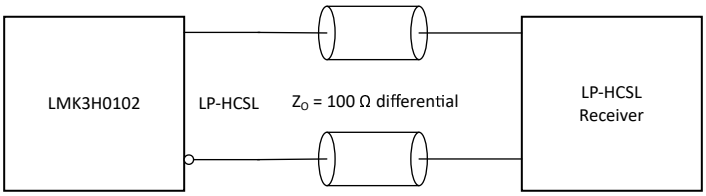

図 7-8. Interfacing LMK3H0102 LVCMOS Output With an LP-HCSL Receiver

7.4.3.1.1.1 LP-HCSL Termination

For LP-HCSL outputs, the LMK3H0102 uses internal 50-Ω termination resistors for the termination to GND. External termination resistors are not required.

7.4.3.2 Output Slew Rate Control

For all LVDS and LP-HCSL outputs, the slew rate can be configured. R6[4:3] and R7[6:5] can be used to slow down output slew rate to reduce EMI for OUT0 and OUT1, respectively. 表 7-8 shows the slew rate options available.

表 7-8. Slew Rate Settings

OUT0: R6[4:3] OUT1: R7[6:5]	Slew Rate
0x0 (default)	Between 2.3 and 3.4 V/ns
0x1	Between 2.0 and 3.0 V/ns
0x2	Between 1.7 and 2.7 V/ns
0x3	Between 1.4 and 2.5 V/ns

7.4.3.3 REF_CTRL Operation

At start-up, the REF_CTRL pin selects I^2C mode when low, and OTP mode when high. After start-up, REF_CTRL can be programmed to output an LVCMOS REF_CLK, which is derived from either FOD0 or FOD1 followed by an integer divider (/2, /4, /8). Alternatively, this pin can be disabled, or function as a "clock ready" signal. 表 7-9 shows these options.

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表 7-9. REF_CTRL Function after Startup

R7[14:13]	REF_CTRL Function
0x0	Disabled, forced low
0x1	Disabled, tri-state
0x2	REF_CLK LVCMOS output
0x3 (default)	CLK_READY output

7.4.4 Output Enable

7.4.4.1 Output Enable Control

This device supports synchronous Output Enable (OE). Synchronous OE means there is no glitch on the outputs when OE signal is asserted or deasserted.

The following table shows the enabling and disabling outputs through pin configuration and I^2C. Note that the OE pin must be low **and** OE bit must be "1" for the output to be active. In both I2C mode default and OTP mode, software OE bits are "1" for both outputs. The output enable bits are R7[1] for OUT0, and R7[8] for OUT1.

表 7-10. OE Functionality

OE pin	OE pin polarity	Software Output Enable OUT0: R7[1] OUT1: R7[8]	OUTx
High	Active low (default)	0	Off
High	Active low	1	Off
Low	Active low	0	Off
Low	Active low	1	Running
High	Active high	0	Off
High	Active high	1	Running
Low	Active high	0	Off
Low	Active high	1	Off

7.4.4.2 Output Enable Polarity

OE pin polarity is programmable and is active low by default. When the OE pin is active low, the internal pulldown resistor is automatically enabled, and the internal pullup resistor is disabled. When the OE pin is active high, the internal pullup resistor is automatically enabled, and the internal pulldown resistor is disabled. By default, clock outputs are always enabled when the OE pin is floating. The OE pin polarity is set by R7[0] - '1' for active-low (default), or '0' for active-high.

7.4.4.3 Output Disable Behavior

When OE is deasserted, the output can be either forced low or tri-state, determined by R3[5] for OUT0 and R3[6] for OUT1. The output is low for a '0', or tri-state for a '1'.

7.4.5 Device Default Settings

表 7-11 summarizes the default settings of the LMK3H0102 at start-up for the four OTP pages. In I^2C mode, the Page 0 settings are loaded. For a full list of every default register setting, see *Device Registers*.

表 7-11. LMK3H0102 Start-up Settings

Parameter	OTP Page 0	OTP Page 1	OTP Page 2	OTP Page 3
OUT0 Frequency	100 MHz	100 MHz	100 MHz	100 MHz
OUT0 Output Format	100-Ω LP-HCSL	100-Ω LP-HCSL	100-Ω LP-HCSL	100-Ω LP-HCSL
OUT0 Enable	Enable	Enable	Enable	Enable
OUT0 Slew Rate	2.3 to 3.4 V/ns	2.3 to 3.4 V/ns	2.3 to 3.4 V/ns	2.3 to 3.4 V/ns

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表 7-11. LMK3H0102 Start-up Settings (続き)

Parameter	OTP Page 0	OTP Page 1	OTP Page 2	OTP Page 3
OUT0 Amplitude	755 mV (typical)	755 mV (typical)	755 mV (typical)	755 mV (typical)
OUT0 Disable Behavior	GND	GND	GND	GND
OUT1 Frequency	100 MHz	100 MHz	100 MHz	100 MHz
OUT1 Output Format	100-Ω LP-HCSL	100-Ω LP-HCSL	100-Ω LP-HCSL	100-Ω LP-HCSL
OUT1 Enable	Enable	Enable	Enable	Enable
OUT1 Slew Rate	2.3 to 3.4 V/ns	2.3 to 3.4 V/ns	2.3 to 3.4 V/ns	2.3 to 3.4 V/ns
OUT1 Amplitude	755 mV (typical)	755 mV (typical)	755 mV (typical)	755 mV (typical)
OUT1 Disable Behavior	GND	GND	GND	GND
REF_CTRL Behavior	CLK_READY	CLK_READY	CLK_READY	CLK_READY
FOD0 Frequency	200 MHz	200 MHz	200 MHz	200 MHz
FOD1 Frequency	200 MHz	200 MHz	200 MHz	200 MHz
SSC Enable	Disable	Disable	Disable	Disable
SSC Modulation Type	Down-spread	Down-spread	Down-spread	Down-spread
SSC Modulation Depth	0%	-0.1%	-0.3%	-0.5%

7.5 Programming

The host (DSP, Microcontroller, FPGA, and so forth) configures and monitors the LMK3H0102 through the I^{2}C port. The host reads and writes to a collection of control bits called the register map. The device blocks can be controlled and monitored through a specific grouping of bits located within the register space. In the absence of the host, the LMK3H0102 can be configured to operate in OTP mode from one of four of the on-chip OTP pages, stored in the internal EFUSE, depending on the state of REF_CTRL and OTP_SELx pins. The EFUSE is one-time programmed by TI, and is not rewritable. This means that the starting registers cannot be changed, only the I^{2}C configuration can be changed. Within the device registers, there are certain bits that have read/write access. Other bits are read-only (an attempt to write to a read only bit does not change the state of the bit). Certain device registers and bits are reserved meaning that the fields must not be changed from the default reset state.

7.5.1 I^{2}C Serial Interface

The I^{2}C port on the LMK3H0102 works as a peripheral device and supports both the 100-kHz standard mode and 400-kHz fast-mode operations. Fast mode imposes a glitch tolerance requirement on the control signals. Therefore, the input receivers ignore pulses of less than 50-ns duration. The I^{2}C timing requirements are provided in the *I2C Interface Specification*. 図 7-9 shows the timing diagram.

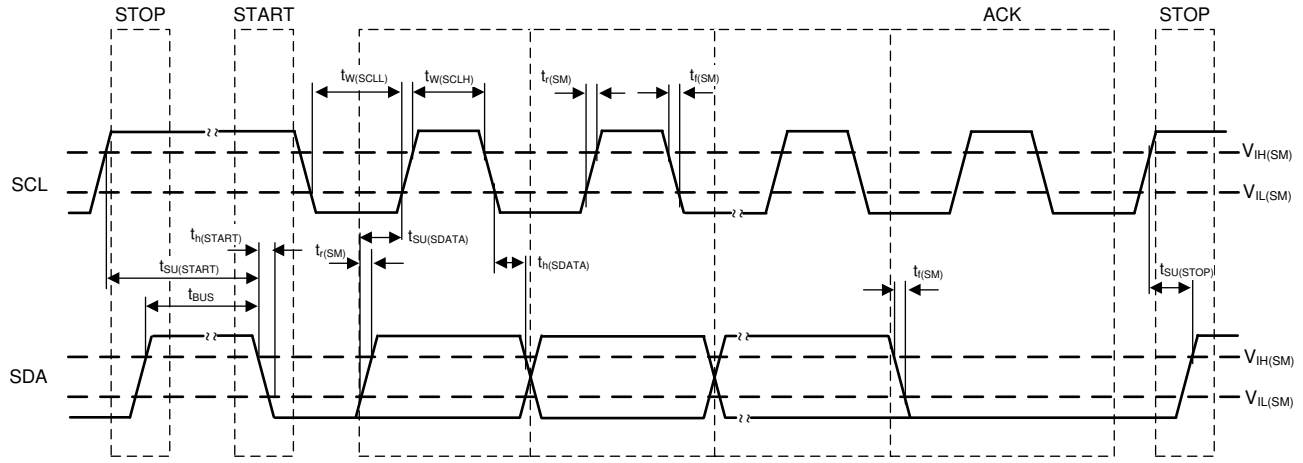

図 7-9. I^{2}C Timing Diagram

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The LMK3H0102 is accessed through a 7-bit peripheral address transmitted as part of an I^2C packet. Only the device with a matching peripheral address responds to subsequent I^2C commands. In I^2C mode, the LMK3H0102 allows up to four unique peripheral devices to occupy the I2C bus based on the pin strapping of FMT_ADDR (tied to VDD, GND, SDA, or SCL). The device peripheral address is 11010xx (the two LSBs are determined by the FMT_ADDR pin).

During the data transfer through the I^2C interface, one clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can change only when the clock signal on the SCL line is low. The start data transfer condition is characterized by a high-to-low transition on the SDA line while SCL is high. The stop data transfer condition is characterized by a low-to-high transition on the SDA line while SCL is high. The start and stop conditions are always initiated by the controller. Every byte on the SDA line must be eight bits long. Each byte must be followed by an acknowledge bit and bytes are sent MSB first. The LMK3H0102 has an 8-bit register address, followed by a 16-bit data word.

The acknowledge bit (A) or non-acknowledge bit (A') is the 9th bit attached to any 8-bit data byte and is always generated by the receiver to inform the transmitter that the byte has been received (when A = 0) or not (when A' = 0). A = 0 is done by pulling the SDA line low during the 9th clock pulse and A' = 0 is done by leaving the SDA line high during the 9th clock pulse.

The I^2C controller initiates the data transfer by asserting a start condition which initiates a response from all peripheral devices connected to the serial bus. Based on the 8-bit address byte sent by the controller over the SDA line (consisting of the 7-bit peripheral address (MSB first) and an R/W' bit), the device whose address corresponds to the transmitted address responds by sending an acknowledge bit. All other devices on the bus remain idle while the selected device waits for data transfer with the controller.

After the data transfer occurs, stop conditions are established. In write mode, the controller asserts a stop condition to end data transfer during the 10th clock pulse following the acknowledge bit for the last data byte from the peripheral. In read mode, the controller receives the last data byte from the peripheral but does not pull SDA low during the 9th clock pulse. This is known as a non-acknowledge bit. By receiving the non-acknowledge bit, the peripheral knows the data transfer is finished and enters the idle mode. The controller then takes the data line low during the low period before the 10th clock pulse, and high during the 10th clock pulse to assert a stop condition. 図 7-10 shows a generic I^2C transaction. 図 7-11 and 図 7-12 show the sequence for block writes and block reads using the LMK3H0102, respectively.

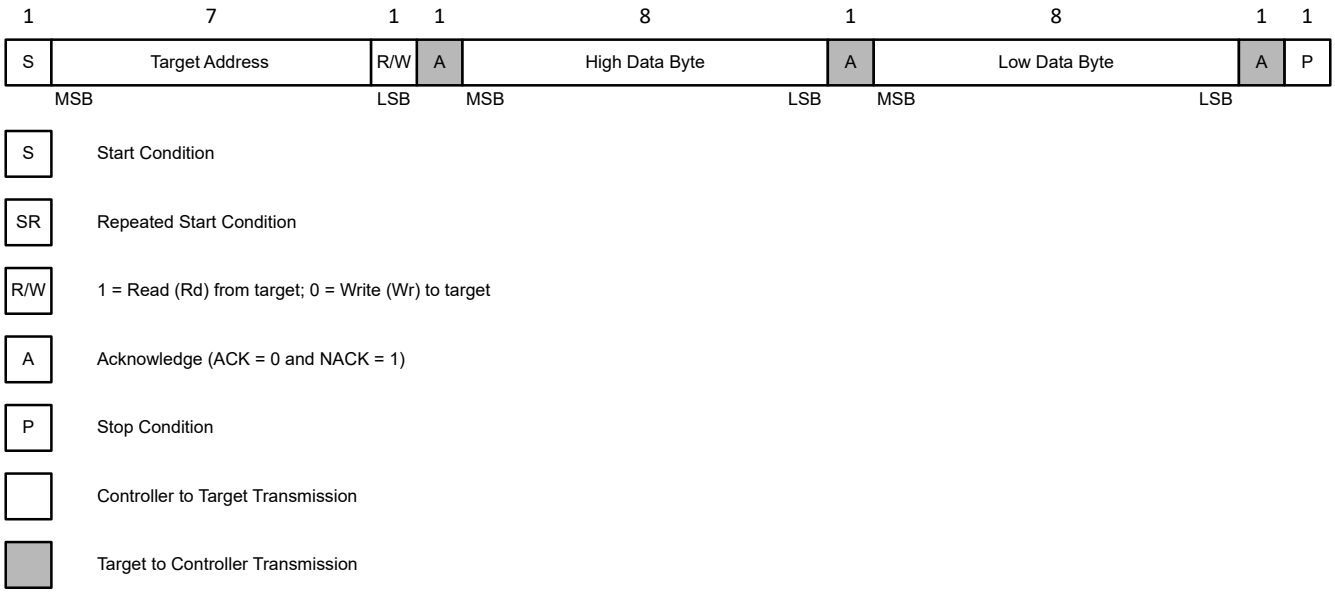

図 7-10. Generic Programming Sequence

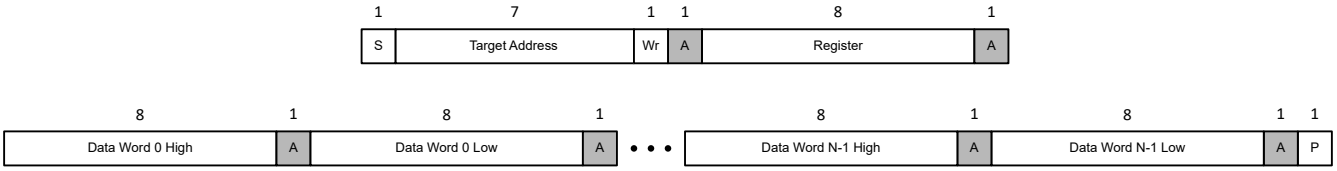

図 7-11. Generic Block Write Sequence

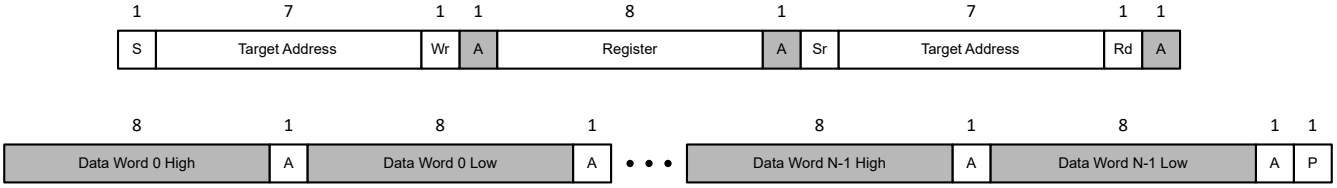

図 7-12. Generic Block Read Sequence

7.5.2 One-Time Programming Sequence

The upper register space includes all registers from R13 onward, as well as R12[15:8]. Unlocking the upper register space is performed by writing 0x5B to R12[7:0], leaving R12[15:8] unchanged. If using the edge combiner, performing the unlock first is required before modifying R146, R147, and R148.

There are six fields that can have different values depending on the EFUSE page loaded at device start-up.

- OUT0 Output Format
- OUT0 Enable
- OUT1 Output Format
- OUT1 Enable
- SSC Enable
- SSC Configuration (either preconfigured or custom)

All other fields retain the same value across all four EFUSE pages. For generating custom configurations, contact TI.

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8 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LMK3H0102 is a reference-less BAW-based clock generator that can be used to provide reference clocks for various applications, including PCIe reference clocking and 1Gb/10Gb Ethernet Switches.

8.2 Typical Applications

8.2.1 Application Block Diagram Examples

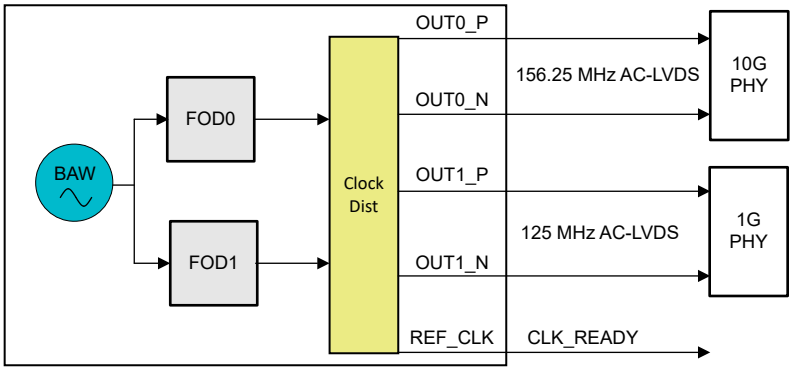

図 8-1. 1Gb/10 Gb Ethernet Switch

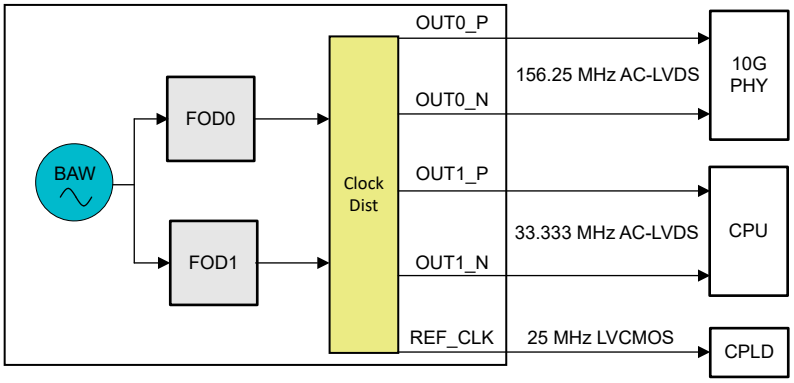

図 8-2. 10 Gb Ethernet Switch

ADVANCE INFORMATION

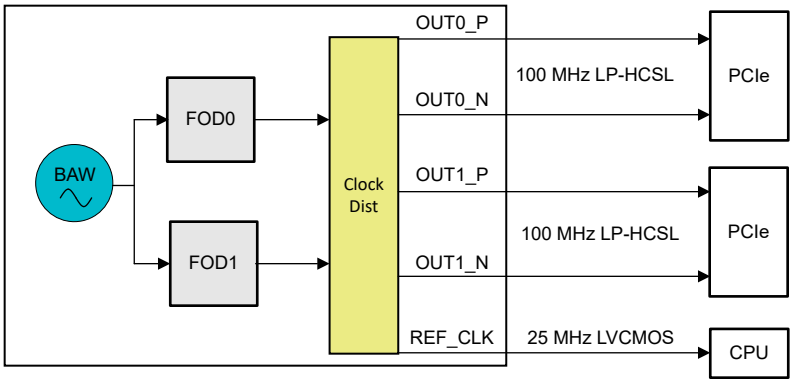

図 8-3. PCIe Applications

8.2.2 Design Requirements

Consider a typical PCIe application. In a system such as this, the clocks are expected to be available upon request without the need for any additional device-level programming. The default device configuration already outputs two 100 MHz LP-HCSL clocks, with no additional programming. A typical output clock requirement in this application is two 100 MHz LP-HCSL clocks. A 33 MHz clock is added to show how to configure the REF_CLK output as well. The section below describes the detailed design procedure to generate the required output frequencies for the above PCIe scenario using the LMK3H0102.

8.2.3 Detailed Design Procedure

Design of all aspects of the LMK3H0102 is straightforward, and software support is available to assist in frequency planning and part programming. This design procedure gives a straightforward outline of the process.

1. Frequency Planning
   a. The first step of designing an LMK3H0102 configuration is to determine the FOD frequencies that are required to generate the required output frequencies. The process is as such:
      i. If the output frequencies are greater than 200 MHz, the frequencies must both be the same, and cannot use SSC. If the frequencies are different, or require SSC, then this frequency plan cannot be supported by the device.
         - In the case of two identical frequencies greater than 200 MHz, the edge combiner must be enabled, the FOD divider values must match, and REF_CLK, if used, can be sourced from either FOD.
      ii. If both output frequencies are the same, and have the same SSC settings (that is, both use SSC or both do not use SSC), only one FOD is required.
      iii. If both output frequencies are different, but have the same SSC settings, the outputs can share an FOD to conserve current. If both frequencies can be generated from dividing a single valid FOD frequency by the channel divider options, then the second FOD can be disabled. Otherwise, both FODs must be used. If both outputs require SSC, then this frequency plan cannot be supported by the LMK3H0102 device.
      iv. If one output requires SSC and the other does not, then the SSC output must use FOD0 and the non-SSC output must use FOD1.
   b. If SSC is being used, determine whether or not a preconfigured down-spread modulation, a custom down-spread modulation, or a center-spread modulation is required for the application. If a custom configuration is required, follow the steps outlined in *Spread-Spectrum Clocking*.
   c. Set the digital clock divider such that the digital clock frequency is as close to 50 MHz as possible.
   d. Determine the REF_CTRL pin functionality. If this is used as an additional LVCMOS reference clock, verify that the desired frequency can be generated based on the FOD0 and FOD1 frequencies, as the divider range for the REF_CLK output is /2, /4, or /8 only.
      i. Keep in mind that if SSC is used on FOD0, and the REF_CLK source is FOD0, this output now has SSC as well.

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2. Setting the Output Formats
   a. The output formats that are required are based upon the clock format needed in the system. For PCIe applications, this is most often a 100-MHz LP-HCSL clock. The internal termination resistance value must be chosen such that the impedance matches the input impedance of the receiver. Note that the termination scheme is different for AC-LVDS and DC-LVDS - an AC-LVDS receiver requires an AC-LVDS output from the LMK3H0102.
   b. For differential outputs, the slew rate is selectable, from the slowest range (1.4 V/ns to 2.5 V/ns) to the fastest range (2.3 V/ns to 3.4 V/ns).
   c. For LP-HCSL outputs of either termination scheme, the amplitude is selectable between 625 mV and 885 mV.
   d. For LVCMOS outputs, the P and N phases can be in phase, opposite, or individually enabled or disabled. This allows for the generation of up to five LVCMOS clocks between OUT0, OUT1, and the REF_CTRL pin.
      i. For LVCMOS outputs, the VDDO_x voltage MUST match the VDD voltage if VDD is 1.8 V or 2.5 V.
3. Output Enable Behavior
   a. The output enable pin is active low by default, with an internal pulldown resistor to GND. If this functionality is not desired, then R7[0] can be set to '0' to change the behavior of the OE pin to active-high. If this is done, the internal pulldown is disabled, and an internal pullup to VDD is used.
   b. Determine whether or not both outputs being disabled means that the device enters low-power mode. While this is able to conserve current, low-power mode is not recommended for any applications where the clocks must turn back on quickly, such as PCIe clocking.

For the PCIe example, the following settings are required:

1. One FOD can be used to generate both LP-HCSL outputs. As such, FOD0 can be set to have an output frequency of 200 MHz, with Channel Divider 0 set to divide by two. Alternatively, FOD0 can be set to 400 MHz with a divider by four. Both configurations are valid. Both output drivers select Channel Divider 0, and are both set to LP-HCSL.
   a. DIG_CLK_N_DIV must be set to four to set the state machine clock properly.
2. FOD1 can be used to generate the 33-MHz LVCMOS clock, as FOD0 cannot support 33 MHz in addition to 100 MHz. The REF_CLK divider options are divides by two, four, or eight. While dividing by two does not yield any valid configurations, both 132 MHz with a divide by four and 264 MHz with a divide by 8 are valid options.

8.2.4 Example: Changing Output Frequency

If the user wants to change the output from 100-MHz LP-HCSL on OUT0 and OUT1 to 24-MHz differential LVCMOS clocks on OUT0 and OUT1,- with an additional LVCMOS clock on the REF_CTRL pin, the value of the BAWFREQ_OFFSET_FIXEDLUT field for this example is 0x3701. The steps for changing the frequency are as follows:

1. Determine the BAW frequency of the device. This is critical for all following calculations. From 式 4, if BAWFREQ_OFFSET_FIXEDLUT is 0x3701, then the BAW frequency of this device is approximately 2471.446441856.
2. Determine the channel divider settings and required FOD frequency. If the output frequency is 24 MHz, and the range of the FODs is from 100 MHz to 400 MHz, then a channel divider value of at least 5 is required to generate the output. As there is not a divide by 5 option, and REF_CLK must also have a clock (see CH0_DIV, CH1_DIV, and REF_CLK_DIV), a divide by 8 is required. From here, 24 MHz times 8 yields an FOD output frequency of 192 MHz. If OUT1 were a different frequency, then using FOD1 frequency can be required if both frequencies cannot be generated by dividing down from the same FOD frequency.
3. Set the FOD divide values. Use 式 1 to calculate the integer divide value FOD0_N_DIV = floor(2471.446441856/192) = 12. From 式 2, the numerator divide value FOD0_NUM = int(((2471.446441856/192) - 12) x 2^{24}) = 14631693
4. Write the desired settings to the device registers. This includes the divider settings listed above, as well as the output driver settings. Follow the procedure outlined in 図 7-4:

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a. Set PDN = 1.
b. Set FOD0_N_DIV = 12 and FOD0_NUM = 14631693.
c. Set CH0_DIV, and REF_CLK_DIV to divide by 8 (by default, OUT1_CH_SEL is set to select Channel Divider 0).
d. Set OUT0_FMT and OUT1_FMT to select Differential LVCMOS as the output format.
e. Set REF_CTRL_PIN_FUNC to output REF_CLK.
f. Set OTP_AUTOLOAD_DIS to 1 (disable the OTP Page 0 autoload feature).
g. Set PDN = 0

The time required for the frequency change to take affect is typically on the order of 1 ms between issuing PDN = 0 and the output clocks starting at the desired frequency.

8.2.5 Crosstalk

Performance degradation can occur in the LMK3H0102 due to crosstalk in the device when the outputs are operating at different frequencies. 表 8-1 displays the performance of the LMK3H0102 outputs for common LVCMOS frequencies. Contact TI for measurement of additional combinations for impact of crosstalk on output performance.

表 8-1. LMK3H0102 LVCMOS Output Crosstalk (1)

OUT0 Frequency (2)	OUT1 Frequency (2)	Worst-Case OUT0 Jitter (fs)	Worst-Case OUT1 Jitter (fs)
24	24	219.6621	226.1054
24	25	851.6348	715.6059
24	27	457.1467	371.3809
24	50	831.7157	778.6995
25	24	784.2522	717.4948
25	25	339.7724	308.0708
25	27	756.7694	786.7765
25	50	214.878	516.1349
27	24	429.2922	367.484
27	25	913.3495	641.4774
27	27	310.246	285.0789
27	50	865.1735	929.5754
50	24	806.1139	548.2382
50	25	559.1824	286.6788
50	27	912.9378	704.1768
50	50	402.6511	348.2761

(1) Measured over 25 °C to 105 °C using differential LVCMOS output formats using VDD = VDDO_x = 3.3 V, no SSC
(2) OUT0 and OUT1 are generated using FOD0 and FOD1, respectively.

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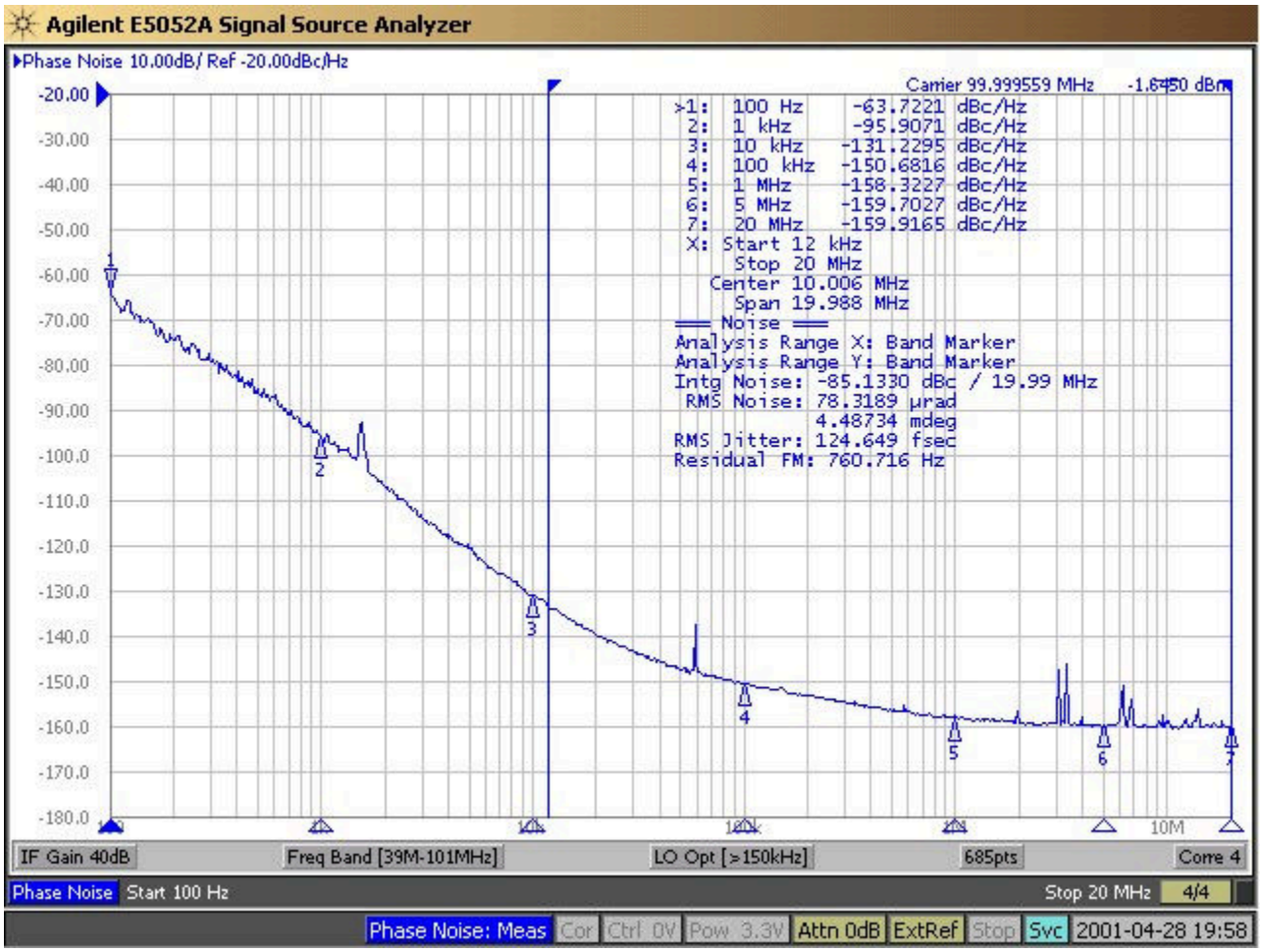
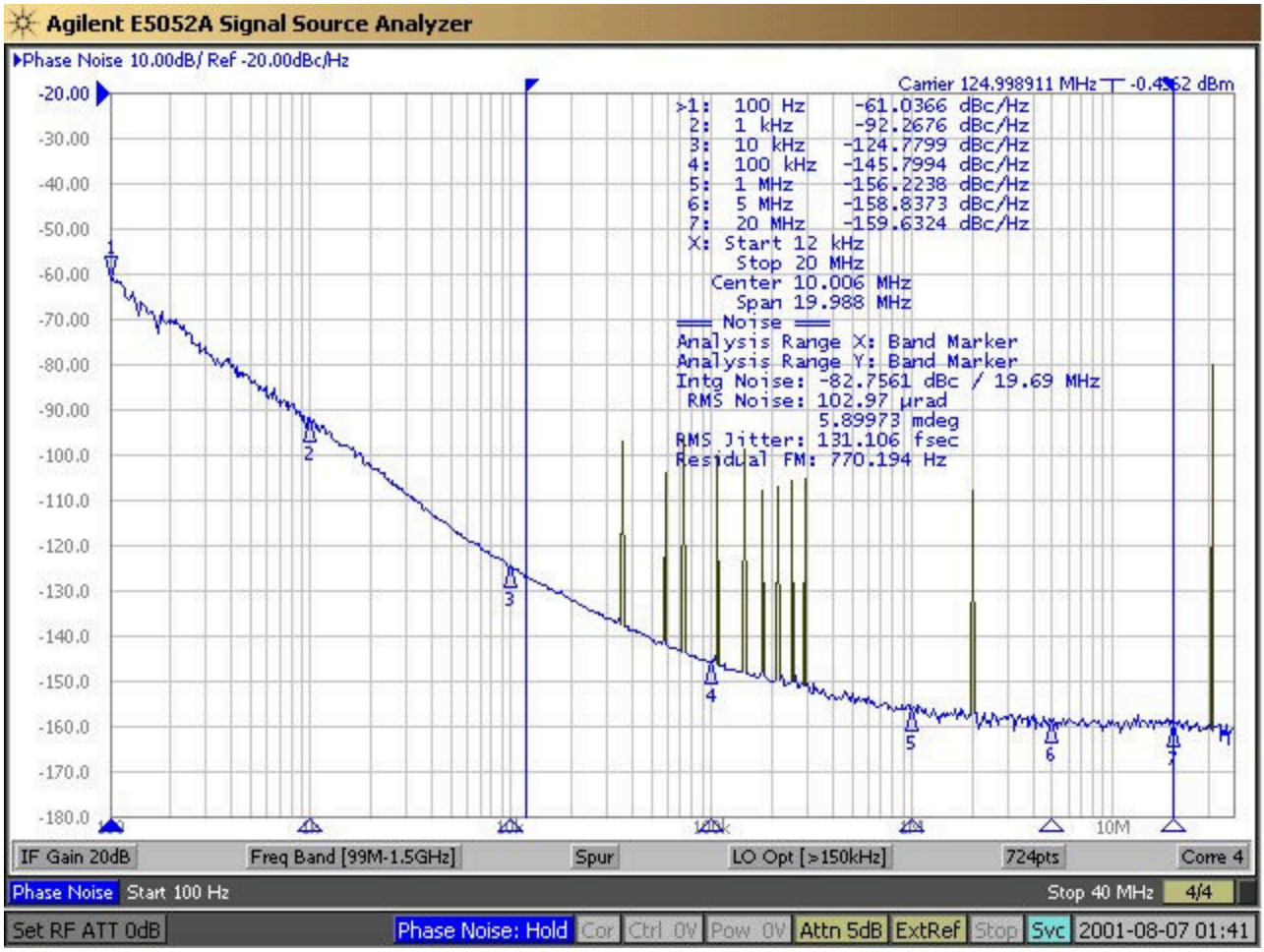
8.2.6 Application Curves



OUT0: 100 MHz LP-HCSL
OUT1: 100 MHz LP-HCSL
Temperature: 25 °C
12k – 20M RMS Jitter: 125 fs

図 8-4. 100-MHz LP-HCSL Output for PCIe Application, Measured on OUT0

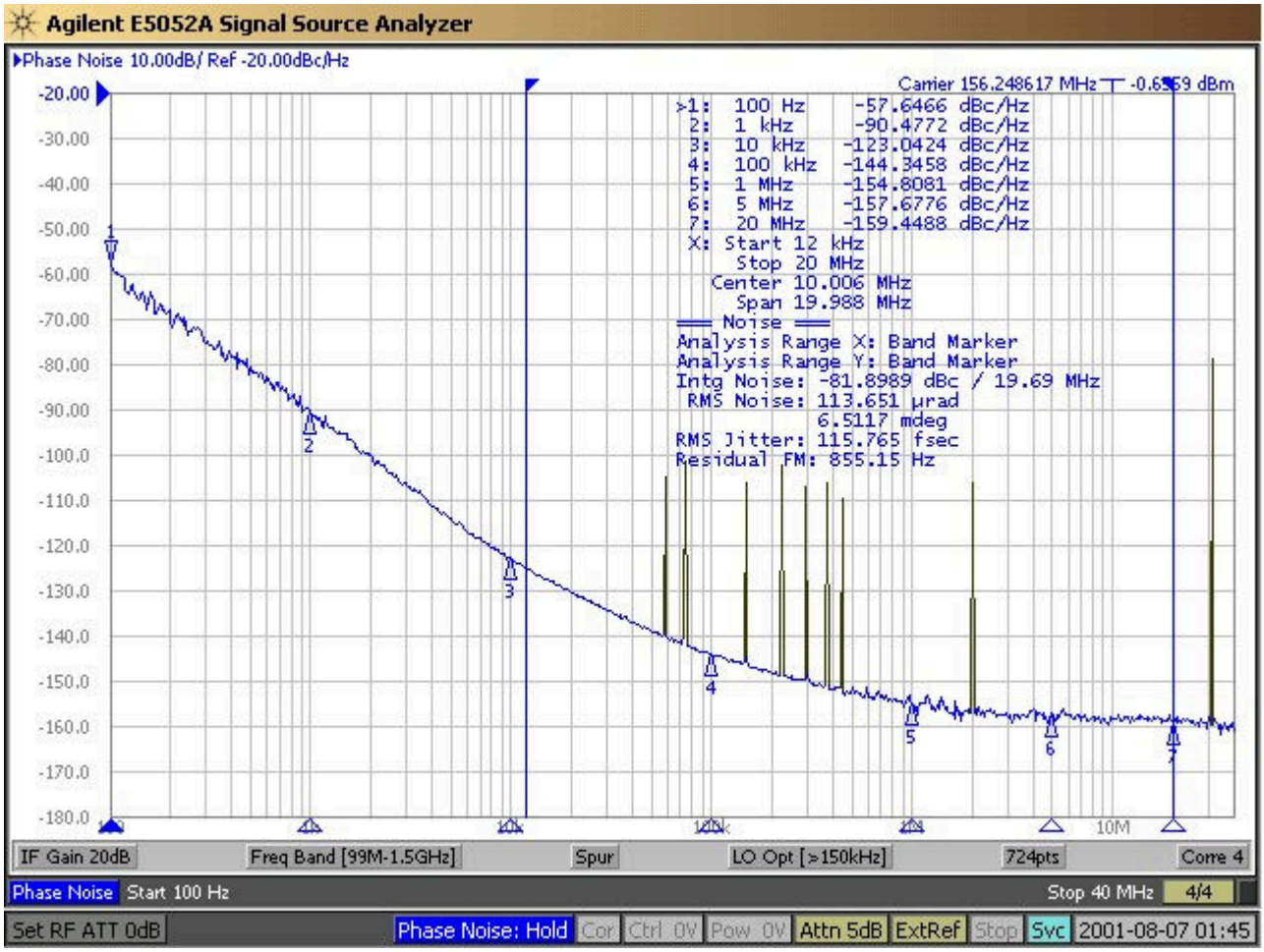
ADVANCE INFORMATION



OUT0: 125 MHz LP-HCSL
OUT1: 125 MHz LP-HCSL
Temperature: 25 °C
12k – 20M RMS Jitter: 131 fs

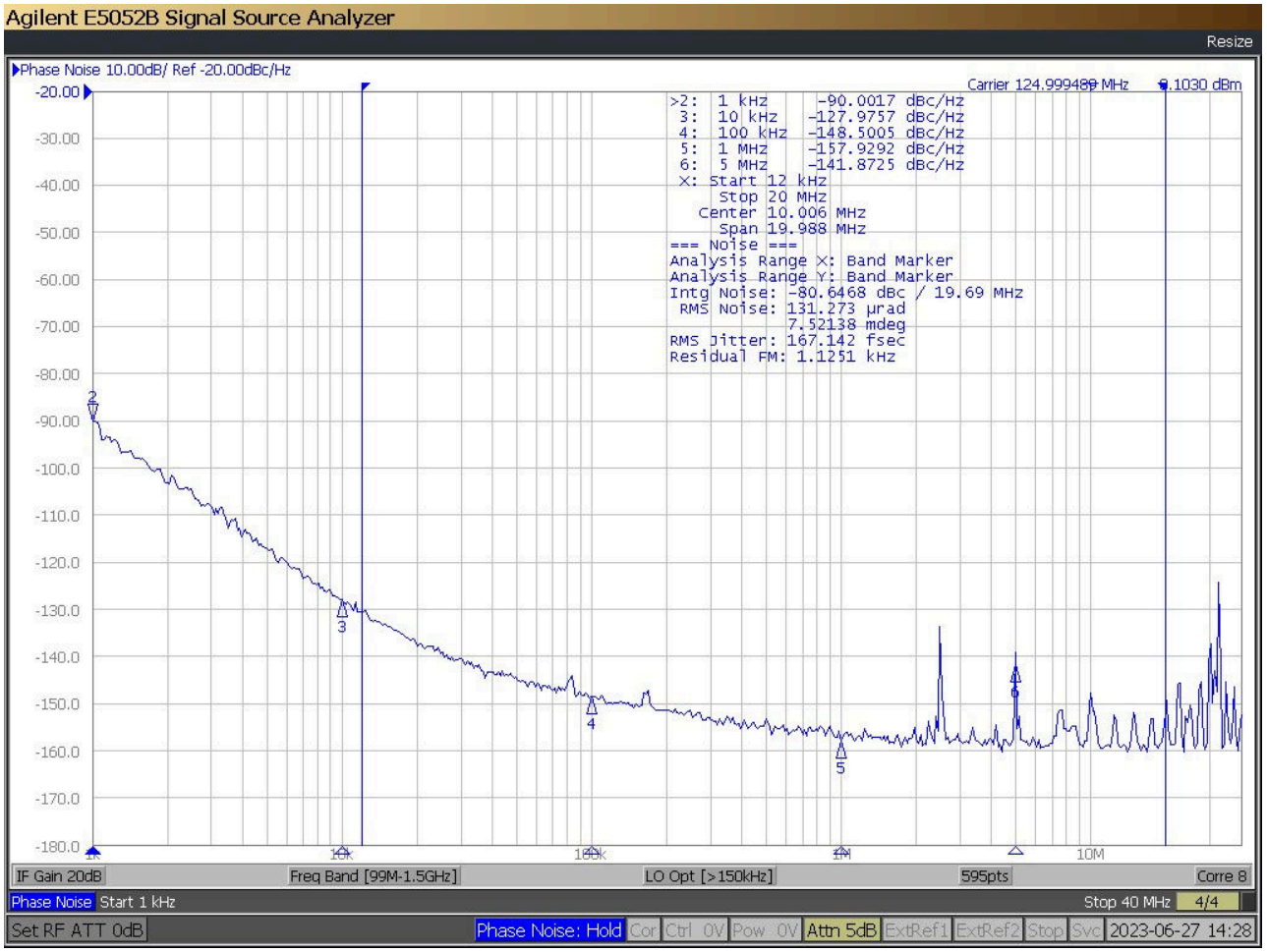
図 8-5. 125-MHz LP-HCSL Output, Measured on OUT0

ADVANCE INFORMATION



OUT0: 156.25 MHz LP-HCSL
OUT1: 156.25 MHz LP-HCSL
Temperature: 25 °C
12k – 20M RMS Jitter: 116 fs

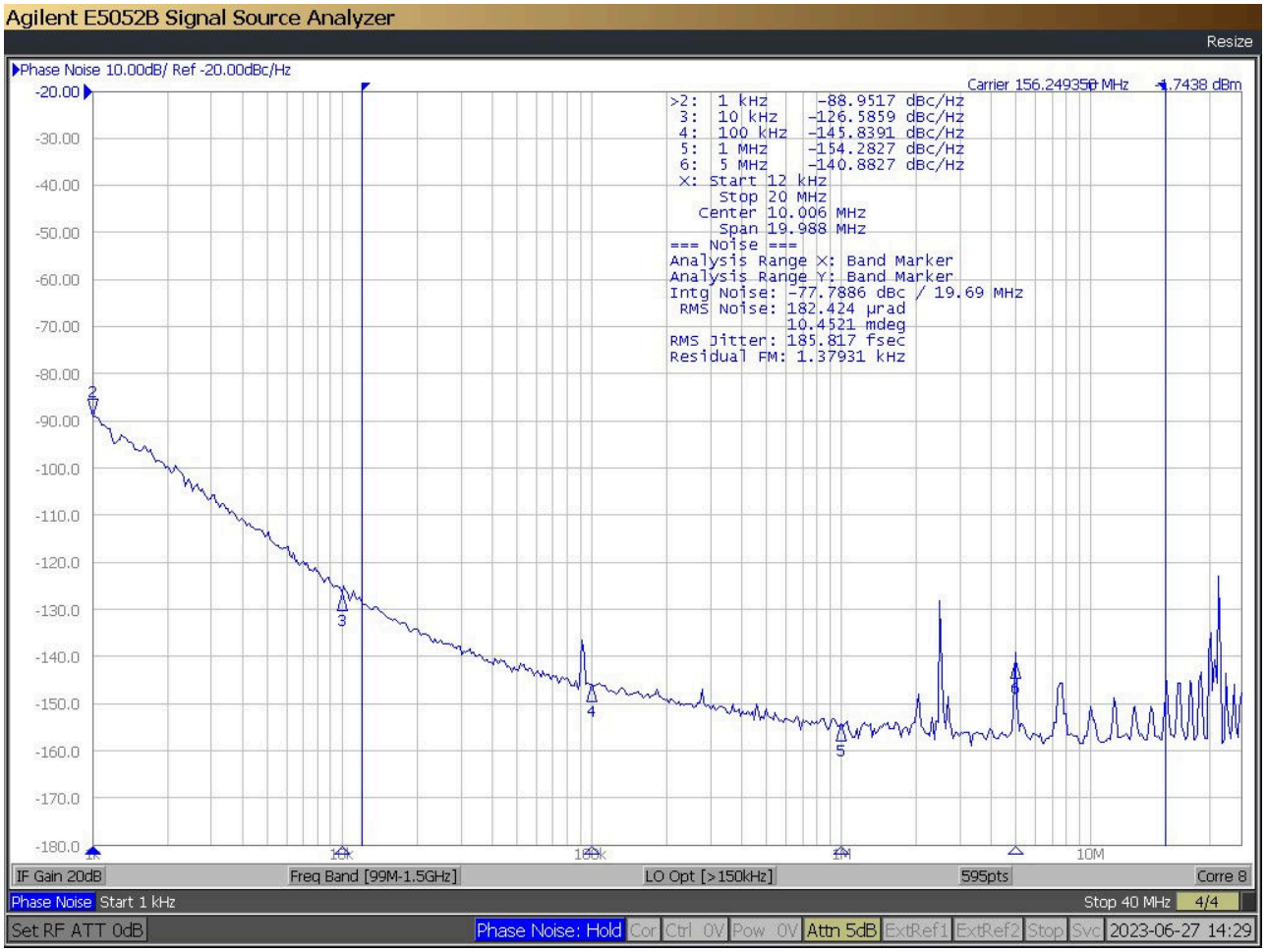
図 8-6. 156.25-MHz LP-HCSL Output, Measured on OUT0



OUT0: 125 MHz LP-HCSL
OUT1: 156.25 MHz LP-HCSL
Temperature: 25 °C
12k – 20M RMS Jitter: 167 fs

図 8-7. 125-MHz LP-HCSL on OUT0 with 156.25-MHz LP-HCSL on OUT1

ADVANCE INFORMATION



OUT0: 125 MHz LP-HCSL
OUT1: 156.25 MHz LP-HCSL
Temperature: 25 °C
12k – 20M RMS Jitter: 186 fs

図 8-8. 156.25-MHz LP-HCSL on OUT1 with 125 MHz-LP-HCSL on OUT0

9 Power Supply Recommendations

9.1 Power-Up Sequencing

The LMK3H0102 provides multiple power supply pins. Each power supply supports 1.8 V, 2.5 V, or 3.3 V. Internal low-dropout regulators (LDO) source the internal blocks and allow each pin to be supplied with individual supply voltages. The VDD pin supplies the control pins, the serial interface, and the REF_CTRL pin. Therefore, any pullup resistors must be connected to the same domain as VDD. VDDO_0 powers output OUT0, and can be left floating if OUT0 is unused. VDDO_1 powers OUT1, and can be left floating if OUT1 is unused.

There are no restrictions from the device for applying power to the supply pins. From an application perspective, TI recommends to either apply all the VDDs at the same time or apply the VDD first, as the digital core is powered by VDD.

9.2 Decoupling Power Supply Inputs

Do not tie VDD and VDDO pins to ground. Use a separate ferrite bead to isolate the VDD and the VDDO supplies. If OUT0 and OUT1 are different frequencies, a separate ferrite bead must be used for each VDDO supply. For each supply voltage pin, a 0.1-µF or 1-µF capacitor must be placed very close to the pin.

10 Layout

10.1 Layout Guidelines

For this example, follow these guidelines:

- Isolate outputs using a GND shield. Route all outputs as differential pairs.
- Isolate outputs to adjacent outputs when generating multiple frequencies.
- Avoid impedance jumps in the fan-in and fan-out areas when possible.
- Use five vias to connect the thermal pad to a solid GND plane. Full-through vias are preferred.
- Place decoupling capacitors with small capacitance values very close to the supply pins. Place the decoupling capacitors on the same layer or on the bottom layer directly underneath the device. Larger values can be placed more far away. Ferrite beads are recommended to isolate the different output supplies and the VDD supply.
- Use multiple vias to connect wide supply traces to the respective power planes.

10.2 Layout Example

Below are printed circuit board (PCB) layout examples that show the application of thermal design practices and a low-inductance ground connection between the device DAP and the PCB.

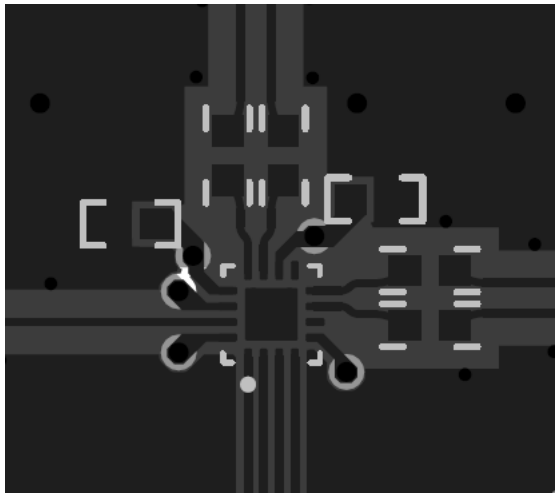


図 10-1. PCB Layout Example for LMK3H0102, Top Layer

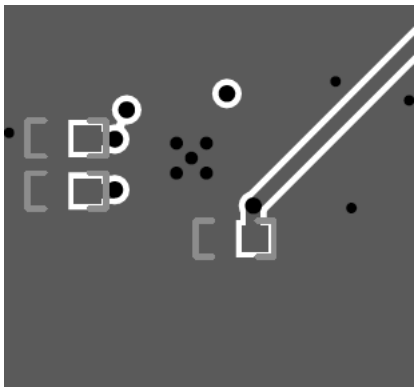


図 10-2. PCB Layout Example for LMK3H0102, Bottom Layer

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Documentation Support

11.1.1 Related Documentation

For documentation related to the Evaluation module, refer to LMK3H0102EVM User's Guide.

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントを工キスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

11.4 Trademarks

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11.5 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.6 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

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12 Device Registers

12.1 Register Maps

表 12-1 lists the LMK3H0102 Device registers. All register offset address not listed in 表 12-1 can be considered as reserved locations and the register contents must not be modified.

表 12-1. LMK3H0102 Registers

Address	Acronym	Section
0x0	R0	Go
0x1	R1	Go
0x2	R2	Go
0x3	R3	Go
0x4	R4	Go
0x5	R5	Go
0x6	R6	Go
0x7	R7	Go
0x8	R8	Go
0x9	R9	Go
0xA	R10	Go
0xB	R11	Go
0xC	R12	Go
0x1B	R27	Go
0x1C	R28	Go
0x20	R32	Go
0x21	R33	Go
0x92	R146	Go
0x93	R147	Go
0x94	R148	Go
0xEE	R238	Go

Complex bit access types are encoded to fit into small table cells. 表 12-2 shows the codes that are used for access types in this section.

表 12-2. LMK3H0102 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
WL	W L	Write Locked, requires R12[7:0] = 0x5B to unlock and write successfully

12.1.1 R0 Register (Address = 0x0) [reset = 0x0861]

R0 is shown in 表 12-3.

Return to the Summary Table.

表 12-3. R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	DIG_CLK_N_DIV	R/W	0x02	Digital State Machine clock rate. Derived from FOD frequency. Target is 45 MHz
9:3	FOD0_N_DIV	R/W	0x0C	Integer Ratio of BAW frequency to FOD0 frequency.
2:1	Reserved	R	0x0	Reserved, do not write to this field.
0	OTP_BURNT	R/WL	0x1	Indicates if the EFUSE has been programmed. If this field is '1', the EFUSE is programmed.

12.1.2 R1 Register (Address = 0x1) [reset = 0x5599]

R1 is shown in 表 12-4.

Return to the Summary Table.

表 12-4. R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	FOD0_NUM[23:16]	R/W	0x55	High byte of the FOD0 fractional divide value.
7:0	ADC_CLK_N_DIV	R/W	0x99	ADC clock frequency in MHz, derived directly from BAW. Default is ceil(2467 / 16) = 0x9B. TI does not recommend modifying the value of this field.

12.1.3 R2 Register (Address = 0x2) [reset = 0xC28F]

R2 is shown in 表 12-5.

Return to the Summary Table.

表 12-5. R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	FOD0_NUM[15:0]	R/W	0xC28F	Lower two bytes of the FOD0 fractional divide value.

12.1.4 R3 Register (Address = 0x3) [reset = 0x1801]

R3 is shown in 表 12-6.

Return to the Summary Table.

表 12-6. R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	FOD1_N_DIV	R/W	0x0C	Integer Ratio of BAW frequency to FOD1 frequency.
8	CH1_FOD_SEL	R/W	0x0	Selects the FOD to use as the input source for Channel Divider 1. 0h: FOD0. 1h: FOD1.
7	CH1_EDGE_COMB_EN	R/W	0x0	Selects between using one of the FODs or using the Edge Combiner as the input source for Channel Divider 1. Both CH0_EDGE_COMB_EN and CH1_EDGE_COMB_EN must be set to '1' for the edge combiner to be enabled. 0h: FOD input 1h: Edge Combiner input
6	OUT1_DISABLE_STATE	R/W	0x0	When OUT1 is disabled, this bit selects whether the OUT1_P and OUT1_N pins are forced to GND or tri-state. 0h: Forced to GND on disable. 1h: Tri-state on disable.

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表 12-6. R3 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
5	OUT0_DISABLE_STATE	R/W	0x0	When OUT0 is disabled, this bit selects whether the OUT0_P and OUT0_N pins are forced to GND or tri-state. 0h: Forced to GND on disable. 1h: Tri-state on disable.
4	CH0_FOD_SEL	R/W	0x0	Selects the FOD to use as the input source for Channel Divider 0. 0h: FOD0. 1h: FOD1.
3	CH0_EDGE_COMB_EN	R/W	0x0	Selects between using one of the FODs or using the Edge Combiner as the input source for Channel Divider 0. Both CH0_EDGE_COMB_EN and CH1_EDGE_COMB_EN must be set to '1' for the edge combiner to be enabled. 0h: FOD input 1h: Edge Combiner input
2:0	CH0_DIV	R/W	0x1	Divider value for Channel Divider 0. 0h: Channel Divider disabled. 1h: FOD / 2 2h: FOD / 4 3h: FOD / 6 4h: FOD / 8 5h: FOD / 10 6h: FOD / 20 7h: FOD / 40

12.1.5 R4 Register (Address = 0x4) [reset = 0x0000]

R4 is shown in 表 12-7.

Return to the Summary Table.

表 12-7. R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R	0x0	Reserved
14:2	SSC_STEPS	R/W	0x0000	Number of steps in each segment of the triangular profile for SSC. See Spread Spectrum Clocking for instructions to calculate this value.
1	SSC_MOD_TYPE	R/W	0x0	Selects between down-spread or center-spread modulation for custom SSC configurations. 0h: Down-spread modulation. 1h: Center-spread modulation.
0	SSC_EN	R/W	0x0	Enable SSC. 0h: SSC Disabled. 1h: SSC Enabled.

12.1.6 R5 Register (Address = 0x5) [reset = 0x0000]

R5 is shown in 表 12-8.

Return to the Summary Table.

表 12-8. R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	SSC_STEP_SIZE	R/W	0x0000	Numerator increment value per step for SSC. See Spread Spectrum Clocking for instructions to calculate this value.

12.1.7 R6 Register (Address = 0x6) [reset = 0x2AA0]

R6 is shown in 表 12-9.

Return to the Summary Table.

表 12-9. R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	CH1_DIV	R/W	0x1	Divider value for Channel Divider 1. 0h: Channel Divider disabled. 1h: FOD / 2 2h: FOD / 4 3h: FOD / 6 4h: FOD / 8 5h: FOD / 10 6h: FOD / 20 7h: FOD / 40
12:5	FOD1_NUM[23:16]	R/W	0x55	High byte of the FOD1 fractional divide value.
4:3	OUT0_SLEW_RATE	R/W	0x0	Slew rate control for OUT0. Only applies to differential output formats. 0h: Between 2.3 and 3.4 V/ns. 1h: Between 2.0 and 3.0 V/ns. 2h: Between 1.7 and 2.7 V/ns. 3h: Between 1.4 and 2.5 V/ns.
2:0	OUT0_FMT	R/W	0x0	Selects the output format for OUT0. 0h: LP-HCSL 100 Ω Termination. 1h: LP-HCSL 85 Ω Termination. 2h: AC-coupled LVDS. 3h: DC-coupled LVDS. 4h: LVCMOS, OUTx_P enabled, OUTx_N disabled. 5h: LVCMOS, OUTx_P disabled, OUTx_N enabled. 6h: LVCMOS, OUTx_P enabled, OUTx_N enabled, 180 degrees out of phase. 7h: LVCMOS, OUTx_P enabled, OUTx_N enabled, OUTx_P and OUTx_N in phase.

12.1.8 R7 Register (Address = 0x7) [reset = 0x6503]

R7 is shown in 表 12-10.

Return to the Summary Table.

表 12-10. R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R	0x0	Reserved
14:13	REF_CTRL_PIN_FUNC	R/W	0x3	Sets the function of the REF_CTRL pin. 0h: REF_CTRL pin disabled, pulled to GND. 1h: REF_CTRL pin disabled, tri-state. 2h: REF_CTRL pin functions as an additional LVCMOS REF_CLK output. 3h: REF_CTRL pin functions as "clock ready" signal.
12:11	REF_CLK_DIV	R/W	0x0	REF_CLK output divisor value when REF_CTRL is used as REF_CLK. 0h: REF_CLK disabled. 1h: FOD / 2. 2h: FOD / 4. 3h: FOD / 8.
10	Reserved	R/W	0x1	Reserved. Do not write any value other than '1' to this field.

表 12-10. R7 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
9	REF_CLK_FOD_SEL	R/W	0x0	Select the FOD used to generate the REF_CLK output. 0h: FOD0. 1h: FOD1.
8	OUT1_EN	R/W	0x1	Output Enable bit for OUT1. 0h: OUT1 is disabled. 1h: OUT1 is enabled.
7	OUT1_CH_SEL	R/W	0x0	Selects the source for OUT1. If the Edge Combiner is enabled, then this bit is ignored. 0h: OUT1 is sourced from Channel Divider 0. 1h: OUT1 is sourced from Channel Divider 1.
6:5	OUT1_SLEW_RATE	R/W	0x0	Slew rate control for OUT01 Only applies to differential output formats. 0h: Between 2.3 and 3.4 V/ns. 1h: Between 2.0 and 3.0 V/ns. 2h: Between 1.7 and 2.7 V/ns. 3h: Between 1.4 and 2.5 V/ns.
4:2	OUT1_FMT	R/W	0x0	Selects the output format for OUT1. 0h: LP-HCSL 100-Ω Termination. 1h: LP-HCSL 85-Ω Termination. 2h: AC-coupled LVDS. 3h: DC-coupled LVDS. 4h: LVCMOS, OUTx_P enabled, OUTx_N disabled. 5h: LVCMOS, OUTx_P disabled, OUTx_N enabled. 6h: LVCMOS, OUTx_P enabled, OUTx_N enabled, 180 degrees out of phase. 7h: LVCMOS, OUTx_P enabled, OUTx_N enabled, OUTx_P and OUTx_N in phase.
1	OUT0_EN	R/W	0x1	Output Enable bit for OUT0. 0h: OUT0 is disabled. 1h: OUT0 is enabled.
0	OE_PIN_POLARITY	R/W	0x1	OE pin polarity selection. This bit does not affect the polarity of the OUTx_EN bits, only the OE pin. 0h: OE is active high (OE tied to VDD enables outputs). 1h: OE is active low (OE tied to GND enables outputs).

12.1.9 R8 Register (Address = 0x8) [reset = 0xC28F]

R8 is shown in 表 12-11.

Return to the Summary Table.

表 12-11. R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	FOD1_NUM[15:0]	R/W	0xC28F	Lower two bytes of the FOD1 fractional divide value.

12.1.10 R9 Register (Address = 0x9) [reset = 0x0066]

R9 is shown in 表 12-12.

Return to the Summary Table.

表 12-12. R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	OTP_ID	R/W	0x0	Configurable field for identifying the OTP configuration. Can be used in I2C mode as a 4-bit spare field.
11:9	SSC_CONFIG_SEL	R/W	0x0	SSC modulation configuration. If center-spread modulation is desired, then custom SSC configuration is required. Four pre-configured down-spread modulation depths are also available - other modulation depths require custom SSC configuration. 0h: Custom SSC Configuration - see Spread Spectrum Clocking for details on creating a custom configuration. 1h: –0.10% pre-configured down-spread. 2h: –0.25% pre-configured down-spread. 3h: –0.30% pre-configured down-spread. 4h: –0.50% pre-configured down-spread. All other values: Reserved
8	OUT_FMT_SRC_SEL	R/W	0x0	Forces the FMT_ADDR pin to override the output format register settings in OTP Mode. When in I2C mode, the FMT_ADDR pin is never used for this purpose. 0h: FMT_ADDR pin is ignored in OTP mode. 1h: FMT_ADDR pin overrides the register settings. The output format is LP-HCSL, and the termination resistor values are based on the FMT_ADDR pin state on start-up.
7:4	OUT1_LPHSCL_AMP_SEL	R/W	0x6	OUT1 output swing level when using LP-HCSL output format. 0h: 625 mV. 1h: 647 mV. 2h: 668 mV. 3h: 690 mV. 4h: 712 mV. 5h: 733 mV. 6h: 755 mV. 7h: 777 mV. 8h: 798 mV. 9h: 820 mV. Ah: 842 mV. Bh: 863 mV. Ch: 885 mV. Dh: 907 mV. Eh: 928 mV. Fh: 950 mV.

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表 12-12. R9 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
3:0	OUT0_LPHSCL_AMP_SEL	R/W	0x6	OUT0 output swing level when using LP-HCSL output format. 0h: 625 mV. 1h: 647 mV. 2h: 668 mV. 3h: 690 mV. 4h: 712 mV. 5h: 733 mV. 6h: 755 mV. 7h: 777 mV. 8h: 798 mV. 9h: 820 mV. Ah: 842 mV. Bh: 863 mV. Ch: 885 mV. Dh: 907 mV. Eh: 928 mV. Fh: 950 mV.

12.1.11 R10 Register (Address = 0xA) [reset = 0x0010]

R10 is shown in 表 12-13.

Return to the Summary Table.

表 12-13. R10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PUP_DTC_GAIN_CAL_EN	R/W	0x0	Writing a '1' to this bit enables gain calibration on power up. This is recommended for applications where the clock frequencies differ from the default settings.
14:11	PROD_REVID	R	0x0	Product revision identifier.
10	CLK_READY	R	0x0	CLK_READY status. The REF_CTRL pin mirrors this status signal when the pin functions as a "clock ready" signal.
9	CRC_ERROR	R	0x0	This bit indicates if there was a CRC error when programming the EFUSE of the device. If this bit is a '1', then an error has occurred. Outside of EFUSE programming, this bit can be ignored.
8	RB_PIN_15	R	0x0	Readback of the REF_CTRL pin.
7	RB_PIN_4	R	0x0	Readback of the OTP_SEL1/SDA pin.
6	RB_PIN_3	R	0x0	Readback of the OTP_SEL0/SCL pin.
5	RB_PIN_2	R	0x0	Readback of the FMT_ADDR pin.
4	DEV_IDLE_STATE_SEL	R/W	0x1	This bit controls the behavior of the device when both outputs are disabled. Placing the device into a low-power state is not recommended for PCIe applications, as the time to re-enable the clocks is extended. 0h: When both outputs are disabled, the outputs are muted, and the device is placed into a low-power state. 1h: When both outputs are disabled, the outputs are muted. The device does not enter a low-power state.
3	Reserved	R/W	0x0	Reserved. Only write '0' to this bit.
2	Reserved	R/W	0x0	Reserved. Only write '0' to this bit.
1	PDN	R/W	0x0	Writing a '1' to this bit forces a power down all analog logic blocks.
0	Reserved	R/W	0x0	Reserved. Only write '0' to this bit.

12.1.12 R11 Register (Address = 0xB) [reset = 0x0000]

R11 is shown in 表 12-14.

Return to the Summary Table.

表 12-14. R11 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	Reserved	R/W	0x0	Reserved
8:1	SPARE	R/W	0x0	This field functions as a spare byte.
0	DTC_GAIN_CAL_MODE	R/W	0x0	Disables FODs not in use during gain calibration. 0h: Unused FOD is allowed to run during gain calibration. 1h: Unused FOD is disabled during gain calibration.

12.1.13 R12 Register (Address = 0xC) [reset = 0xE800]

R12 is shown in 表 12-15.

Return to the Summary Table.

表 12-15. R12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	I2C_ADDR_LSB_SEL	R/WL	0x1	I2C peripheral address source. 0h: I2C peripheral address comes entirely from the I2C_ADDR field. 1h: The two lowest bits of the I2C peripheral address come from the FMT_ADDR pin, all other bits come from R12[14:10].
14:8	I2C_ADDR	R/WL	0x68	I2C peripheral address. After writing to this field, the device responds to the new I2C address.
7:0	UNLOCK_PROTECTED_REG	R/W	0x00	This field locks all registers from R13 onward, in addition to R12[15:8]. Registers R13 onward are largely device calibration registers, and must not have their contents modified. These registers can be read from normally regardless of the unlock status. 5Bh: Unlocks register writes for R12[15:8] and above. Any other value: R12[15:8] and above ignore all writes.

12.1.14 R27 Register (Address = 0x1B) [reset = 0x0000]

R27 is shown in 表 12-16.

Return to the Summary Table.

表 12-16. R27 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	EFC_WDATA	R/WL	0x0000	EFUSE Controller Write Data. See One-Time Programming Sequence for more details on using this register.

12.1.15 R28 Register (Address = 0x1C) [reset = 0x0000]

R28 is shown in 表 12-17.

Return to the Summary Table.

表 12-17. R28 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R/WL	0x0	Reserved
14	Reserved	R/WL	0x0	Reserved
13	Reserved	R/WL	0x0	Reserved
12	EFC_READY	R	0x0	Indicates that the EFUSE Controller is ready for read/write operations

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表 12-17. R28 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
11:6	EFC_ERROR	R	0x0	EFUSE Controller error status indicator
5:0	EFC_ADDR	R/WL	0x0	EFUSE Controller Address

12.1.16 R32 Register (Address = 0x20) [reset = 0x0000]

R32 is shown in 表 12-18.

Return to the Summary Table.

表 12-18. R32 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	EFC_DUMP_L	R/W	0x0000	Lower 16 bits of readback from the device EFUSE.

12.1.17 R33 Register (Address = 0x21) [reset = 0x0000]

R33 is shown in 表 12-19.

Return to the Summary Table.

表 12-19. R33 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	EFC_DUMP_H	R/W	0x0000	Upper 16 bits of readback from the device EFUSE.

12.1.18 R146 Register (Address = 0x92) [reset = 0x0000]

R146 is shown in 表 12-20.

Return to the Summary Table.

表 12-20. R146 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	Reserved	R/WL	0x0	Reserved. Only write '0' to these bits.
12:5	DTC1_GAIN_RT	R/WL	0x00	Room temperature gain calibration code for FOD0. This must be averaged with DTC2_GAIN_RT when using the edge combiner.
4:0	DTC1_GAIN_DELTA_CT	R/WL	0x00	Cold temperature gain calibration code for FOD0. This must be averaged with DTC2_GAIN_DELTA_CT when using the edge combiner.

12.1.19 R147 Register (Address = 0x93) [reset = 0x0000]

R147 is shown in 表 12-21.

Return to the Summary Table.

表 12-21. R147 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	Reserved	R/WL	0x00	Reserved. Only write '0' to these bits.
13:8	DTC2_GAIN_DELTA_CT	R/WL	0x00	Cold temperature gain calibration code for FOD1. This must be averaged with DTC1_GAIN_DELTA_CT when using the edge combiner.
7:0	DTC1_GAIN_DELTA_HT	R/WL	0x00	Hot temperature gain calibration code for FOD0. This must be averaged with DTC2_GAIN_DELTA_HT when using the edge combiner.

12.1.20 R148 Register (Address = 0x94) [reset = 0x0000]

R148 is shown in 表 12-22.

Return to the Summary Table.

表 12-22. R148 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	Reserved	R/WL	0x0	Reserved. Only write '0' to these bits.
13:8	DTC2_GAIN_DELTA_HT	R/WL	0x00	Hot temperature gain calibration code for FOD1. This must be averaged with DTC1_GAIN_DELTA_HT when using the edge combiner.
7:0	DTC2_GAIN_RT	R/WL	0x00	Room temperature gain calibration code for FOD1. This must be averaged with DTC1_GAIN_RT when using the edge combiner.

12.1.21 R238 Register (Address = 0xEE) [reset = 0x0000]

R246 is shown in 表 12-23.

Return to the Summary Table.

表 12-23. R246 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	BAWFREQ_OFFSET_FIXEDLUT	R/WL	0x0000	Offset value from 2467 MHz for the BAW frequency. Signed 16-bit integer value. Each bit of this fields corresponds to 128 ppm of frequency deviation. **This field varies from part to part.** This field is for calculation purposes only, the device does not use this register for any internal calculation. Do **NOT** write to this field.

ADVANCE INFORMATION

13 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
November 2023	*	Initial Release

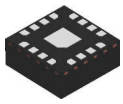
14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

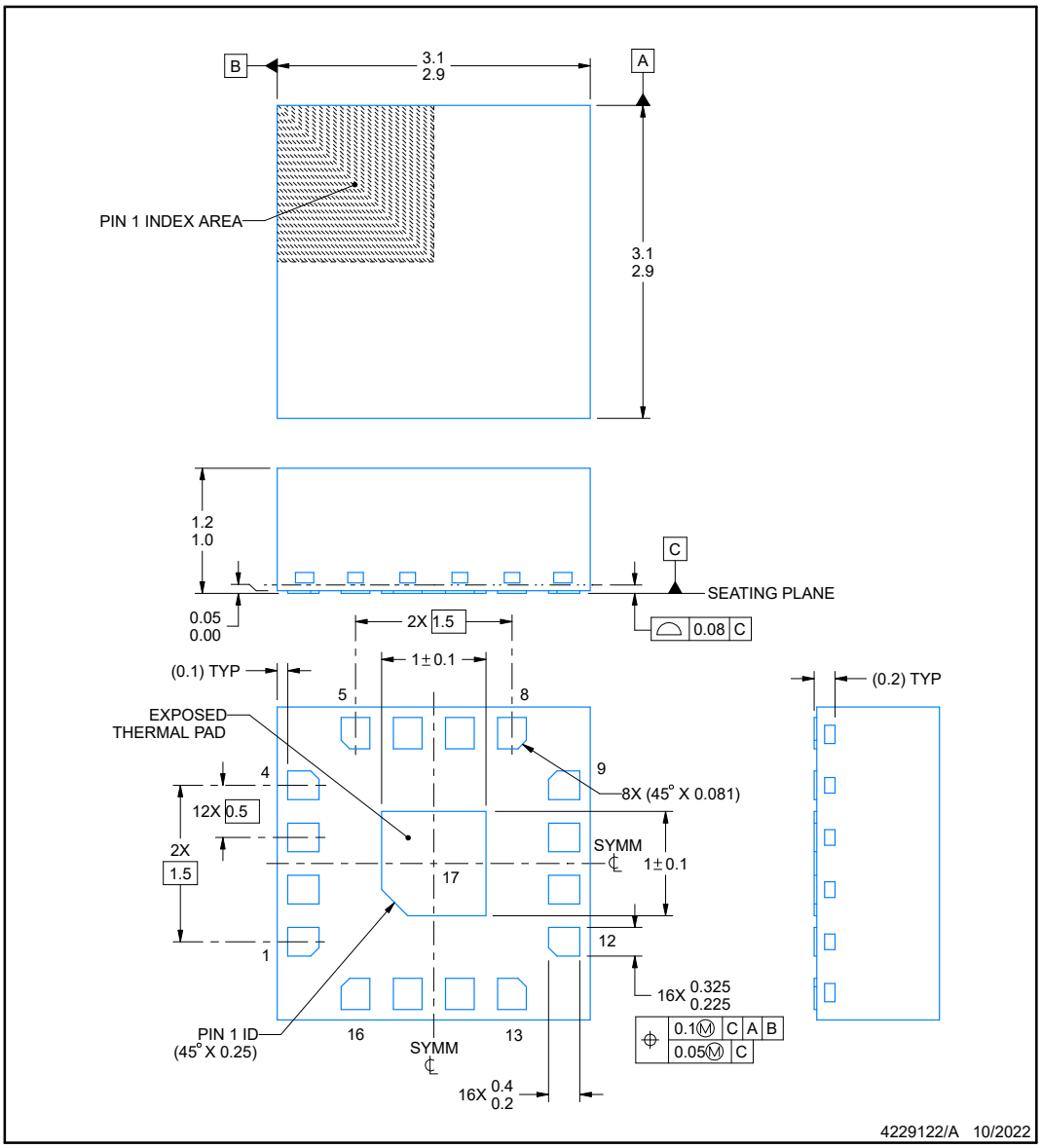
PACKAGE OUTLINE

RER0016A



TQFN - 1.2 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

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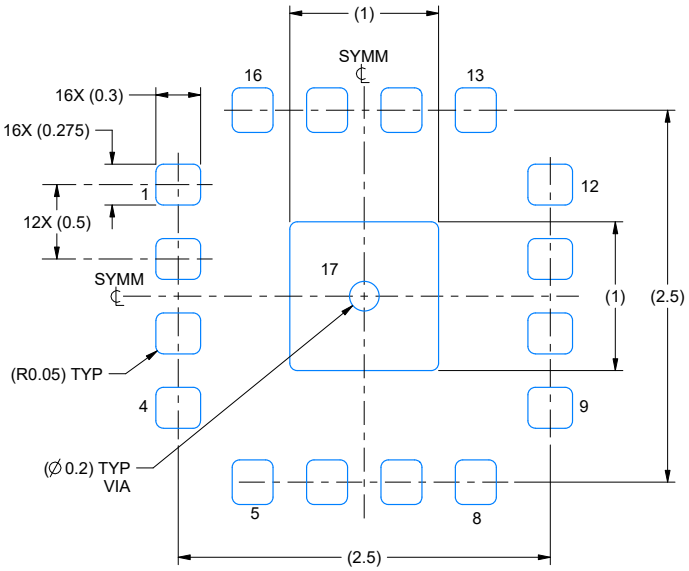
ADVANCE INFORMATION

ADVANCE INFORMATION

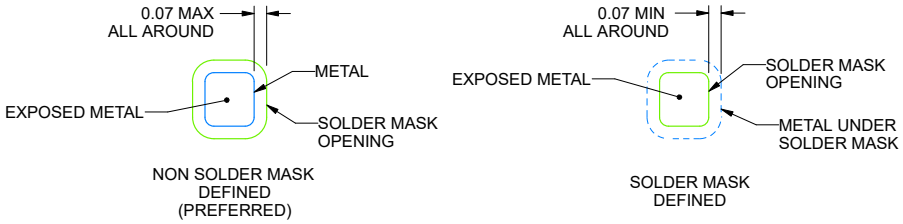
EXAMPLE BOARD LAYOUT

RER0016A — **TQFN - 1.2 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X



SOLDER MASK DETAILS

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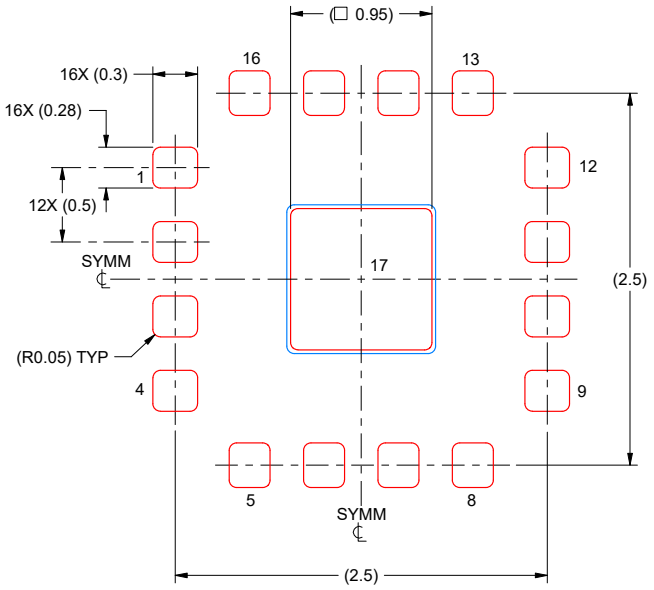
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RER0016A — **TQFN - 1.2 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

14.1 Package Option Addendum

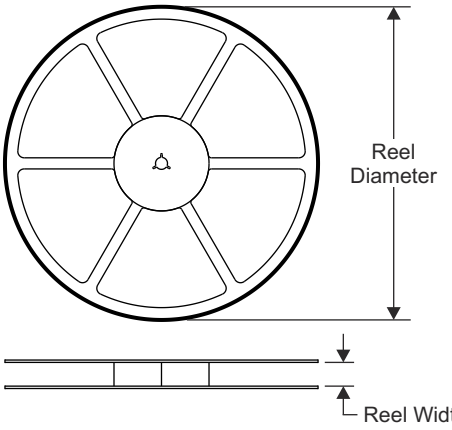
Packaging Information

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking
LMK3H0102RERR	PRE_PROD	TQFN	RER	16	3000	RoHS & Green	NIPDAU	Level-2-260C-168 HR	-40 to 85	PLMK3H
LMK3H0102RERT	PRE_PROD	TQFN	RER	16	250	RoHS & Green	NIPDAU	Level-2-260C-168 HR	-40 to 85	PLMK3H

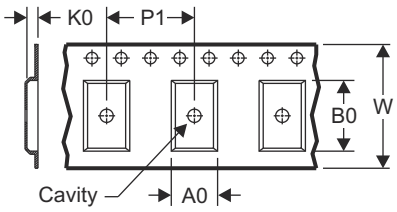
ADVANCE INFORMATION

14.2 Tape and Reel Information

REEL DIMENSIONS

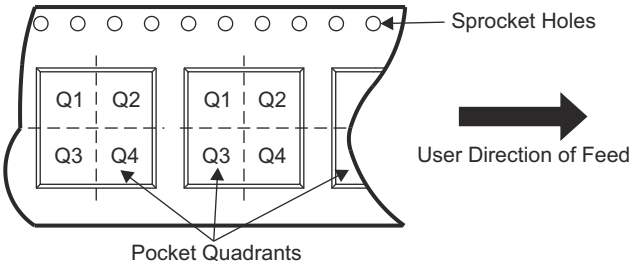


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

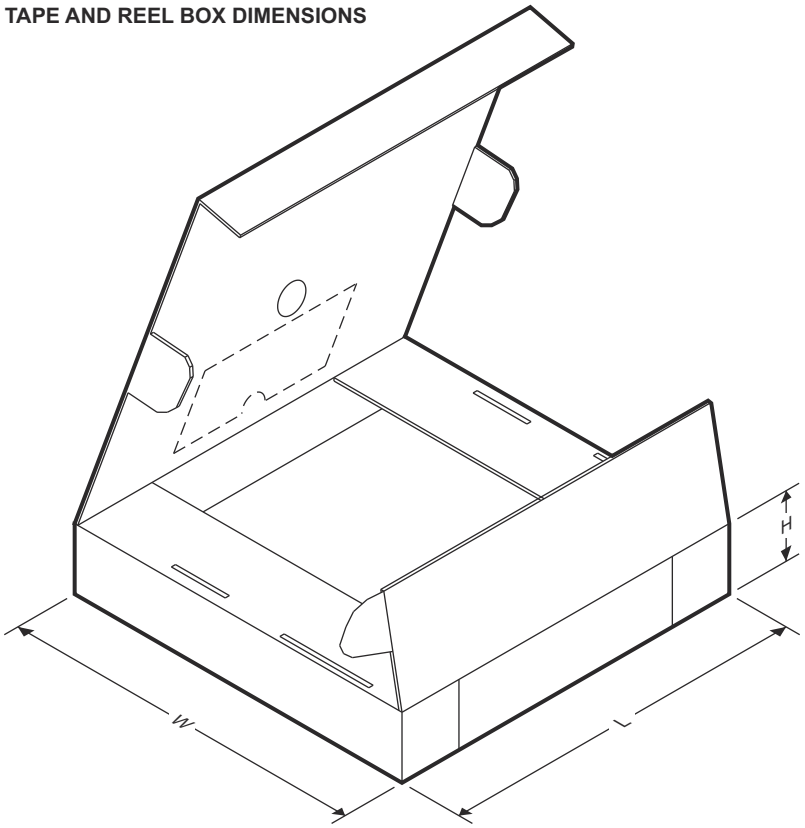


Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMK3H0102RERR	TQFN	RER	16	3000	(TBD)	(TBD)	(TBD)	(TBD)	(TBD)	(TBD)	(TBD)	(TBD)
LMK3H0102RERT	TQFN	RER	16	250	(TBD)	(TBD)	(TBD)	(TBD)	(TBD)	(TBD)	(TBD)	(TBD)

ADVANCE INFORMATION

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMK3H0102RERR	TQFN	RER	16	3000	(TBD)	(TBD)	(TBD)
LMK3H0102RERT	TQFN	RER	16	250	(TBD)	(TBD)	(TBD)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PLMK3H0102RERT	ACTIVE	TQFN	RER	16	250	TBD	Call TI	Call TI	-40 to 85		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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