

LM7171 超高速、大出力電流、電圧帰還型アンプ

1 特長

- 特に記述のない限り標準値
- 使いやすい電圧帰還トポロジ
- 非常に高いスルーレート: 4100V/μs
- 広いユニティ ゲイン帯域幅: 200MHz
- $A_V = +2$ での -3dB 周波数: 220MHz
- 低い消費電流: 6.5mA
- 高いオープンループ ゲイン: 85dB
- 大出力電流: 100mA
- 差動ゲインおよび位相: 0.01%, 0.02°
- ±15V および ±5V での動作を規定

2 アプリケーション

- HDSL および ADSL ドライバ
- マルチメディア放送システム
- プロフェッショナル ビデオ カメラ
- ビデオ アンプ
- コピー機、スキャナ、ファックス
- HDTV アンプ
- パルス アンプおよびピーク検出器
- CATV および光ファイバー信号処理

3 概要

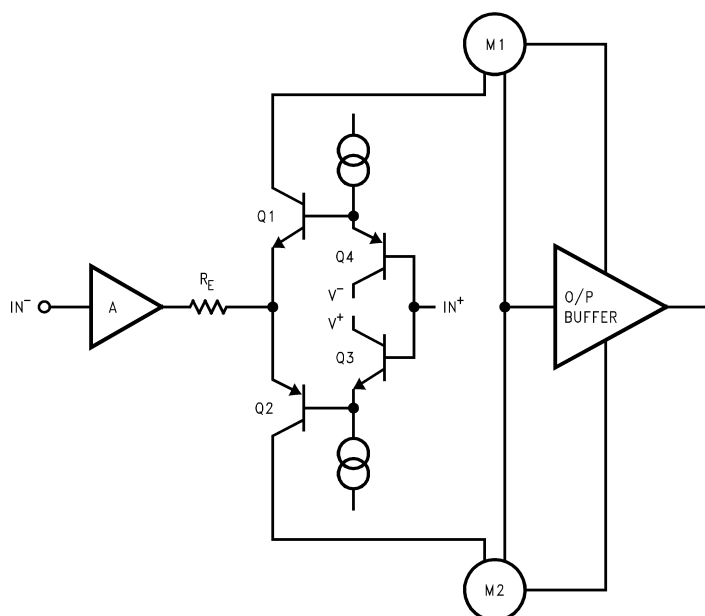
LM7171 は、電流帰還アンプと同様のスルーイング特性を持つ高速電圧帰還アンプですが、従来のすべての電圧帰還アンプ構成に使用できます。LM7171 は +2 倍 または -1 倍 の低いゲインで安定です。LM6171 は、わずか 6.5mA の消費電流で、4100V/μs の高速なスルーレートと 200MHz の広いユニティ ゲイン帯域幅を実現します。LM7171 は、HDSL やパルスアンプなどのビデオおよび高速信号処理アプリケーションに最適です。100mA の出力電流があるので、LM7171 はビデオ配信、トランスドライバ、またはレーザー ダイオードドライバとして使用できます。

±15V 電源での動作により、大きな信号スイングが可能で、ダイナミックレンジと信号対雑音比 (SNR) が向上します。LM7171 は SFDR と THD が低く、ADC/DAC システムに最適です。さらに、LM7171 は、携帯機器のアプリケーション向けに ±5V での動作が規定されています。

パッケージ情報

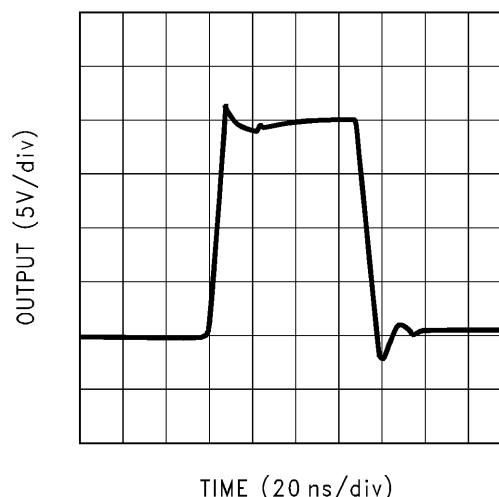
部品番号	パッケージ (1)	パッケージ サイズ (2)
LM7171	D (SOIC, 8)	4.90mm × 6mm
	P (PDIP, 8)	9.81mm × 9.43mm

- 詳細については、[セクション 9](#) を参照してください。
- パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



注: M1 と M2 は電流ミラーです。

概略回路図



大信号パルス応答 $A_V = +2$ 、 $V_S = \pm 15V$



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4 Pin Configuration and Functions

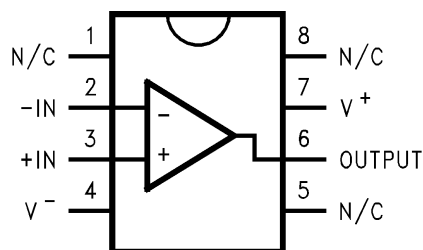


図 4-1. D Package, 8-Pin SOIC (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	NC	—	No connection
2	–IN	Input	Inverting power supply
3	+IN	Input	Noninverting power supply
4	V–	Input	Supply voltage
5	NC	—	No connection
6	OUTPUT	Output	Output
7	V+	Input	Supply voltage
8	NC	—	No connection

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _S	Supply voltage (V ⁺ – V [–])		36	V
V _I	Differential input voltage ⁽²⁾		±10	V
I _{SC}	Output current short to ground ⁽³⁾		Continuous	A
T _J	Junction temperature ⁽⁴⁾		150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Input differential voltage is applied at V_S = ±15V.
- (3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
- (4) The maximum power dissipation is a function of T_{J(MAX)}, R_{θJA}, and T_A. The maximum allowable power dissipation at any ambient temperature is P_D = (T_{J(MAX)} – T_A)/R_{θJA}. All numbers apply for packages soldered directly into a PC board.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001 ⁽¹⁾	±2500	V
		Charged device model (CDM), per ANSI/ESDA/ JEDEC JS-002 ⁽²⁾	±1500	V

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP155 states that 2500V HBM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V _S	Supply voltage	5.5		36	V
T _A	Ambient temperature	–40		85	°C

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LM7171			UNIT
		D (SOIC) A Version	D (SOIC) B Version	P (PDIP)	
		8 PINS	8 PINS	8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	122.5	172	108	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	64.7	62.4	52.4	°C/W
R _{θJB}	Junction-to-board thermal resistance	65.9	55.7	51.9	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	17.6	16.5	6.8	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	65.1	55.1	51.1	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.5 Electrical Characteristics: $\pm 15V$

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OS}	Input offset voltage	LM7171A			0.2	1	mV
			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$			4	
		LM7171B			0.2	3	
			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$			7	
TCV_{OS}	Input offset voltage average drift				35		$\mu\text{V}/^\circ\text{C}$
I_B	Input bias current				2.7	10	μA
			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$			12	
I_{OS}	Input offset current				0.1	4	μA
			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$			6	
R_{IN}	Input resistance	Common mode			320		M Ω
		Differential mode			18		
R_O	Open-loop output resistance				19		Ω
CMRR	Common-mode rejection ratio	LM7171A	$V_{CM} = \pm 10V$	85	105		dB
			$V_{CM} = \pm 10V$, $T_A = -40^\circ\text{C to } +85^\circ\text{C}$	80			
		LM7171B	$V_{CM} = \pm 10V$	75	105		
			$V_{CM} = \pm 10V$, $T_A = -40^\circ\text{C to } +85^\circ\text{C}$	70			
PSRR	Power supply rejection ratio	LM7171A	$V_S = \pm 15V$	85	90		dB
			$V_S = \pm 15V$, $T_A = -40^\circ\text{C to } +85^\circ\text{C}$	80			
		LM7171B	$V_S = \pm 15V$				
			$V_S = \pm 15V$, $T_A = -40^\circ\text{C to } +85^\circ\text{C}$				
V_{CM}	Input common-mode voltage	CMRR > 60dB			± 13.35		V
A_v	Large-signal voltage gain	LM7171A	$R_L = 1k\Omega$, $V_{OUT} = \pm 5V$	80	85		dB
			$R_L = 1k\Omega$, $V_{OUT} = \pm 5V$, $T_A = -40^\circ\text{C to } +85^\circ\text{C}$	75			
			$R_L = 100\Omega$, $V_{OUT} = \pm 5V$	75	81		
			$R_L = 100\Omega$, $V_{OUT} = \pm 5V$, $T_A = -40^\circ\text{C to } +85^\circ\text{C}$	70			
		LM7171B	$R_L = 1k\Omega$, $V_{OUT} = \pm 5V$	75	85		
			$R_L = 1k\Omega$, $V_{OUT} = \pm 5V$, $T_A = -40^\circ\text{C to } +85^\circ\text{C}$	70			
			$R_L = 100\Omega$, $V_{OUT} = \pm 5V$	70	81		
			$R_L = 100\Omega$, $V_{OUT} = \pm 5V$, $T_A = -40^\circ\text{C to } +85^\circ\text{C}$	66			
V_O	Output swing	$R_L = 1k\Omega$		13	13.3		V
			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	12.7			
		$R_L = 1k\Omega$		-13	-13.2		
			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	-12.7			
		$R_L = 100\Omega$		10.5	11.8		
			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	9.5			
		$R_L = 100\Omega$		-9.5	-10.5		
			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	-9			

5.5 Electrical Characteristics: $\pm 15V$ (続き)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Output current (open loop)	Sourcing, $R_L = 100\Omega$	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	105	118		mA
				95			
		Sinking, $R_L = 100\Omega$	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	95	105		
				90			
	Output current (in linear region)	Sourcing, $R_L = 100\Omega$			100		mA
		Sinking, $R_L = 100\Omega$			100		
I_{SC}	Output short-circuit current	Sourcing			140		
		Sinking			135		
I_S	Supply current				6.5	8.5	
						9.5	
SR	Slew rate	$A_V = +2$, $V_{IN} = 13V_{PP}$			4100		V/ μs
		$A_V = +2$, $V_{IN} = 10V_{PP}$			3100		
	Unity-gain bandwidth	LM7171A			160		MHz
		LM7171B			200		
	-3dB frequency	$A_V = +2$			220		MHz
Φ_m	Phase margin				50		Deg
t_s	Settling time (0.1%)	$A_V = -1$, $V_{OUT} = \pm 5V$, $R_L = 500\Omega$	LM7171A		16		ns
			LM7171B		42		ns
t_p	Propagation delay	$A_V = -2$, $V_{IN} = \pm 1V$, $R_L = 500\Omega$			5		ns
HD2	Second harmonic distortion	LM7171A	$f_{IN} = 10\text{kHz}$		-123		dBc
			$f_{IN} = 5\text{MHz}$		-75		
		LM7171B	$f_{IN} = 10\text{kHz}$		-110		
			$f_{IN} = 5\text{MHz}$		-75		
HD3	Third harmonic distortion	LM7171A	$f_{IN} = 10\text{kHz}$		-133		dBc
			$f_{IN} = 5\text{MHz}$		-88		
		LM7171B	$f_{IN} = 10\text{kHz}$		-115		
			$f_{IN} = 5\text{MHz}$		-55		
e_n	Input-referred voltage noise	$f = 10\text{kHz}$	LM7171A		8.5		nV/ $\sqrt{\text{Hz}}$
			LM7171B		14		
i_n	Input-referred current noise	$f = 10\text{kHz}$	LM7171A		1		pA/ $\sqrt{\text{Hz}}$
			LM7171B		1.5		

5.6 Electrical Characteristics: $\pm 5V$

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OS}	Input offset voltage	LM7171A			0.3	1.5	mV
			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$			4	
		LM7171B			0.3	3.5	
			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$			7	
TCV_{OS}	Input offset voltage average drift				35		$\mu\text{V}/^\circ\text{C}$
I_B	Input bias current				3.3	10	μA
		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$				12	
I_{OS}	Input offset current				0.1	4	μA
		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$				6	
R_{IN}	Input resistance	Common mode			250		M Ω
		Differential mode			18		
R_O	Open-loop output resistance				18		Ω
CMRR	Common-mode rejection ratio	LM7171A	$V_{CM} = \pm 2.5V$	80	104		dB
			$V_{CM} = \pm 2.5V, T_A = -40^\circ\text{C to } +85^\circ\text{C}$	75			
		LM7171B	$V_{CM} = \pm 2.5V$	70	104		
			$V_{CM} = \pm 2.5V, T_A = -40^\circ\text{C to } +85^\circ\text{C}$	65			
PSRR	Power supply rejection ratio	LM7171A	$V_S = \pm 5V$	85	90		dB
			$V_S = \pm 5V, T_A = -40^\circ\text{C to } +85^\circ\text{C}$	80			
		LM7171B	$V_S = \pm 5V$	75	90		
			$V_S = \pm 5V, T_A = -40^\circ\text{C to } +85^\circ\text{C}$	70			
V_{CM}	Input common-mode voltage range	CMRR > 60dB			± 3.2		V
A_v	Large-signal voltage gain	LM7171A	$R_L = 1k\Omega, V_{OUT} = \pm 1V$	75	78		dB
			$R_L = 1k\Omega, V_{OUT} = \pm 1V, T_A = -40^\circ\text{C to } +85^\circ\text{C}$	70			
			$R_L = 100\Omega, V_{OUT} = \pm 1V$	72	76		
			$R_L = 100\Omega, V_{OUT} = \pm 1V, T_A = -40^\circ\text{C to } +85^\circ\text{C}$	67			
		LM7171B	$R_L = 1k\Omega, V_{OUT} = \pm 1V$	70	78		
			$R_L = 1k\Omega, V_{OUT} = \pm 1V, T_A = -40^\circ\text{C to } +85^\circ\text{C}$	65			
			$R_L = 100\Omega, V_{OUT} = \pm 1V$	68	76		
			$R_L = 100\Omega, V_{OUT} = \pm 1V, T_A = -40^\circ\text{C to } +85^\circ\text{C}$	63			
V_O	Output swing	$R_L = 1k\Omega$		3.2	3.4		V
				-3.2	-3.4		
			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	3			
				-3			
		$R_L = 100\Omega$		2.9	3.1		
				-2.9	-3		
			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	2.8			
				-2.8			

5.6 Electrical Characteristics: $\pm 5V$ (続き)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Output current (open loop)	Sourcing, R _L = 100Ω		29	31	mA	
			T _A = −40°C to +85°C	28			
		Sinking, R _L = 100Ω		29	30		
			T _A = −40°C to +85°C	28			
	Output current (in linear region)	Sourcing, R _L = 100Ω		30		mA	
		Sinking, R _L = 100Ω		31			
I _{SC}	Output short-circuit current	Sourcing		135		mA	
		Sinking		100			
I _S	Supply current			6.2	8	mA	
		T _A = −40°C to +85°C		9			
SR	Slew rate	A _V = +2, V _{IN} = 3.2V _{PP}	LM7171A	1200		V/μs	
			LM7171B	950			
	Unity-gain bandwidth	LM7171A		125		MHz	
		LM7171B		125			
	−3dB frequency	A _V = +2	LM7171A	140		MHz	
			LM7171B	140			
φ _m	Phase margin	LM7171A		68		Deg	
		LM7171B		57			
t _s	Settling time (0.1%)	A _V = −1, V _{OUT} = ±1V, R _L = 500Ω	LM7171A	15		ns	
			LM7171B	56			
t _p	Propagation delay	A _V = −2, V _{IN} = ±1V, R _L = 500Ω	LM7171A	2.5		ns	
			LM7171B	6			
HD2	Second harmonic distortion	LM7171A	f _{IN} = 10kHz	−125		dBc	
			f _{IN} = 5MHz	−72			
		LM7171B	f _{IN} = 10kHz	−102			
			f _{IN} = 5MHz	−70			
HD3	Third harmonic distortion	LM7171A	f _{IN} = 10kHz	−129		dBc	
			f _{IN} = 5MHz	−81			
		LM7171B	f _{IN} = 10kHz	−110			
			f _{IN} = 5MHz	−51			
e _n	Input-referred voltage noise	f = 10kHz	LM7171A	8.5		nV/√Hz	
			LM7171B	14			
i _n	Input-referred current noise	f = 10kHz	LM7171A	1		pA/√Hz	
			LM7171B	1.8			

5.7 Typical Characteristics: LM7171A

at $T_A = 25^\circ\text{C}$ (unless otherwise noted)

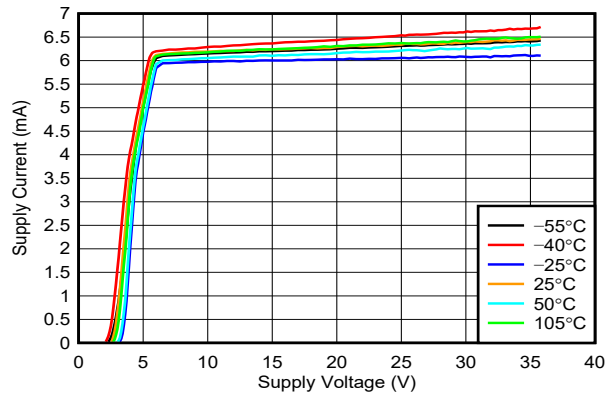


図 5-1. Supply Current vs Supply Voltage

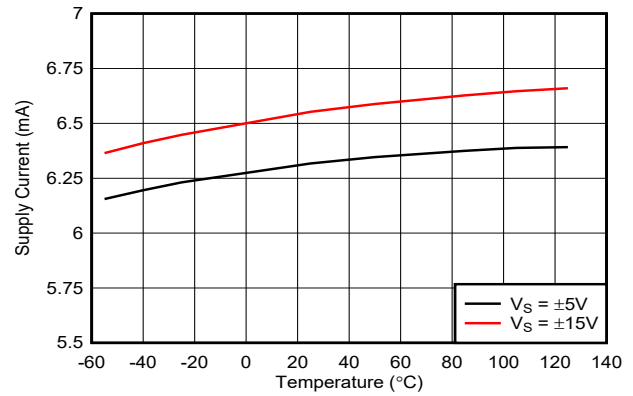


図 5-2. Supply Current vs Temperature

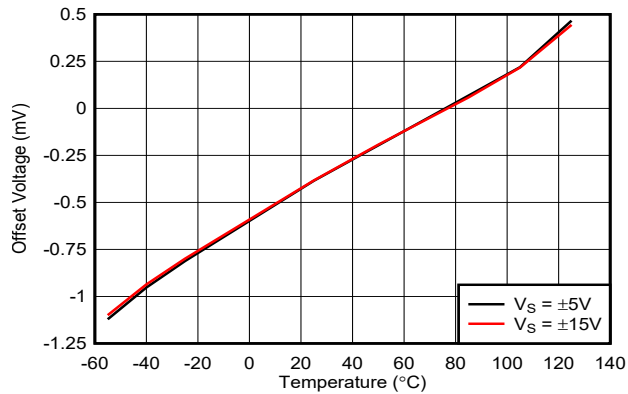


図 5-3. Input Offset Voltage vs Temperature

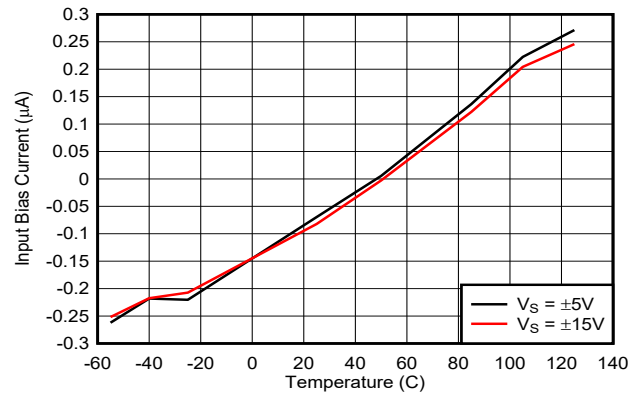


図 5-4. Input Bias Current vs Temperature

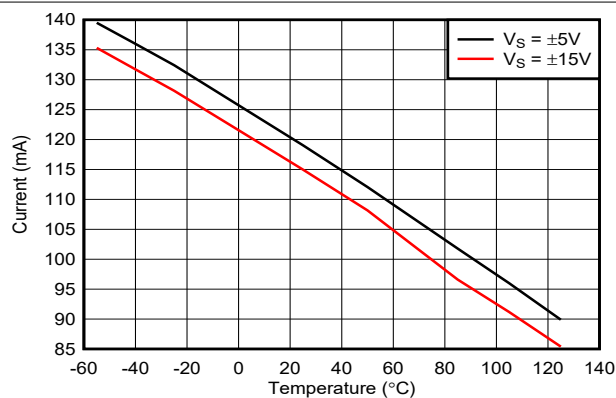


図 5-5. Short Circuit Current vs Temperature (Sourcing)

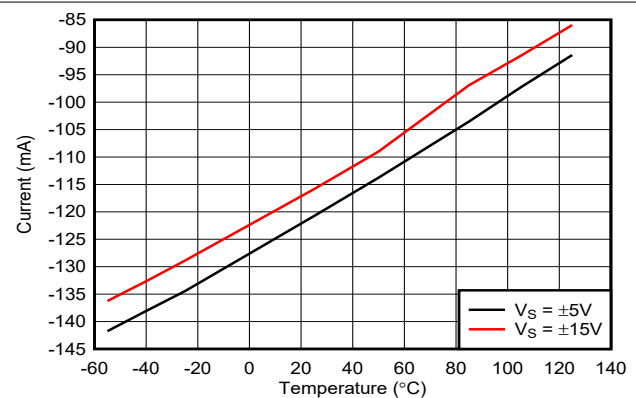


図 5-6. Short Circuit Current vs Temperature (Sinking)

5.7 Typical Characteristics: LM7171A (continued)

at $T_A = 25^\circ\text{C}$ (unless otherwise noted)

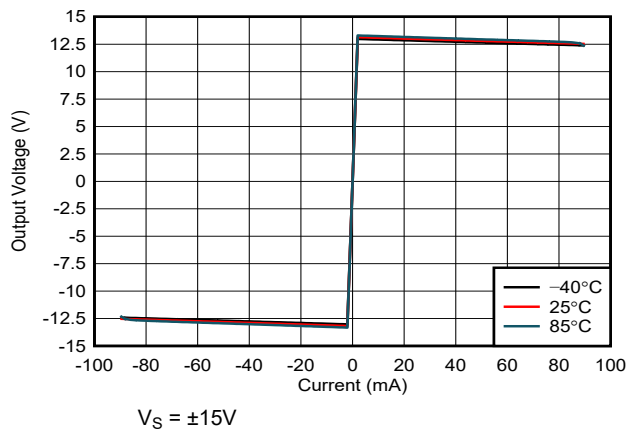


図 5-7. Output Voltage vs Output Current

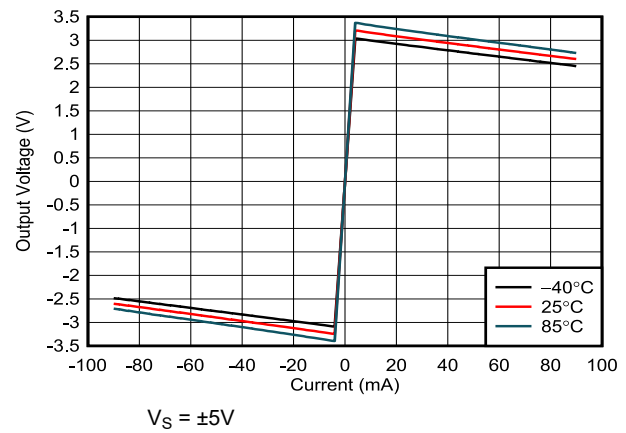


図 5-8. Output Voltage vs Output Current

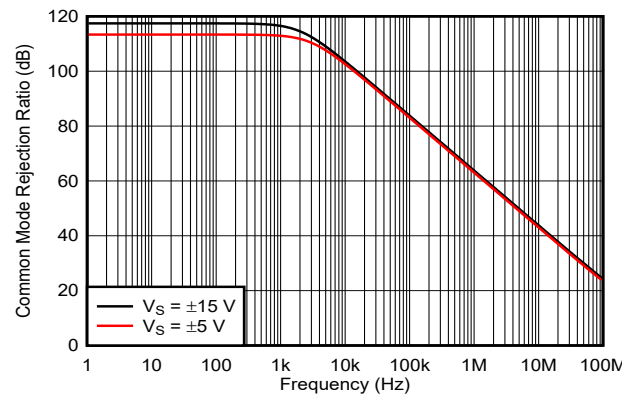


図 5-9. CMRR vs Frequency

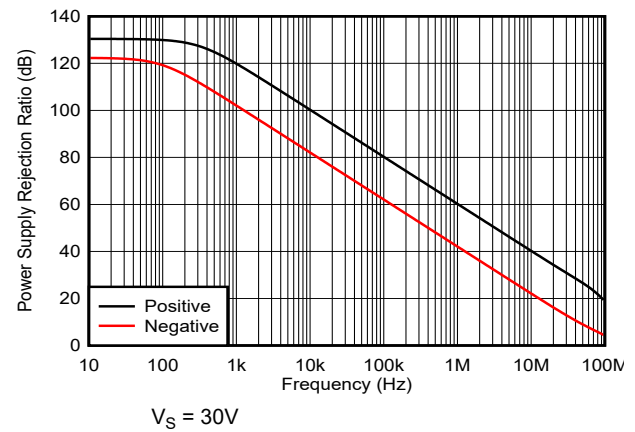


図 5-10. PSRR vs Frequency

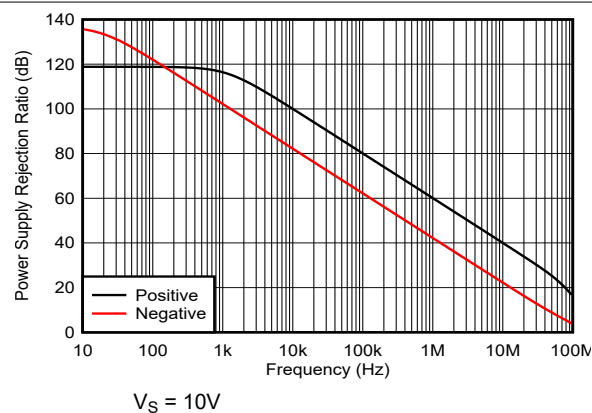


図 5-11. PSRR vs Frequency

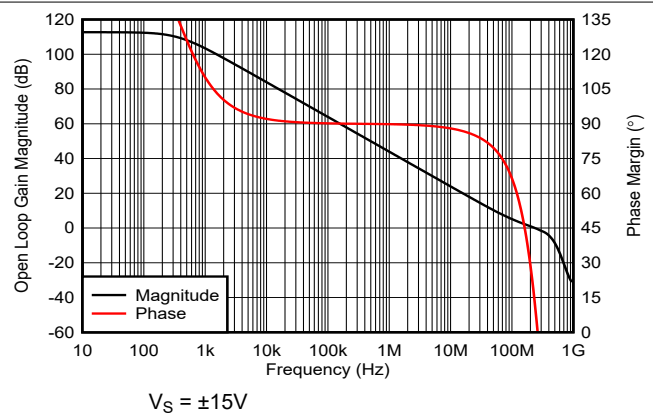


図 5-12. Open Loop Frequency Response

5.7 Typical Characteristics: LM7171A (continued)

at $T_A = 25^\circ\text{C}$ (unless otherwise noted)

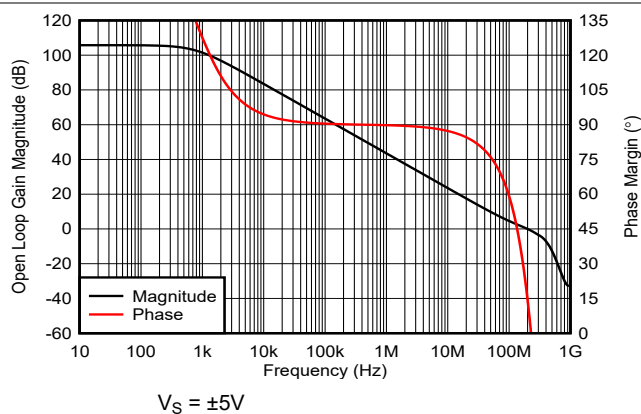


图 5-13. Open Loop Frequency Response

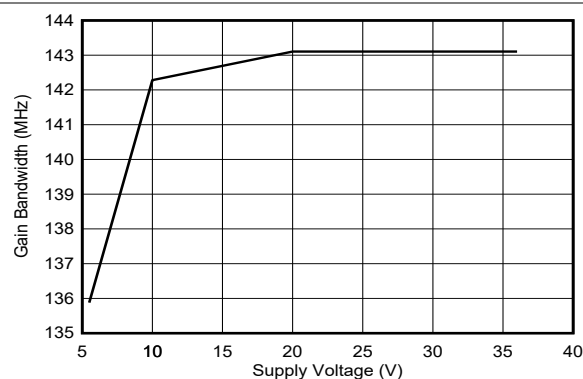


图 5-14. Gain-Bandwidth Product vs Supply Voltage

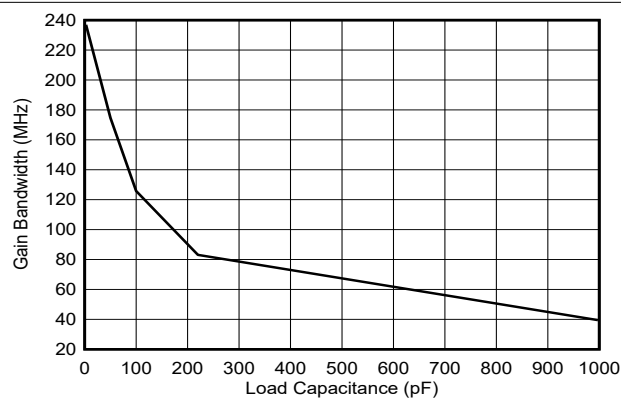


图 5-15. Gain-Bandwidth Product vs Load Capacitance

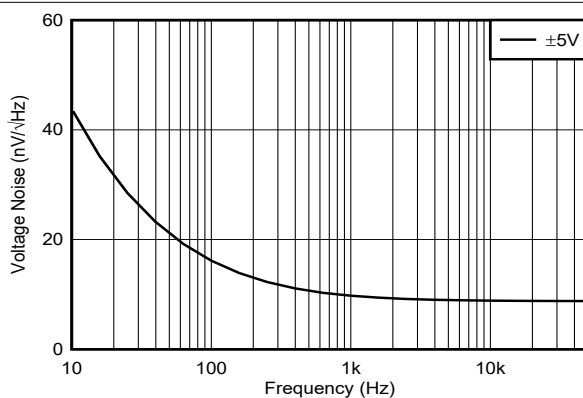


图 5-16. Input Voltage Noise vs Frequency

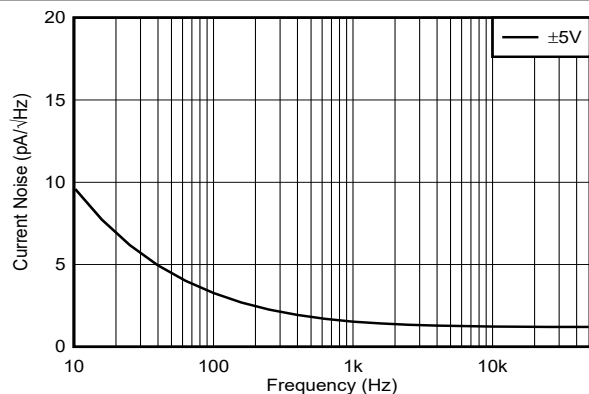


图 5-17. Input Current Noise vs Frequency

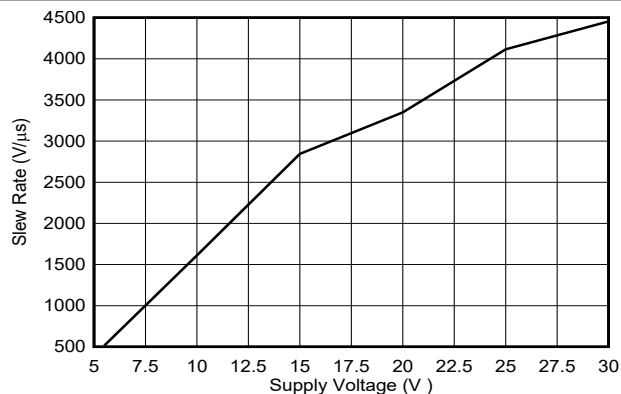


图 5-18. Slew Rate vs Supply Voltage

5.7 Typical Characteristics: LM7171A (continued)

at $T_A = 25^\circ\text{C}$ (unless otherwise noted)

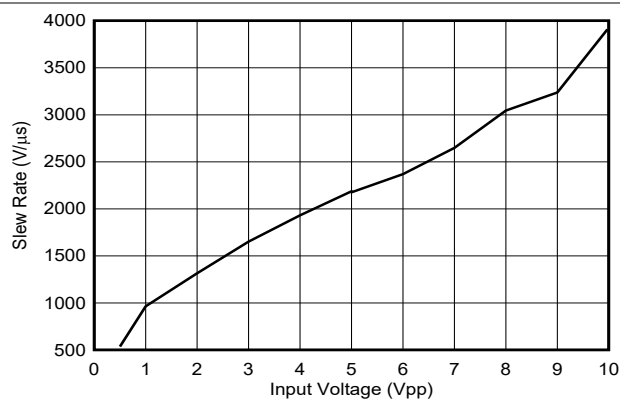


FIG 5-19. Slew Rate vs Input Voltage

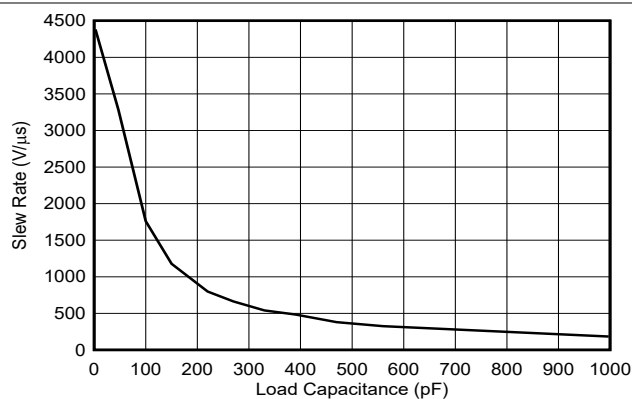
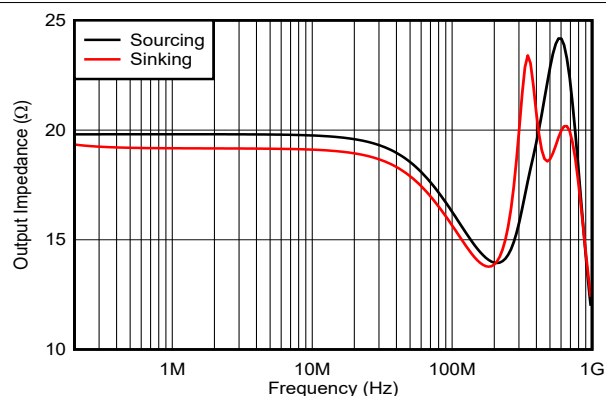
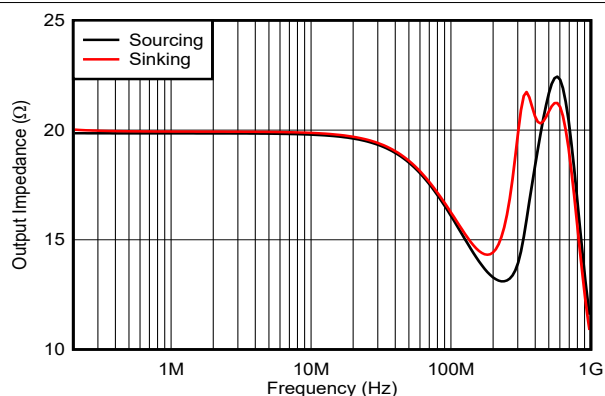


FIG 5-20. Slew Rate vs Load Capacitance



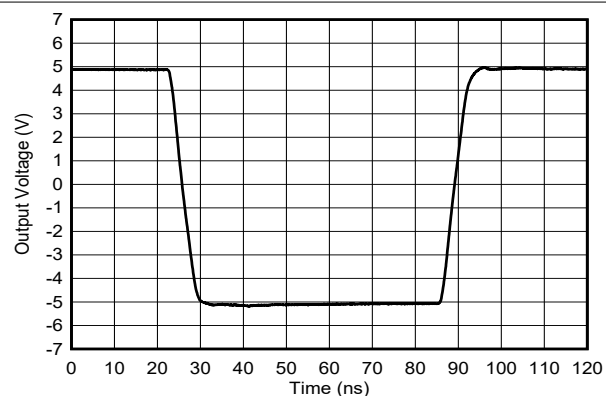
$V_S = \pm 15\text{V}$

FIG 5-21. Open Loop Output Impedance vs Frequency



$V_S = \pm 5\text{V}$

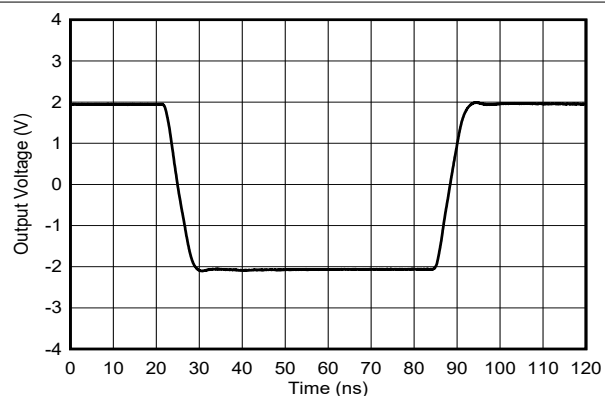
FIG 5-22. Open Loop Output Impedance vs Frequency



$A_V = -1$

$V_S = \pm 15\text{V}$

FIG 5-23. Large-Signal Pulse Response



$A_V = -1$

$V_S = \pm 5\text{V}$

FIG 5-24. Large-Signal Pulse Response

5.7 Typical Characteristics: LM7171A (continued)

at $T_A = 25^\circ\text{C}$ (unless otherwise noted)

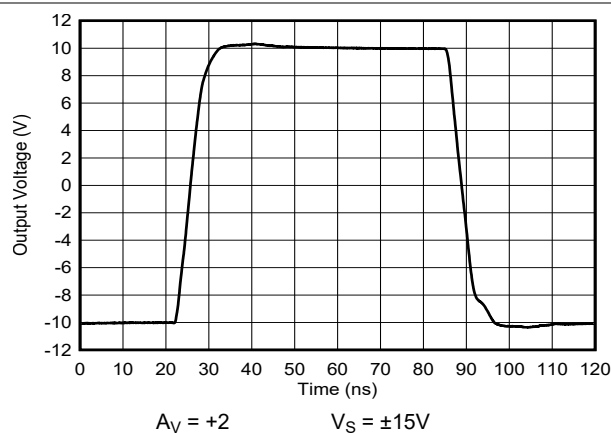


図 5-25. Large-Signal Pulse Response

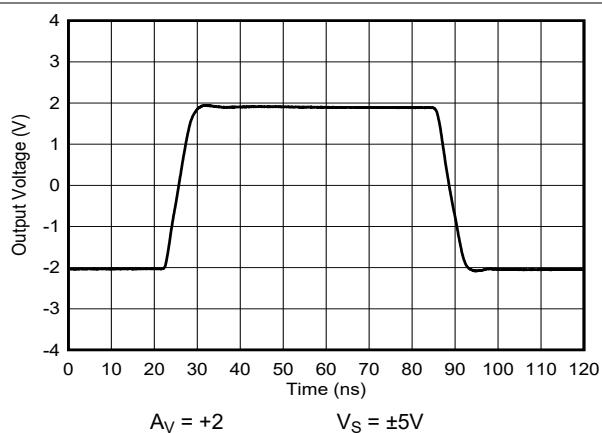


図 5-26. Large-Signal Pulse Response

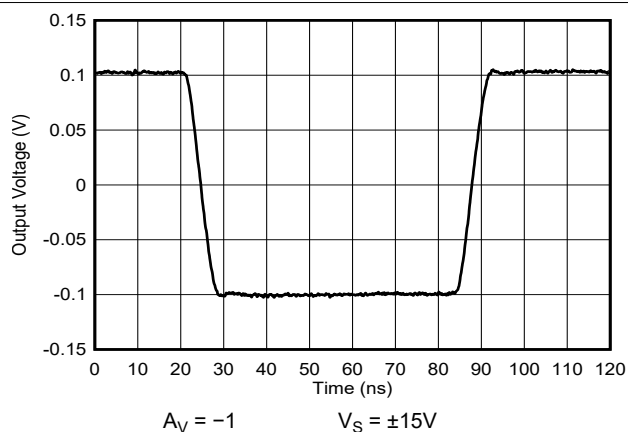


図 5-27. Small-Signal Pulse Response

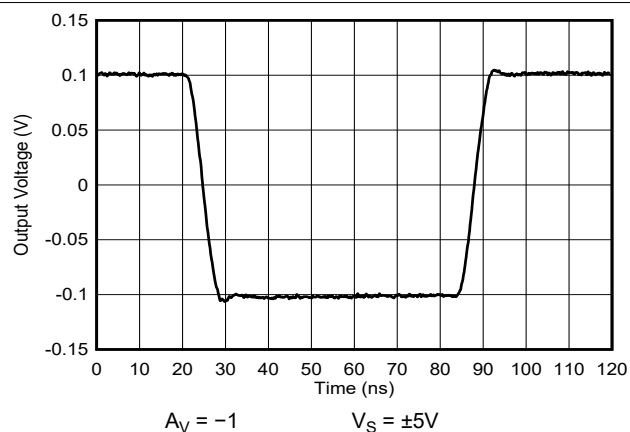


図 5-28. Small-Signal Pulse Response

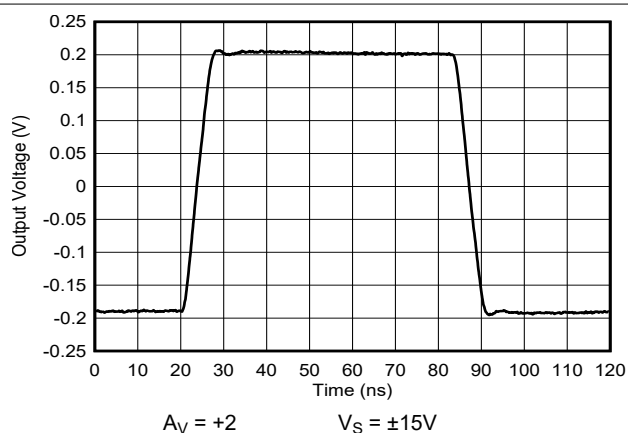


図 5-29. Small-Signal Pulse Response

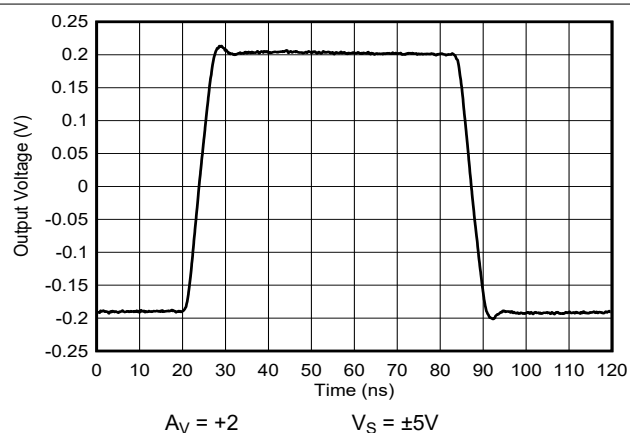
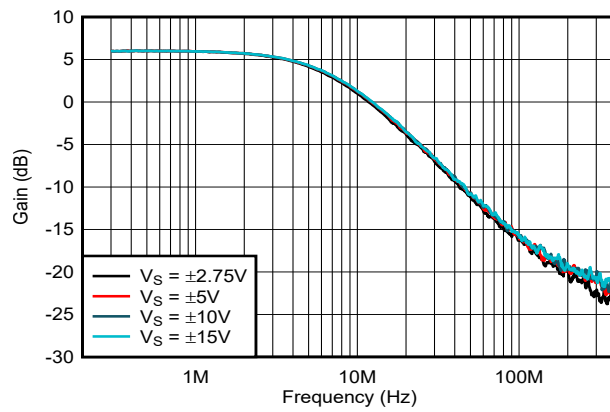


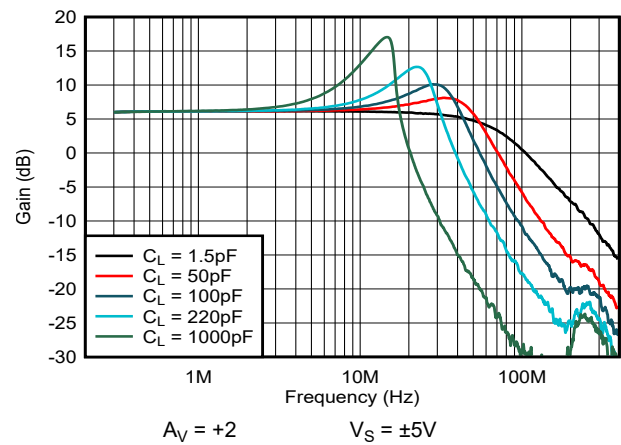
図 5-30. Small-Signal Pulse Response

5.7 Typical Characteristics: LM7171A (continued)

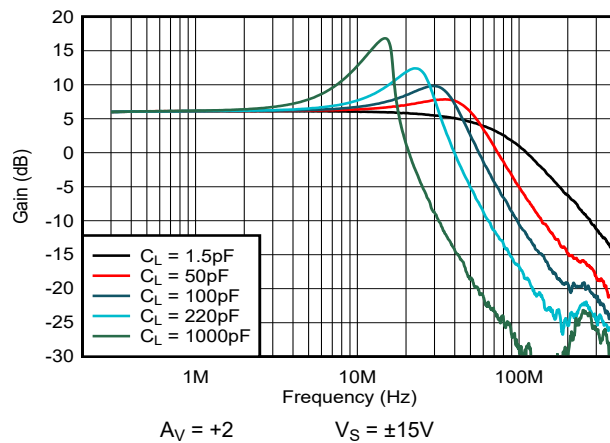
at $T_A = 25^\circ\text{C}$ (unless otherwise noted)



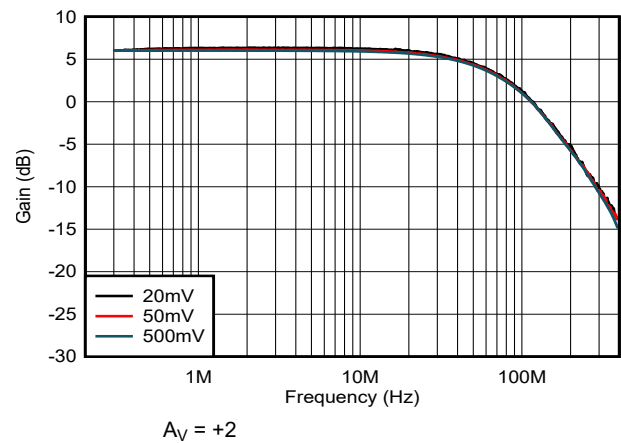
5-31. Closed-Loop Frequency Response vs Supply Voltage



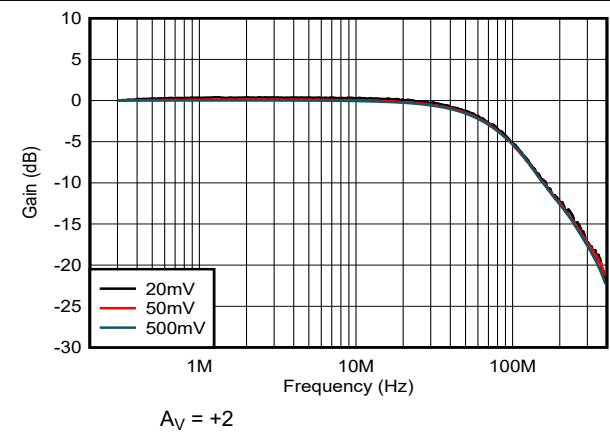
5-32. Closed-Loop Frequency Response vs Capacitive Load



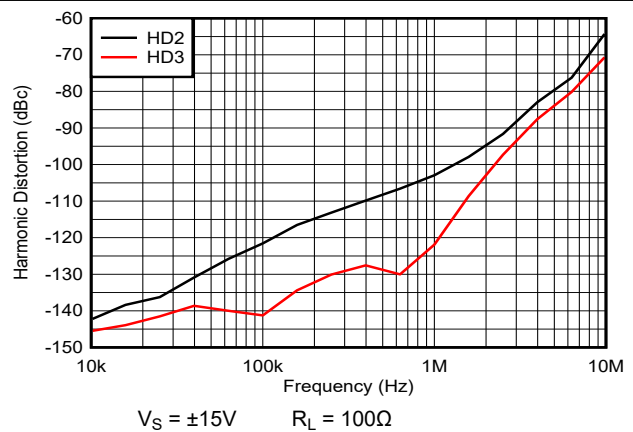
5-33. Closed-Loop Frequency Response vs Capacitive Load



5-34. Closed-Loop Frequency Response vs Input Signal Level



5-35. Closed-Loop Frequency Response vs Input Signal Level



5-36. Total Harmonic Distortion vs Frequency

5.7 Typical Characteristics: LM7171A (continued)

at $T_A = 25^\circ\text{C}$ (unless otherwise noted)

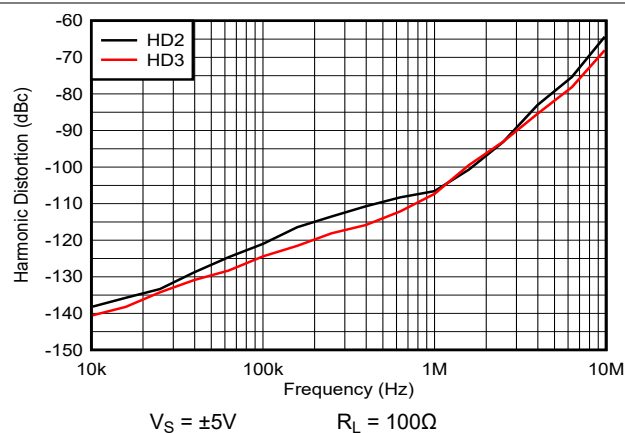


图 5-37. Total Harmonic Distortion vs Frequency

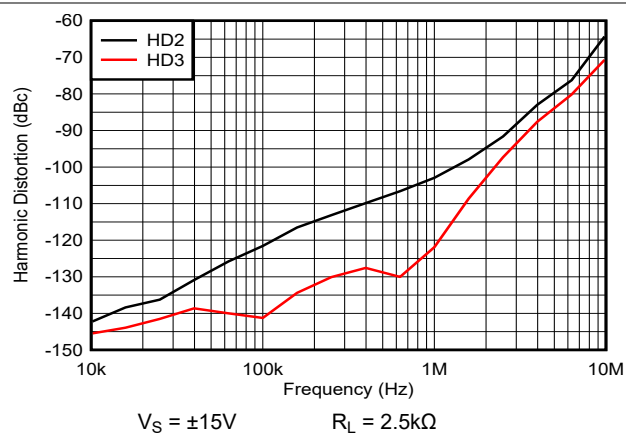


图 5-38. Harmonic Distortion vs Frequency

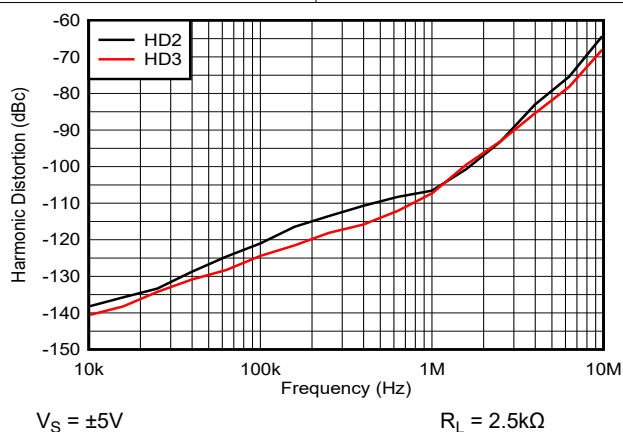
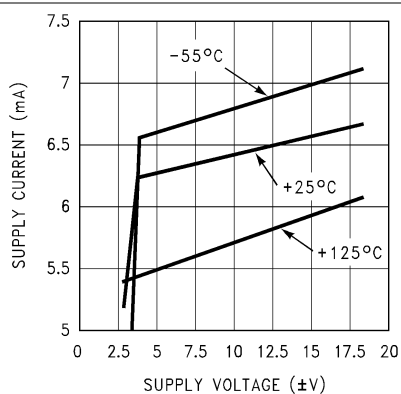


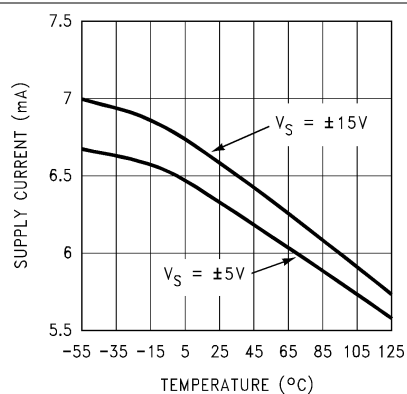
图 5-39. Harmonic Distortion vs Frequency

5.8 Typical Characteristics: LM7171B

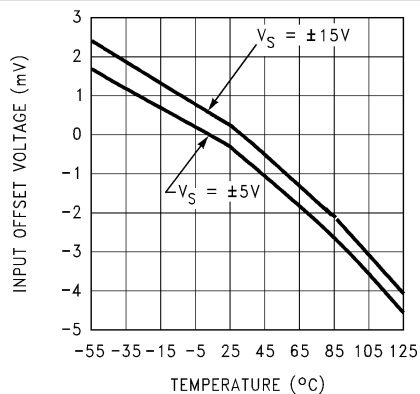
at $T_A = 25^\circ\text{C}$ (unless otherwise noted)



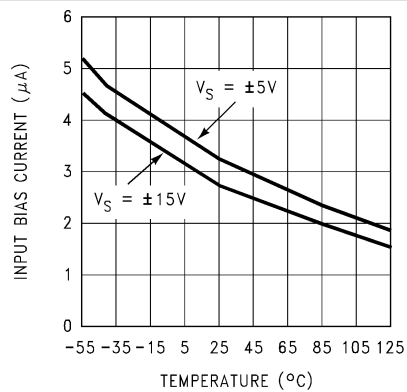
5-40. Supply Current vs Supply Voltage



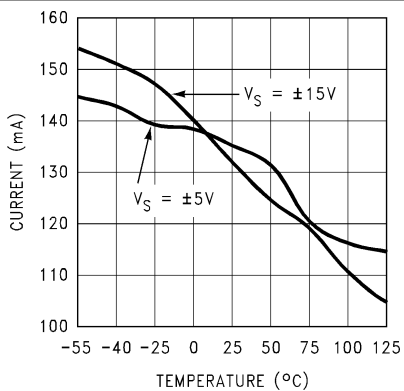
5-41. Supply Current vs Temperature



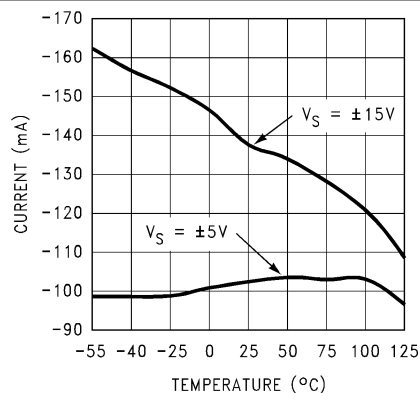
5-42. Input Offset Voltage vs Temperature



5-43. Input Bias Current vs Temperature



5-44. Short Circuit Current vs Temperature (Sourcing)



5-45. Short Circuit Current vs Temperature (Sinking)

5.8 Typical Characteristics: LM7171B (continued)

at $T_A = 25^\circ\text{C}$ (unless otherwise noted)

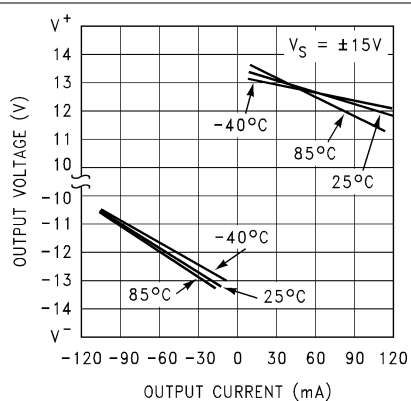


FIG 5-46. Output Voltage vs Output Current

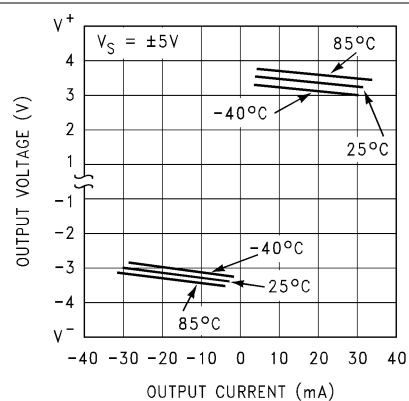


FIG 5-47. Output Voltage vs Output Current

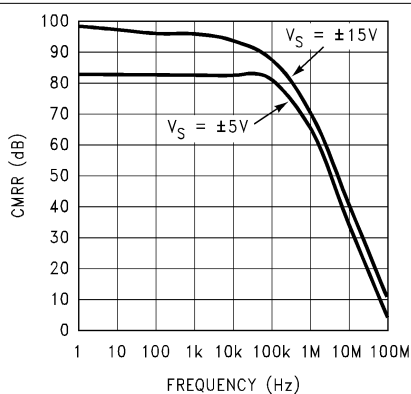


FIG 5-48. CMRR vs Frequency

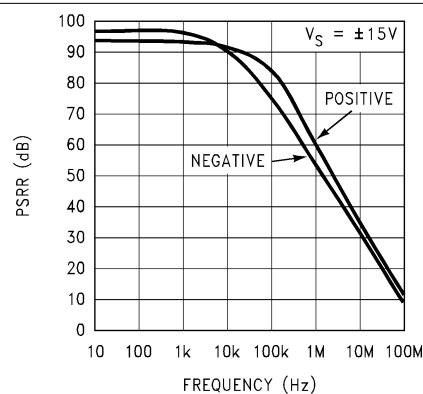


FIG 5-49. PSRR vs Frequency

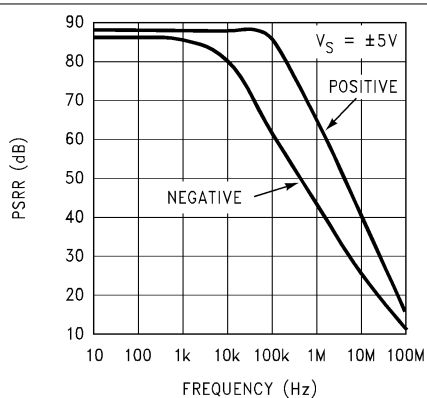


FIG 5-50. PSRR vs Frequency

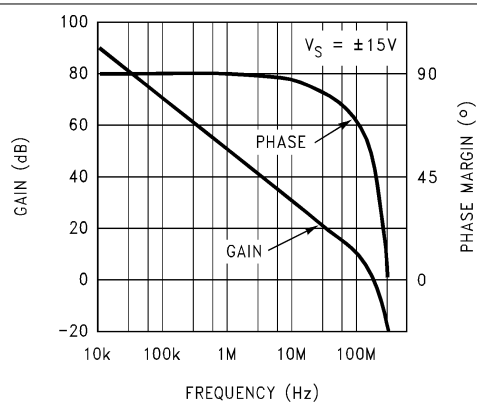


FIG 5-51. Open Loop Frequency Response

5.8 Typical Characteristics: LM7171B (continued)

at $T_A = 25^\circ\text{C}$ (unless otherwise noted)

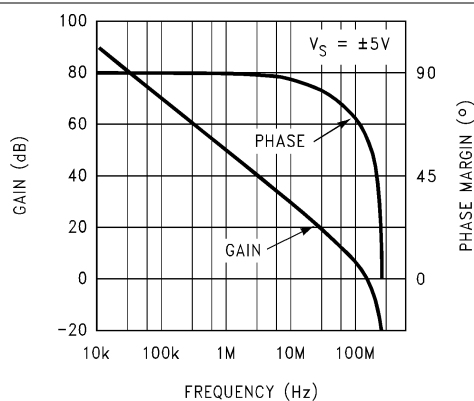


Figure 5-52. Open Loop Frequency Response

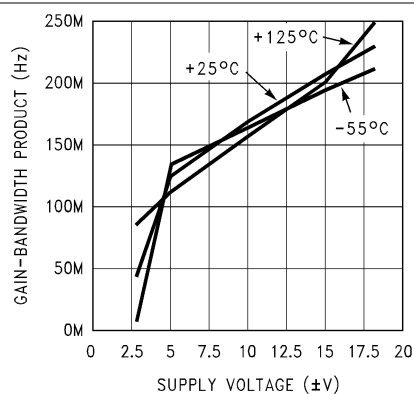


Figure 5-53. Gain-Bandwidth Product vs Supply Voltage

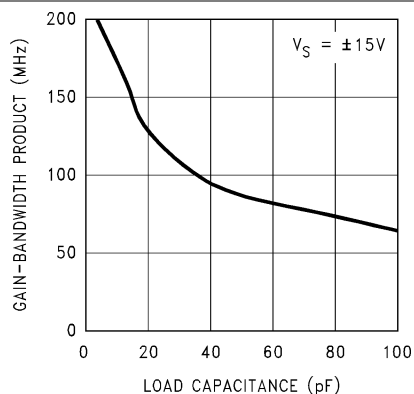


Figure 5-54. Gain-Bandwidth Product vs Load Capacitance

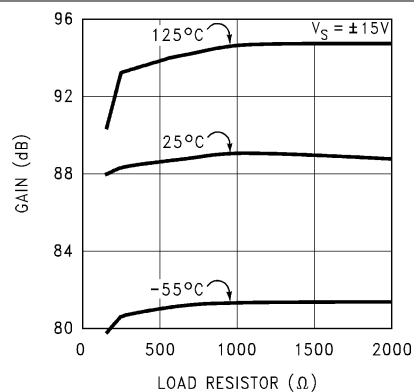


Figure 5-55. Large Signal Voltage Gain vs Load

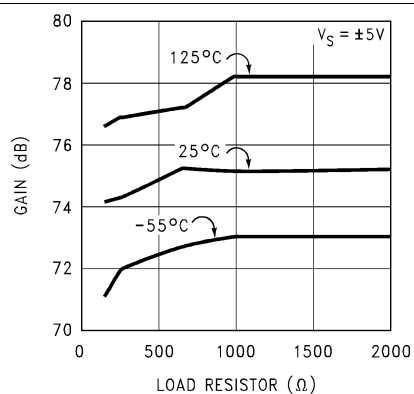


Figure 5-56. Large Signal Voltage Gain vs Load

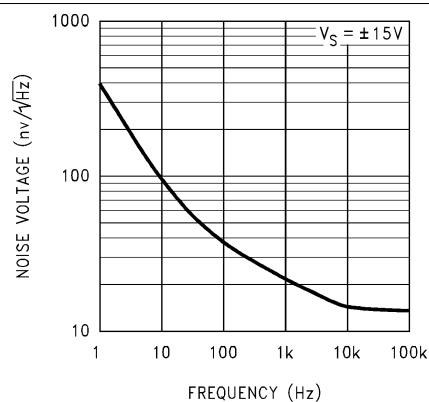


Figure 5-57. Input Voltage Noise vs Frequency

5.8 Typical Characteristics: LM7171B (continued)

at $T_A = 25^\circ\text{C}$ (unless otherwise noted)

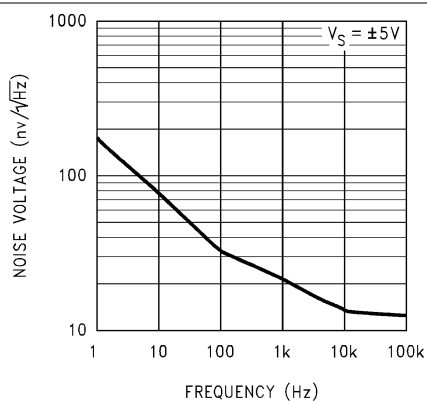


FIG 5-58. Input Voltage Noise vs Frequency

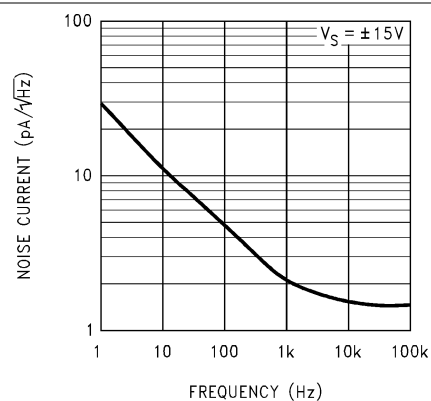


FIG 5-59. Input Current Noise vs Frequency

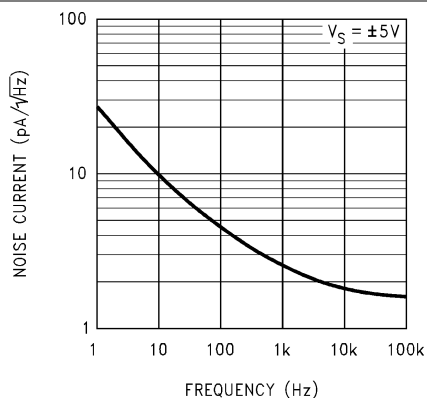


FIG 5-60. Input Current Noise vs Frequency

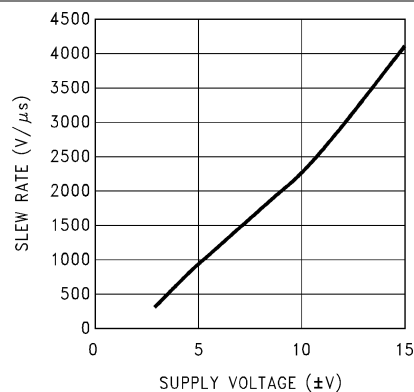


FIG 5-61. Slew Rate vs Supply Voltage

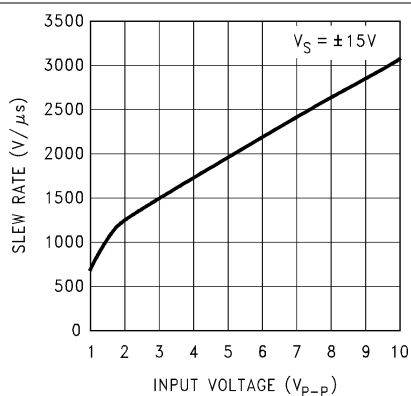


FIG 5-62. Slew Rate vs Input Voltage

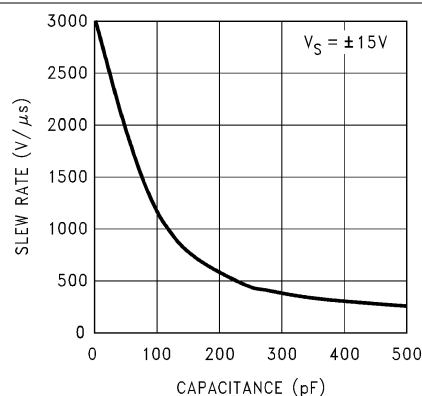


FIG 5-63. Slew Rate vs Load Capacitance

5.8 Typical Characteristics: LM7171B (continued)

at $T_A = 25^\circ\text{C}$ (unless otherwise noted)

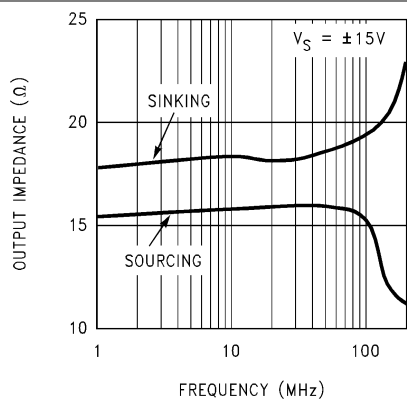


FIG 5-64. Open Loop Output Impedance vs Frequency

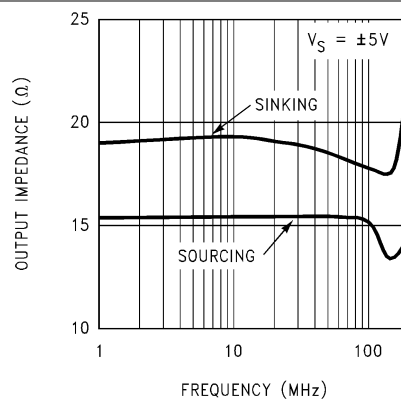


FIG 5-65. Open Loop Output Impedance vs Frequency

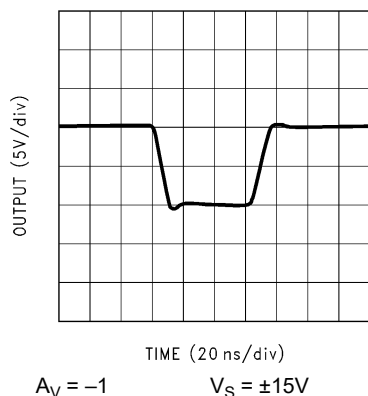


FIG 5-66. Large-Signal Pulse Response

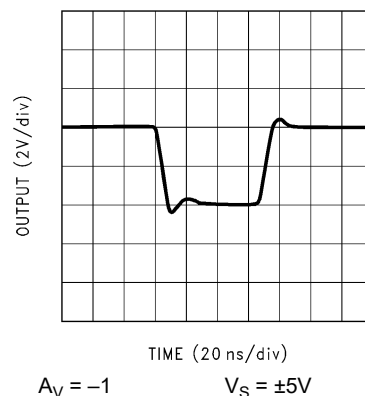


FIG 5-67. Large-Signal Pulse Response

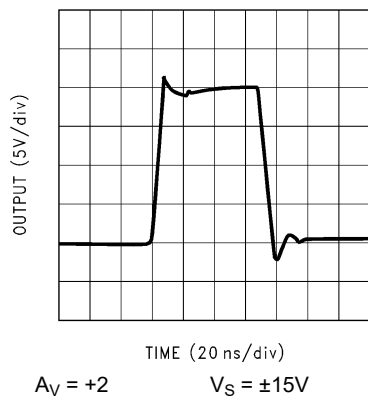


FIG 5-68. Large-Signal Pulse Response

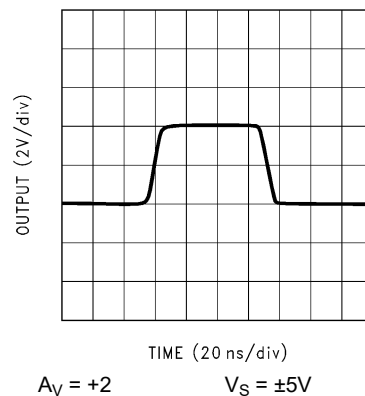


FIG 5-69. Large-Signal Pulse Response

5.8 Typical Characteristics: LM7171B (continued)

at $T_A = 25^\circ\text{C}$ (unless otherwise noted)

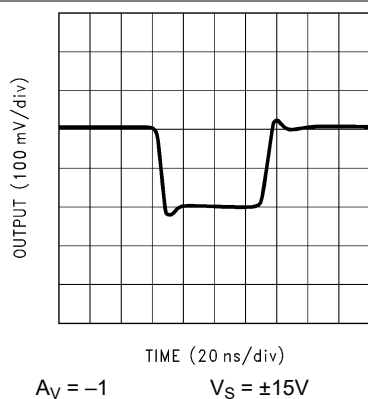


图 5-70. Small-Signal Pulse Response

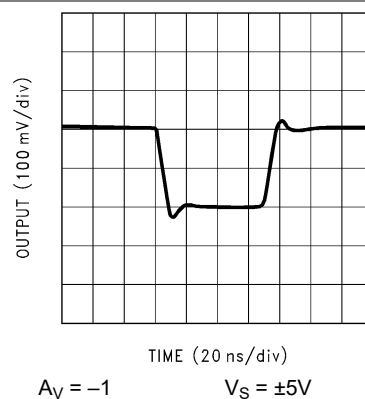


图 5-71. Small-Signal Pulse Response

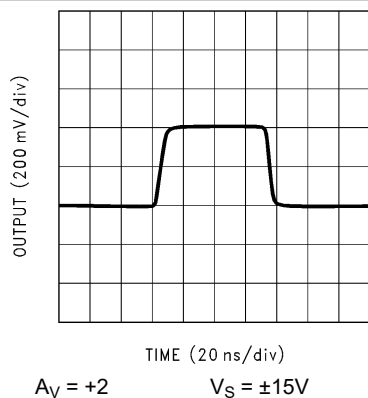


图 5-72. Small-Signal Pulse Response

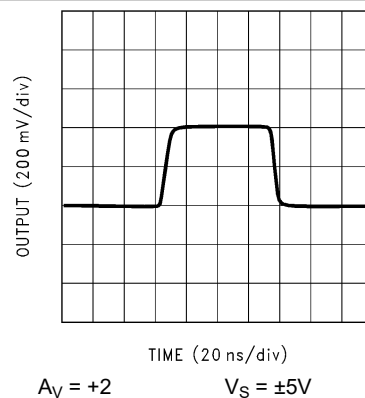


图 5-73. Small-Signal Pulse Response

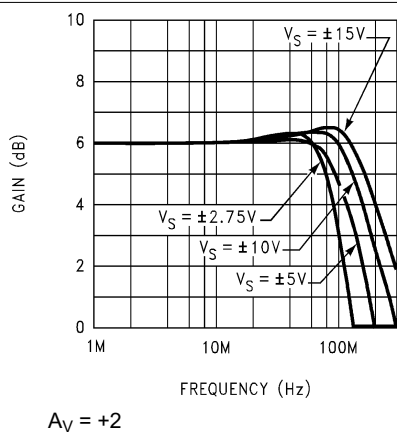


图 5-74. Closed-Loop Frequency Response vs Supply Voltage

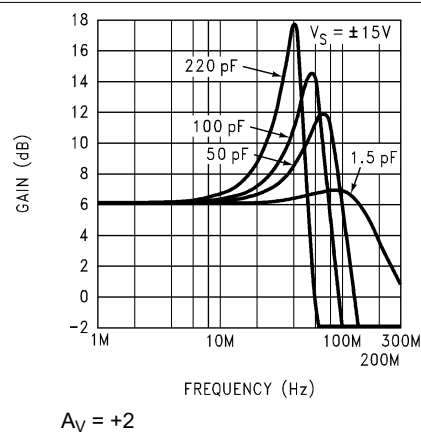


图 5-75. Closed-Loop Frequency Response vs Capacitive Load

5.8 Typical Characteristics: LM7171B (continued)

at $T_A = 25^\circ\text{C}$ (unless otherwise noted)

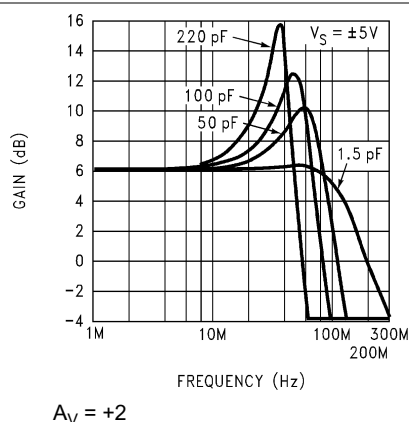


FIG 5-76. Closed-Loop Frequency Response vs Capacitive Load

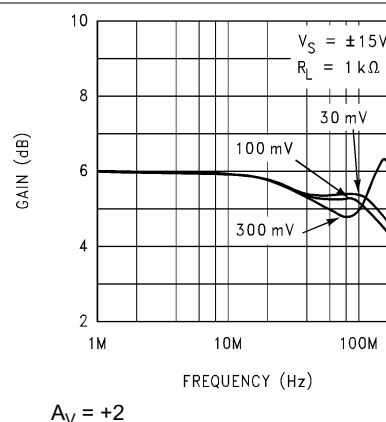


FIG 5-77. Closed-Loop Frequency Response vs Input Signal Level

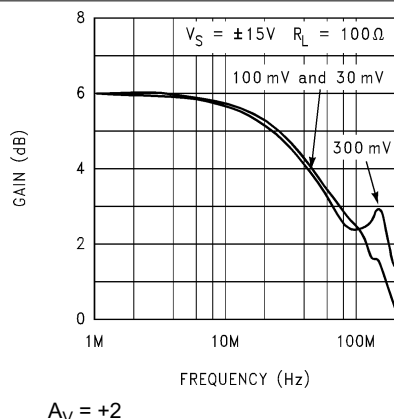


FIG 5-78. Closed-Loop Frequency Response vs Input Signal Level

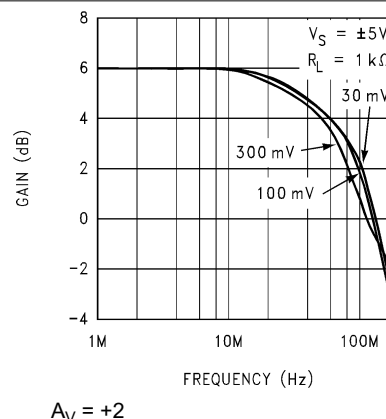


FIG 5-79. Closed-Loop Frequency Response vs Input Signal Level

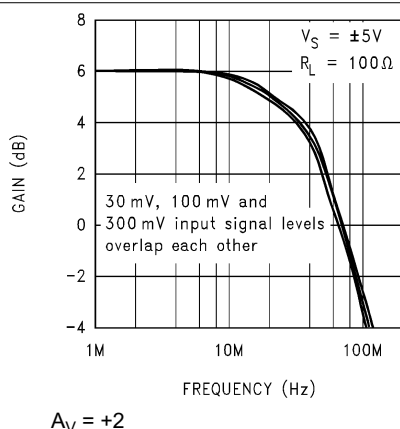


FIG 5-80. Closed-Loop Frequency Response vs Input Signal Level

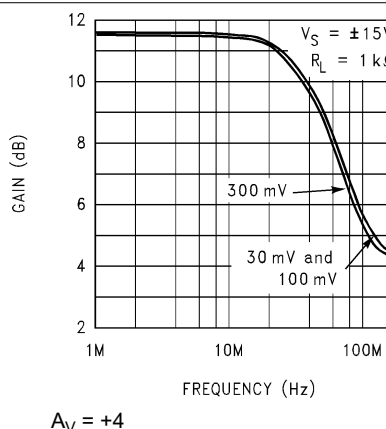
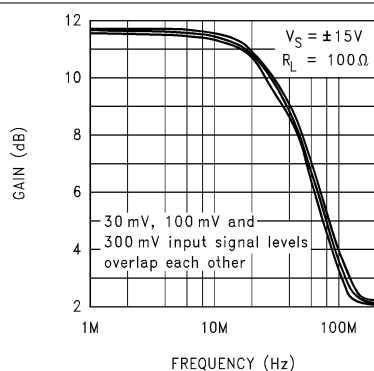


FIG 5-81. Closed-Loop Frequency Response vs Input Signal Level

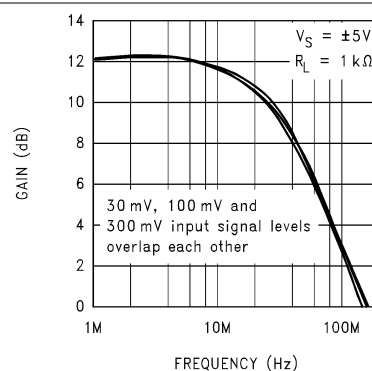
5.8 Typical Characteristics: LM7171B (continued)

at $T_A = 25^\circ\text{C}$ (unless otherwise noted)



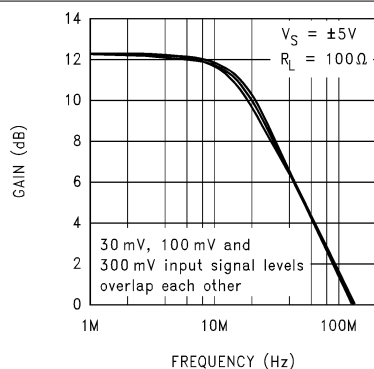
$A_V = +4$

FIG 5-82. Closed-Loop Frequency Response vs Input Signal Level



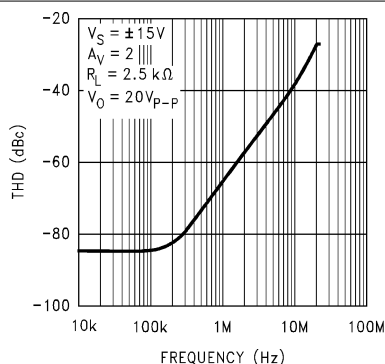
$A_V = +4$

FIG 5-83. Closed-Loop Frequency Response vs Input Signal Level



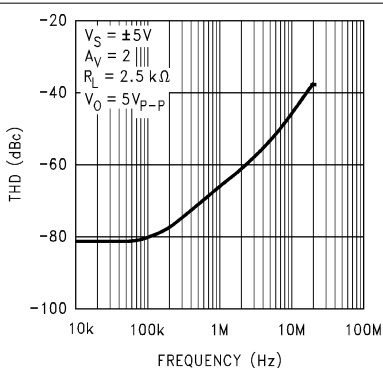
$A_V = +4$

FIG 5-84. Closed-Loop Frequency Response vs Input Signal Level



THD measurement at low frequency limited by test instrument

FIG 5-85. Total Harmonic Distortion vs Frequency



THD measurement at low frequency limited by test instrument

FIG 5-86. Total Harmonic Distortion vs Frequency

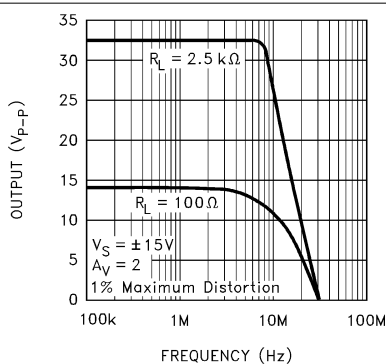


FIG 5-87. Undistorted Output Swing vs Frequency

5.8 Typical Characteristics: LM7171B (continued)

at $T_A = 25^\circ\text{C}$ (unless otherwise noted)

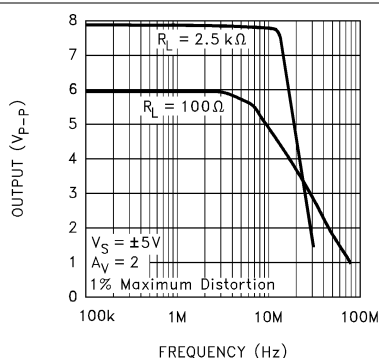


Figure 5-88. Undistorted Output Swing vs Frequency

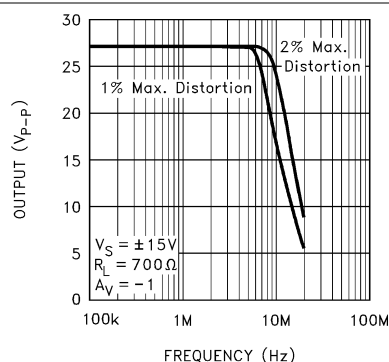
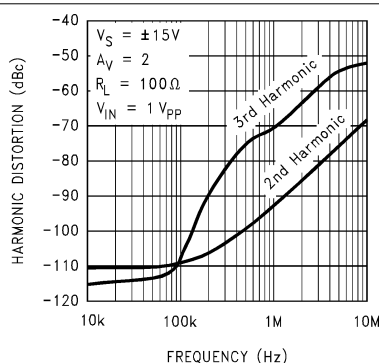
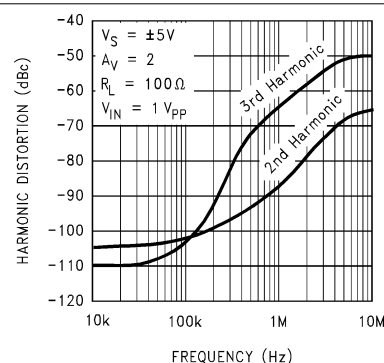


Figure 5-89. Undistorted Output Swing vs Frequency



THD measurement at low frequency limited by test instrument

Figure 5-90. Harmonic Distortion vs Frequency



THD measurement at low frequency limited by test instrument

Figure 5-91. Harmonic Distortion vs Frequency

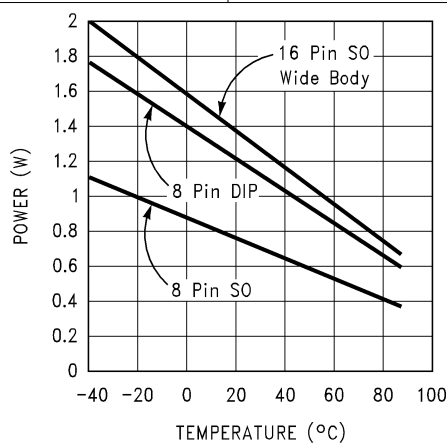


Figure 5-92. Maximum Power Dissipation vs Ambient Temperature

6 Application and Implementation

注

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6.1 Application Information

The LM7171 is a very high-speed, voltage-feedback amplifier (VFA). This device consumes only 6.5mA of supply current while providing a unity-gain bandwidth of 200MHz and a slew rate of 4100V/ μ s. The LM7171 also has other great features such as low differential gain and phase and high output current.

The LM7171 is a true VFA. Unlike a current-feedback amplifier (CFA) with a low inverting input impedance and a high noninverting input impedance, both inputs of a VFA have high-impedance nodes. The low-impedance inverting input of a CFA and a feedback capacitor create an additional pole that leads to instability. As a result, CFAs cannot be used in traditional op-amp circuits such as photodiode amplifiers, I-to-V converters, and integrators, where a feedback capacitor is required.

6.1.1 Circuit Operation

The class AB input stage in LM7171 is fully symmetrical and has a similar slewing characteristic to a CFA. In the LM7171 simplified schematic, Q1 through Q4 form the equivalent of the current-feedback input buffer, R_E the equivalent of the feedback resistor, and stage A buffers the inverting input. The triple-buffered output stage isolates the gain stage from the load to provide low output impedance.

6.1.2 Slew Rate Characteristic

The slew rate of LM7171 is determined by the current available to charge and discharge an internal high impedance node capacitor. This current is the differential input voltage divided by the total degeneration resistor R_E . Therefore, the slew rate is proportional to the input voltage level, and the higher slew rates are achievable in the lower gain configurations. A curve of slew rate versus input voltage level is provided in [セクション 5.8](#).

When a very fast large signal pulse is applied to the input of an amplifier, some overshoot or undershoot occurs. By placing an external resistor such as 1k Ω in series with the input of LM7171, the bandwidth is reduced to help lower the overshoot.

6.1.2.1 Slew-Rate Limitation

If the amplifier input signal amplitude is too large and the frequency too high, the amplifier is slew-rate limited. This limiting can cause ringing in the time domain and peaking in the frequency domain at the output of the amplifier.

For the $A_V = +2$ curves, slight peaking occurs. This peaking at high frequency (> 100 MHz) is due to a large input signal at a high enough frequency that exceeds the amplifier slew rate. The peaking in the frequency response does not limit the pulse response in the time domain, and the LM7171 is stable with a noise gain of $\geq +2$.

6.1.3 Compensation for Input Capacitance

The combination of an amplifier input capacitance with the gain setting resistors adds a pole that can cause peaking or oscillation. To solve this problem, a feedback capacitor with a value of

$$C_F > (R_G \times C_{IN}) / R_F \quad (1)$$

can be used to cancel that pole. For LM7171, a feedback capacitor of 2pF is recommended. 図 6-1 illustrates the compensation circuit.

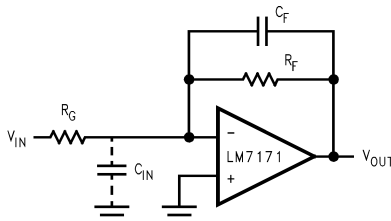


図 6-1. Compensating for Input Capacitance

6.2 Typical Applications

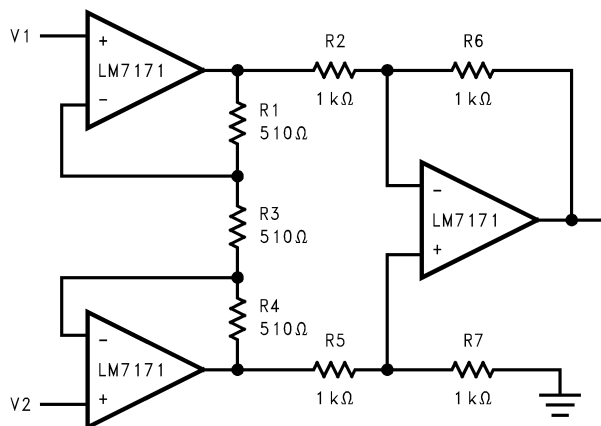


図 6-2. Fast Instrumentation Amplifier

$$V_{IN} = V_2 - V_1$$

if $R_6 = R_2$, $R_7 = R_5$, and $R_1 = R_4$

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_6}{R_2} \left(1 + 2 \frac{R_1}{R_3} \right) = 3$$

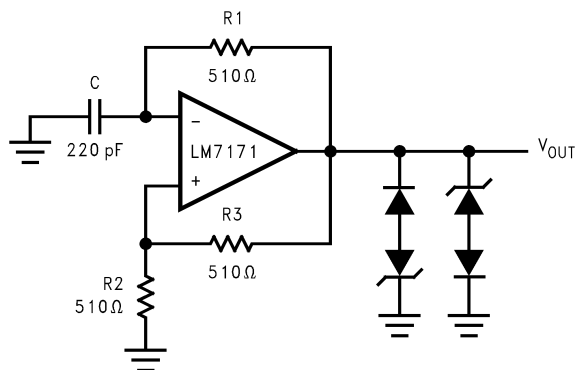
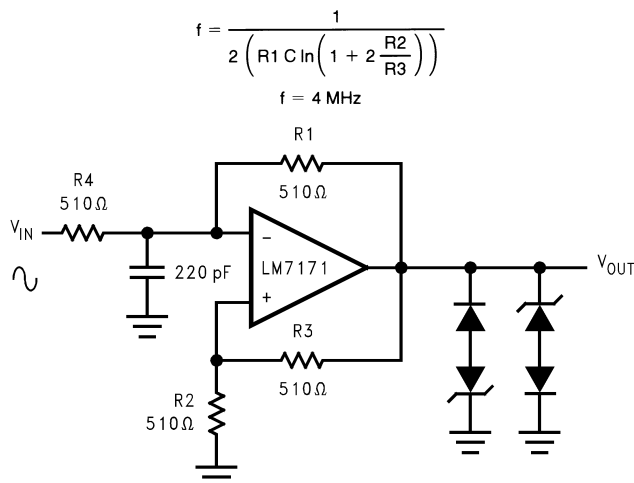
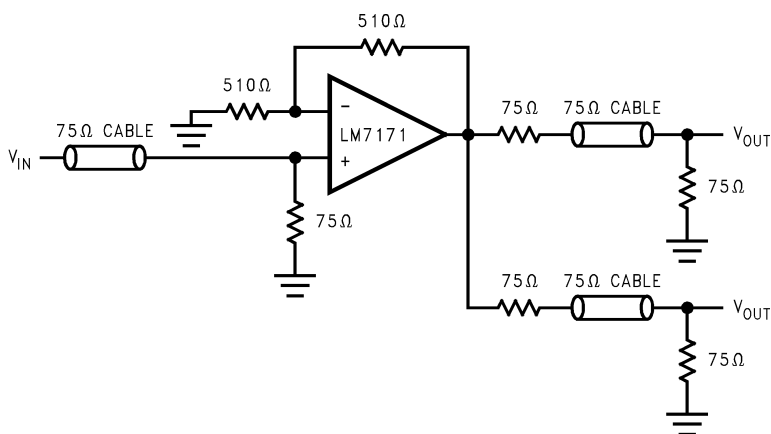


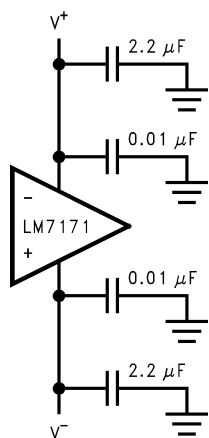
図 6-3. Multivibrator


 **6-4. Pulse Width Modulator**

 **6-5. Video Line Driver**

6.3 Power Supply Recommendations

6.3.1 Power-Supply Bypassing

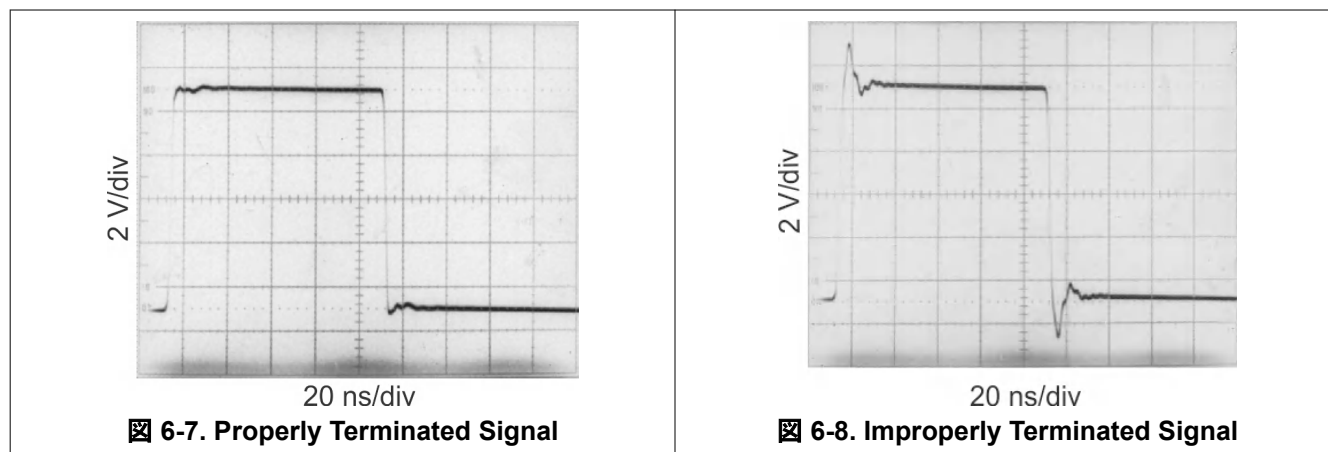
Bypassing the power supply is necessary to maintain low power-supply impedance across frequency. To bypass both positive and negative power supplies individually, place 0.01μF ceramic capacitors directly to the power-supply pins, and 2.2μF tantalum capacitors close to the power-supply pins.



✎ 6-6. Power-Supply Bypassing

6.3.2 Termination

In high-frequency applications, reflections occur if signals are not properly terminated. [Figure 6-7](#) shows a properly terminated signal while [Figure 6-8](#) shows an improperly terminated signal.



To minimize reflection, use coaxial cable with matching characteristic impedance to the signal source. Terminate the other end of the cable with the same-value terminator or resistor. For commonly used cables, RG59 has a 75Ω characteristic impedance, and RG58 has a 50Ω characteristic impedance.

6.3.3 Driving Capacitive Loads

Amplifiers driving capacitive loads can oscillate or have ringing at the output. To eliminate oscillation or reduce ringing, place an isolation resistor as shown in [Figure 6-9](#). The combination of the isolation resistor and the load capacitor forms a pole to increase stability by adding more phase margin to the overall system. The desired performance depends on the value of the isolation resistor; the bigger the isolation resistor, the more damped the pulse response becomes. For LM7171, a 50Ω isolation resistor is recommended for initial evaluation. [Figure 6-10](#) shows the LM7171 driving a 150pF load with the 50Ω isolation resistor.

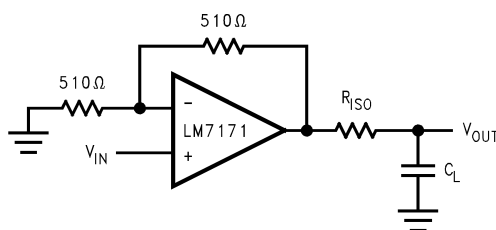


Figure 6-9. Isolation Resistor Used to Drive Capacitive Load

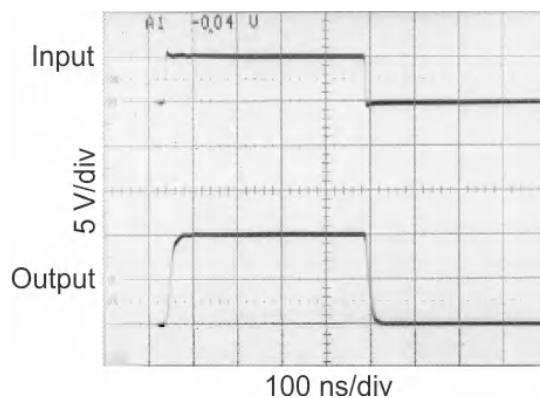


図 6-10. The LM7171 Driving a 150pF Load With a 50Ω Isolation Resistor

6.3.4 Power Dissipation

The maximum power allowed to dissipate in a device is defined as:

$$P_D = (T_{J(MAX)} - T_A) / \theta_{JA} \quad (2)$$

where

- P_D is the power dissipation in a device
- $T_{J(max)}$ is the maximum junction temperature
- T_A is the ambient temperature
- $R_{\theta JA}$ is the thermal resistance of a particular package

For example, for the LM7171 in a SOIC-8 package, the maximum power dissipation at 25°C ambient temperature is 730mW.

Thermal resistance, $R_{\theta JA}$, depends on parameters such as die size, package size and package material. The smaller the die size and package, the higher $R_{\theta JA}$ becomes. The 8-pin DIP package has a lower thermal resistance (108°C/W) than that of 8-pin SOIC (172°C/W). Therefore, for higher dissipation capability, use an 8-pin DIP package.

The total power dissipated in a device can be calculated as:

$$P_D = P_Q + P_L \quad (3)$$

where

- P_Q is the quiescent power dissipated in a device with no load connected at the output. P_L is the power dissipated in the device with a load connected at the output; P_L is not the power dissipated by the load.

Furthermore,

- P_Q is the supply current × total supply voltage with no load
- P_L is the output current × (voltage difference between supply voltage and output voltage of the same side of supply voltage)

For example, the total power dissipated by the LM7171 with $V_S = \pm 15V$ and output voltage of 10V into 1kΩ is

$$P_D = P_Q + P_L \quad (4)$$

$$= (6.5mA) \times (30V) + (10mA) \times (15V - 10V) \quad (5)$$

$$= 195mW + 50mW \quad (6)$$

$$= 245mW \quad (7)$$

6.4 Layout

6.4.1 Layout Guidelines

6.4.1.1 Printed Circuit Board and High-Speed Op Amps

There are many things to consider when designing printed circuit boards (PCBs) for high-speed op amps. Without proper caution, excessive ringing, oscillation, and other degraded ac performance can easily occur in high-speed circuits. As a rule, keep signal traces short and wide to provide low inductance and low impedance paths. Ground any unused board space to reduce stray signal pickup. Ground critical components at a common point to eliminate voltage drop. Sockets add capacitance to the board and can affect high-frequency performance. Soldering the amplifier directly into the PCB without using any socket is better.

6.4.1.2 Using Probes

Active (FET) probes are an excellent choice for taking high-frequency measurements because of the wide bandwidth, high input impedance, and low input capacitance. However, the probe ground leads provide a long ground loop that produces errors in measurement. Instead, ground the probes directly by removing the ground leads and probe jackets and using scope probe jacks.

6.4.1.3 Component Selection and Feedback Resistor

In high-speed applications, keep all component leads short. For discrete components, choose carbon composition-type resistors and mica-type capacitors. Surface-mount components are preferred over discrete components for minimum inductive effect.

Large values of feedback resistors can couple with parasitic capacitance and cause undesirable effects, such as ringing or oscillation in high-speed amplifiers. For LM7171, a feedback resistor of 510Ω gives optimized performance.

7 Device and Documentation Support

7.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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7.5 用語集

[テキサス・インスツルメンツ用語集](#)

この用語集には、用語や略語の一覧および定義が記載されています。

8 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (September 2014) to Revision D (February 2024)	Page
ドキュメント全体にわたって表、図、相互参照の採番方法を更新.....	1
パッケージ情報を更新.....	1
Deleted footnote from <i>Recommended Operating Conditions</i>	3
Changed DC and AC specifications tables to <i>Electrical Characteristics: ±15V</i>	4
Changed LM7171A unity-gain bandwidth from 200MHz to 160MHz.....	4
Changed LM7171A settling time from 42ns to 16ns.....	4
Changed LM7171 A Input-referred voltage noise from 14nV/√Hz to 8.5nV/√Hz.....	4
Changed LM7171 A Input-referred current noise from 1.5pA/√Hz to 1pA/√Hz.....	4
Changed DC and AC specifications tables to <i>Electrical Characteristics: ±5V</i>	6
Changed LM7171A slew rate from 950V/μs to 1200V/μs.....	6
Changed LM7171A phase margin from 57° to 68°	6
Changed LM7171A settling time from 56ns to 15ns.....	6
Changed LM7171A propagation delay from 6ns to 2.5ns.....	6
Changed LM7171A input-referred voltage noise from 14nV/√Hz to 8.5nV/√Hz.....	6
Changed LM7171A input-referred current noise from 1.8pA/√Hz to 1pA/√Hz.....	6
Added new <i>Typical Characteristics</i> section for LM7171A.....	8
Deleted second paragraph in <i>Slew-Rate Limitation</i>	24

Changes from Revision B (March 2013) to Revision C (September 2014)	Page
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- | | |
|---|---|
| <ul style="list-style-type: none"> • 新しい TI 標準に合わせてデータシートのフローとレイアウトを変更。以下のセクションを追加:「製品情報」表、「アプリケーションと実装」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクション..... | 1 |
|---|---|
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Changes from Revision A (March 2013) to Revision B (March 2013)	Page
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- | | |
|---|----|
| <ul style="list-style-type: none"> • Changed layout of National Data Sheet to TI format..... | 25 |
|---|----|
-

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM7171AIM/NOPB	LIFEBUY	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LM71 71AIM	
LM7171AIMX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LM71 71AIM	Samples
LM7171BIM/NOPB	LIFEBUY	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LM71 71BIM	
LM7171BIMX/NOPB	LIFEBUY	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LM71 71BIM	
LM7171BIN/NOPB	ACTIVE	PDIP	P	8	40	RoHS & Green	NIPDAU	Level-1-NA-UNLIM	-40 to 85	LM7171 BIN	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM7171AIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM7171BIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

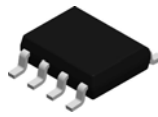
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM7171AIMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM7171BIMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
LM7171AIM/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM7171BIM/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM7171BIN/NOPB	P	PDIP	8	40	502	14	11938	4.32

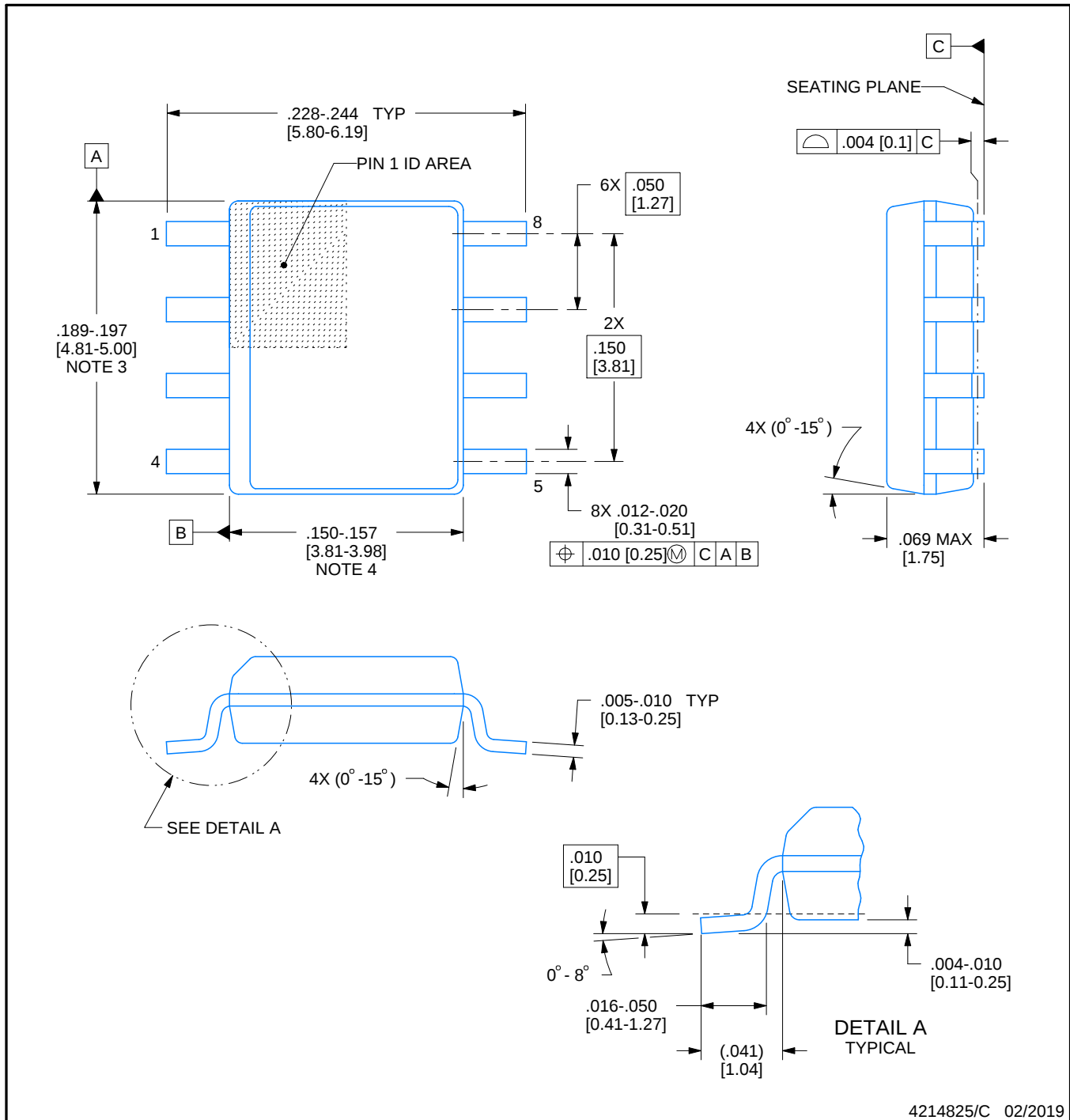


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

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