TEXAS INSTRUMENTS
CD54HC273, CD74HC273
CD54HCT273, CD74HCT273
JAJSNM9C – FEBRUARY 1998 – REVISED DECEMBER 2021

CDx4HC(T)273 高速 CMOS ロジック、オクタル D タイプ・フリップ・フロップ、リセット付き

1 特長

- 共通クロックおよび非同期コントローラ・リセット
- 正のエッジ・トリガ
- バッファ付き入力
- ファンアウト (全温度範囲にわたって)
  - 標準出力:10 の LSTTL 負荷
  - バス・ドライバ出力:15 の LSTTL 負荷
- 広い動作温度範囲:-55℃～125℃
- 平衡な伝搬遅延と遷移時間
- LSTTL ロジック IC に比べて消費電力を大幅削減
- HC タイプ:
  - 2V～6V で動作
  - 優れたノイズ耐性:N_{IL} = V_{CC} の 30%、N_{IH} = V_{CC} の 30% (VCC = 5V の場合)
- HCT タイプ:
  - 4.5V～5.5V で動作
  - LSTTL 入力ロジックと直接互換、V_{IL} = 0.8V (最大値)、V_{IH} = 2V (最小値)
  - CMOS 入力互換、V_{OL}、V_{OH} で I_I ≤ 1μA

2 説明

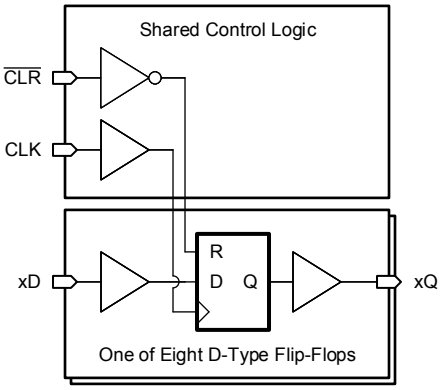
HC273 および HCT273 高速オクタル D タイプ・フリップ・フロップは、直接クリア入力が可能なシリコンゲート CMOS テクノロジーを使用して製造されています。これらは、標準的な CMOS IC の低消費電力の製品です。

D 入力の情報は、クロック・パルスの正方向エッジで Q 出力に転送されます。8 つのフリップ・フロップはすべて、共通クロック (CLK) と共通リセット ($\overline{CLR}$) で制御されます。リセットは、クロックとは独立した低電圧レベルで行われます。8 つの Q 出力はすべてロジック 0 にリセットされます。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
CD54HC273F	CDIP (20)	26.92mm × 6.92mm
CD74HC273M	SOIC (20)	12.80mm × 7.50mm
CD74HC273E	PDIP (20)	25.40mm × 6.35mm
CD74HCT273M	SOIC (20)	12.80mm × 7.50mm
CD74HCT273	PDIP (20)	25.40mm × 6.35mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



機能ブロック図

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3 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (May 2003) to Revision C (December 2021)	Page
• 最新のデータシート規格を反映するように、文書全体の採番、書式設定、表、図、相互参照を更新	1
• 現行の TI の命名規則に合わせてピン名を以下のように更新。$\overline{MR}$ を $\overline{CLR}$ に、Q0 を 1Q に、D0 を 1D に、D1 を 2D に、Q1 を 2Q に、Q2 を 3Q に、D2 を 3Q に、D3 を 4D に、Q3 を 4Q に、CP を CLK に、Q4 を 5Q に、D4 を 5D に、D5 を D6 に、Q5 を 6Q に、Q6 を 7Q に、D6 を 7D に、D7 を 8D に、Q7 を 8Q に更新	1
• Junction-to-ambient thermal resistance values increased. DW was 58 is now 109.1, N was 69 is now 84.6	4

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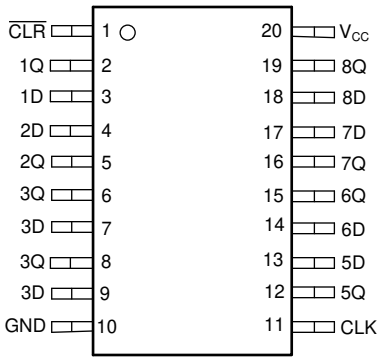
4 Pin Configuration and Functions



J, DW or N package
20-Pin CDIP, PDIP or SOIC
Top View

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		– 0.5	7	V
I_{IK}	Input clamp diode current	For $V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V		±20	mA
I_{OK}	Output clamp diode current	For $V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V		±20	mA
I_O	Drain current, per output	For $–0.5 V < V_O < V_{CC} + 0.5$ V		±25	mA
I_O	Output source or sink current per output pin	For $V_O > –0.5$ V or $V_O < V_{CC} + 0.5$ V		±25	mA
	Continuous current through V_{CC} or ground current			±50	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature range		– 65	150	°C
	Lead temperature (Soldering 10s) (SOIC - Lead Tips Only)			300	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 Recommended Operating Conditions

			MIN	MAX	UNIT
T_A	Temperature range		–55	125	℃
V_{CC}	Supply voltage range	HC types	2	6	V
		HCT types	4.5	5.5	
V_I, V_O	DC input or output voltage		0	V_{CC}	V
t_t	Input rise and fall time	2 V		1000	ns
		4.5 V		500	
		6 V		400	

5.3 Thermal Information

THERMAL METRIC		SN74HC(T)273 DW (SOIC) 20 PINS	SN74HC(T)273 N (PDIP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance[1]	109.1	84.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	76	72.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	77.6	65.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	51.5	55.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	77.1	65.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC package thermal metrics application report.

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5.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS[2]	V_{CC} (V)	25℃			–40℃ to 85℃		–55℃ to 125℃		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
V_{IH}	High level input voltage		2	1.5			1.5		1.5		V
			4.5	3.15			3.15		3.15		
			6	4.2			4.2		4.2		
V_{IL}	Low level input voltage		2			0.5		0.5		0.5	V
			4.5			1.35		1.35		1.35	
			6			1.8		1.8		1.8	
V_{OH}	High level output voltage CMOS loads	I_{OH} = – 20 µA	2	1.9			1.9		1.9		V
		I_{OH} = – 20 µA	4.5	4.4			4.4		4.4		
		I_{OH} = – 20 µA	6	5.9			5.9		5.9		
	High level output voltage TTL loads	I_{OH} = – 4 mA	4.5	3.98			3.84		3.7		V
		I_{OH} = – 5.2 mA	6	5.48			5.34		5.2		
V_{OL}	Low level output voltage CMOS loads	I_{OL} = 20 µA	2			0.1		0.1		0.1	V
		I_{OL} = 20 µA	4.5			0.1	-	0.1	-	0.1	
		I_{OL} = 20 µA	6			0.1		0.1		0.1	
	Low level output voltage TTL loads	I_{OL} = 4 mA	4.5			0.26		0.33		0.4	V
		I_{OL} = 5.2 mA	6			0.26		0.33		0.4	
I_I	Input leakage current	V_I = V_{CC} or GND	6			±0.1		±1		±1	mA
I_{CC}	Quiescent device current	V_I = V_{CC} or GND	6			8		80		160	mA
HCT TYPES											
V_{IH}	High level input voltage		4.5 to 5.5	2			2		2		V
V_{IL}	Low level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V_{OH}	High level output voltage CMOS loads	I_{OH} = – 20 µA	4.5	4.4			4.4		4.4		V
	High level output voltage TTL loads	I_{OH} = – 4 mA	4.5	3.98			3.84		3.7		
V_{OL}	Low level output voltage CMOS loads	I_{OL} = 20 µA	4.5			0.1		0.1		0.1	V
	Low level output voltage TTL loads	I_{OL} = 4 mA	4.5			0.26		0.33		0.4	
I_I	Input leakage current	V_I = V_{CC} or GND	5.5			±0.1		±1		±1	µA
I_{CC}	Quiescent device current	V_I = V_{CC} or GND	5.5			8		80		160	µA

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5.4 Electrical Characteristics (continued)

PARAMETER		TEST CONDITIONS[2]	V_{CC} (V)	25℃			–40℃ to 85℃		–55℃ to 125℃		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
ΔI_{CC} [1]	Additional quiescent device current per input pin	$\overline{CLR}$ input held at V_{CC} –2.1	4.5 to 5.5		100	540		675		735	µA
		Data inputs held at V_{CC} –2.1	4.5 to 5.5		100	144		180		196	µA
		CLK inputs held at V_{CC} –2.1	4.5 to 5.5		100	540		675		735	µA

(1) For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8mA.
(2) $V_I = V_{IH}$ or V_{IL}, unless otherwise noted.

5.5 Prerequisite for Switching Characteristics

See Parameter Measurement Information

PARAMETER		V_{CC} (V)	25℃			–40℃ to 85℃		–55℃ to 125℃		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES										
f_{MAX}	Maximum clock frequency	2	6			5		4		MHz
		4.5	30			25		20		
		6	35			29		23		
t_W	$\overline{CLR}$ pulse width	2	60			75		90		ns
		4.5	12			15		18		
		6	10			13		15		
t_W	Clock pulse width	2	80			100		120		ns
		4.5	16			20		24		
		6	14			17		20		
t_{SU}	Set-up time data to clock	2	60			75		70		ns
		4.5	12			15		18		
		6	10			13		15		
t_H	Hold time, data to clock	2	3			3		3		ns
		4.5	3			3		3		
		6	3			3		3		
t_{REM}	Removal time, $\overline{CLR}$ to clock	2	50			65		75		ns
		4.5	10			13		15		
		6	9			11		13		
HCT TYPES										
f_{MAX}	Maximum clock frequency	4.5	25			20		16		MHz
t_w	$\overline{CLR}$ pulse width	4.5	12			15		18		ns
t_w	Clock pulse width	4.5	20			25		30		ns
t_{SU}	Set-up time data to clock	4.5	12			15		18		ns
t_H	Hold time, data to clock	4.5	3			3		3		ns
t_{REM}	Removal time, $\overline{CLR}$ to clock	4.5	10			13		15		ns

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5.6 Switching Characteristics

Input t_r, t_f = 6 ns (See Parameter Measurement Information)

PARAMETER		TEST CONDITIONS	V_{CC}(V)	25℃		–40℃ to 85℃	–55℃ to 125℃	UNIT
				TYP	MAX	MAX	MAX	
HC TYPES								
t_{PLH}, t_{PHL}	Propagation delay Clock to output	C_L = 50 pF	2		150	190	225	ns
			4.5		30	38	45	
			6		26	30	38	
		C_L = 15 pF	5	12				
t_{PHL}	Propagation delay $\overline{CLR}$ to output	C_L = 50 pF	2		150	190	225	ns
			4.5		30	38	45	
			6		26	30	38	
t_{TLH}, t_{THL}	Output transition time	C_L = 50 pF	2		75	95	110	ns
			4.5		15	19	22	
			6		13	16	19	
C_{IN}	Input capacitance				10	10	10	pF
f_{MAX}	Maximum clock frequency	C_L = 15 pF	5	60				MHz
C_{PD}	Power dissipation capacitance(1) (2)		5	25				pF
HCT TYPES								
t_{PLH}, t_{PHL}	Propagation delay, Clock to output	C_L = 50 pF	4.5		30	38	45	ns
		C_L = 15 pF	5	12				
t_{PHL}	Propagation delay, $\overline{CLR}$ to output	C_L = 50 pF	4.5		32	40	48	ns
t_{TLH}, t_{THL}	Output transition time	C_L = 50 pF	4.5		15	19	22	ns
C_{IN}	Input capacitance				10	10	10	pF
f_{MAX}	Maximum clock frequency	C_L = 15 pF	5	50				MHz
C_{PD}	Power dissipation capacitance(1) (2)		5	25				pF

(1) C_{PD} is used to determine the dynamic power consumption, per flip-flop.
(2) $P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 + f_O)$ where f_i = input frequency, f_O = output frequency, C_L = output load capacitance, V_{CC} = supply voltage.

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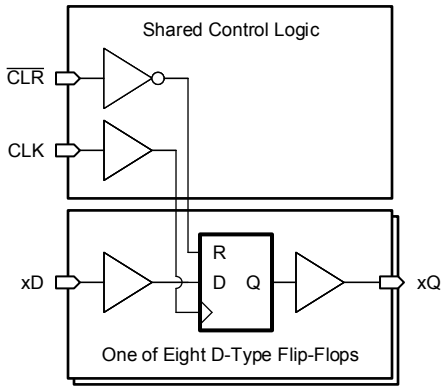
6 Detailed Description

6.1 Overview

The ’HC273 and ’HCT273 high speed octal D-Type flip-flops with a direct clear input are manufactured with silicon-gate CMOS technology. They possess the low power consumption of standard CMOS integrated circuits.

Information at the D input is transferred to the Q outputs on the positive-going edge of the clock pulse. All eight flip-flops are controlled by a common clock (CLK) and a common reset ($\overline{CLR}$). Resetting is accomplished by a low voltage level independent of the clock. All eight Q outputs are reset to a logic 0.

6.2 Functional Block Diagram



6.3 Device Functional Modes

表 6-1. Truth Table(1)

INPUTS			OUTPUT
RESET ($\overline{CLR}$)	CLOCK CLK	DATA D_n	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

(1) H = high voltage level, L = low voltage level, X = don’t care, ↑ = transition from low to high level, Q0 = level before the indicated steady-state input conditions were established

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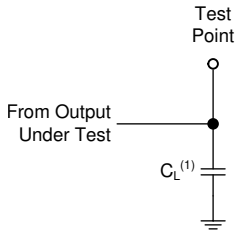
7 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_t < 6 ns.

For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



(1) C_L includes probe and test-fixture capacitance.

図 7-1. Load Circuit for Push-Pull Outputs

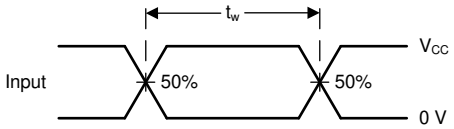


図 7-2. Voltage Waveforms, Standard CMOS Inputs Pulse Duration

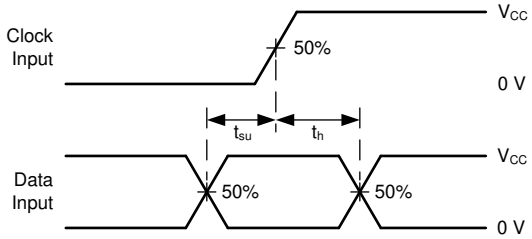
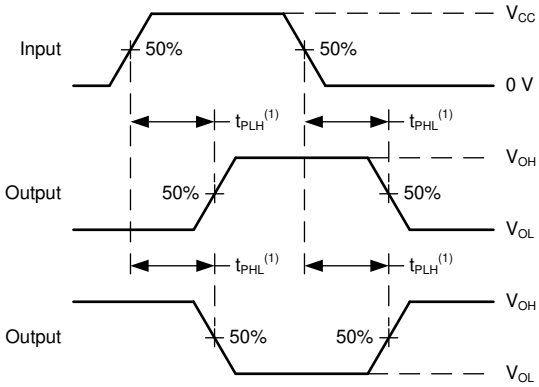
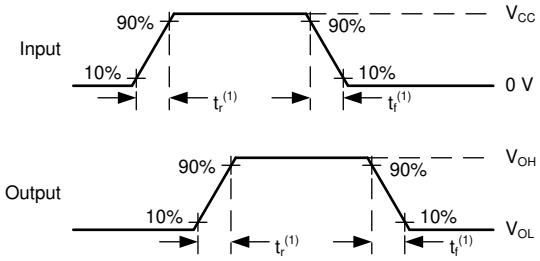


図 7-3. Voltage Waveforms, Standard CMOS Inputs Setup and Hold Times



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

図 7-4. Voltage Waveforms, Propagation Delays for Standard CMOS Inputs



(1) The greater between t_r and t_f is the same as t_t.

図 7-5. Voltage Waveforms, Input and Output Transition Times for Standard CMOS Inputs

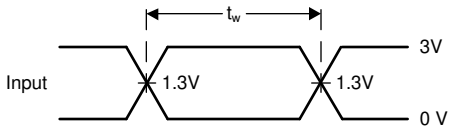


図 7-6. Voltage Waveforms, TTL-Compatible CMOS Inputs Pulse Duration

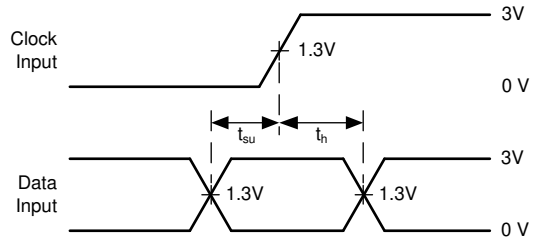
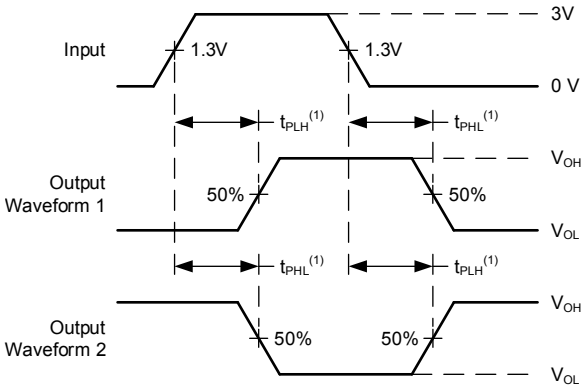


図 7-7. Voltage Waveforms, TTL-Compatible CMOS Inputs Setup and Hold Times



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

図 7-8. Voltage Waveforms, Propagation Delays for TTL-Compatible Inputs

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8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

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10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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10.3 Trademarks

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10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8772501RA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8772501RA CD54HCT273F3A	Samples
CD54HC273F	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54HC273F	Samples
CD54HC273F3A	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8409901RA CD54HC273F3A	Samples
CD54HCT273F	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54HCT273F	Samples
CD54HCT273F3A	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8772501RA CD54HCT273F3A	Samples
CD74HC273E	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC273E	Samples
CD74HC273M96	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC273M	Samples
CD74HC273M96E4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC273M	Samples
CD74HCT273E	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT273E	Samples
CD74HCT273EE4	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT273E	Samples
CD74HCT273M96	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT273M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54HC273, CD54HCT273, CD74HC273, CD74HCT273 :

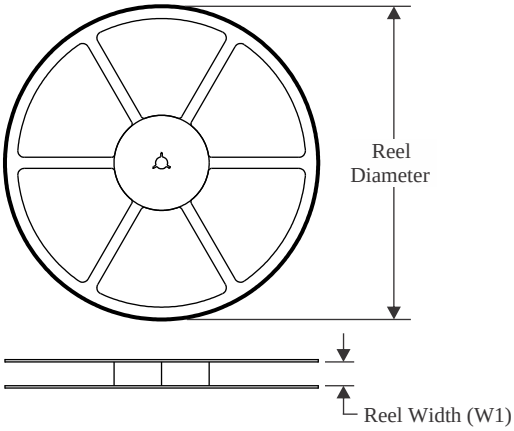
- Catalog : CD74HC273, CD74HCT273
- Military : CD54HC273, CD54HCT273

NOTE: Qualified Version Definitions:

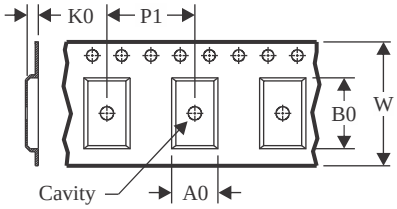
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

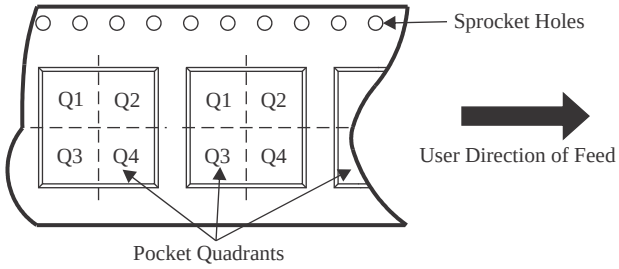


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

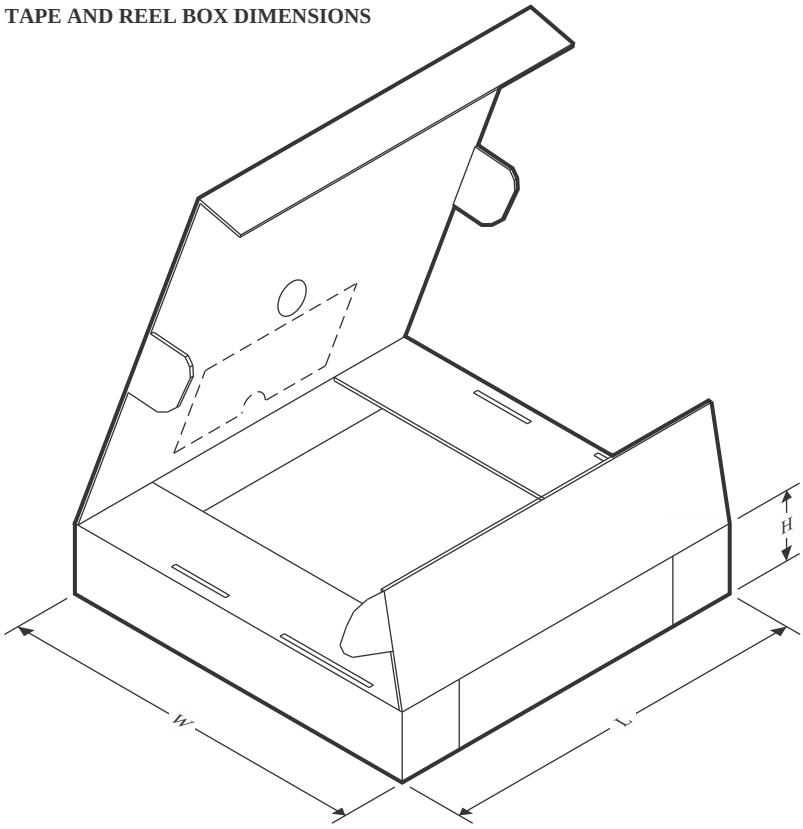
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC273M96	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
CD74HC273M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74HCT273M96	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
CD74HCT273M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

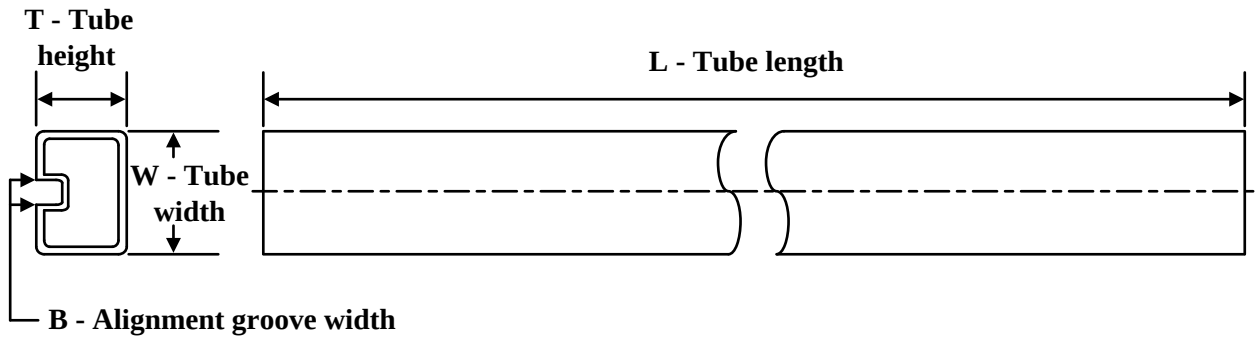
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC273M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74HC273M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74HCT273M96	SOIC	DW	20	2000	356.0	356.0	41.0
CD74HCT273M96	SOIC	DW	20	2000	367.0	367.0	45.0

TUBE



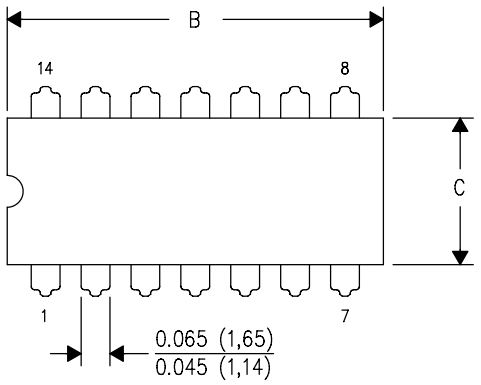
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74HC273E	N	PDIP	20	20	506	13.97	11230	4.32
CD74HCT273E	N	PDIP	20	20	506	13.97	11230	4.32
CD74HCT273EE4	N	PDIP	20	20	506	13.97	11230	4.32

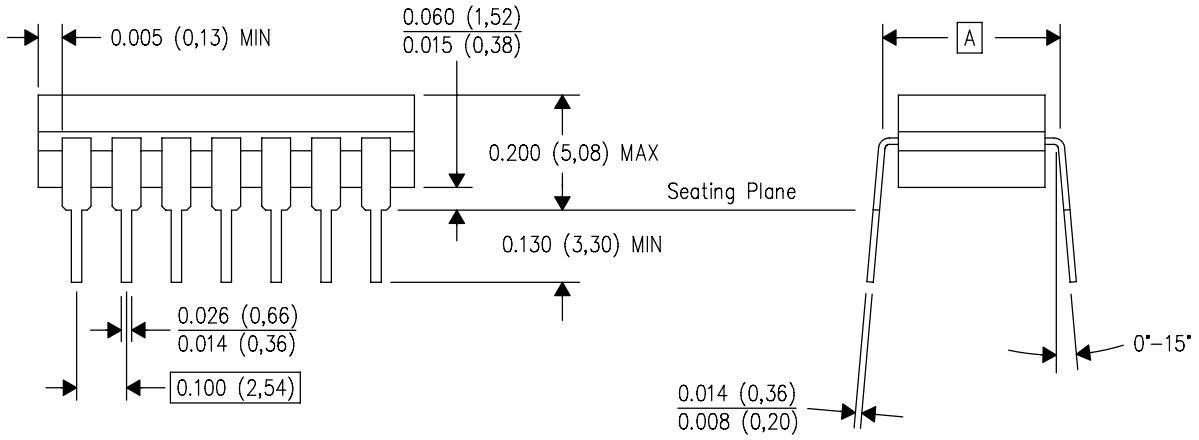
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



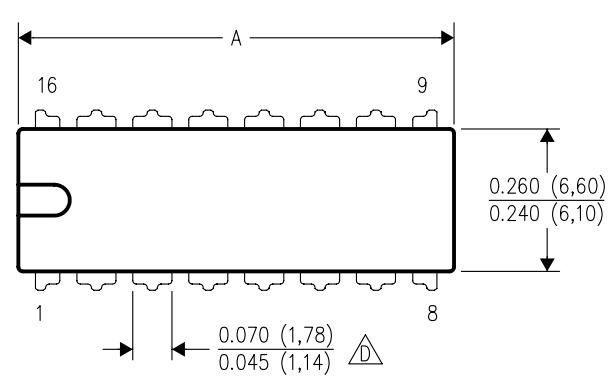
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

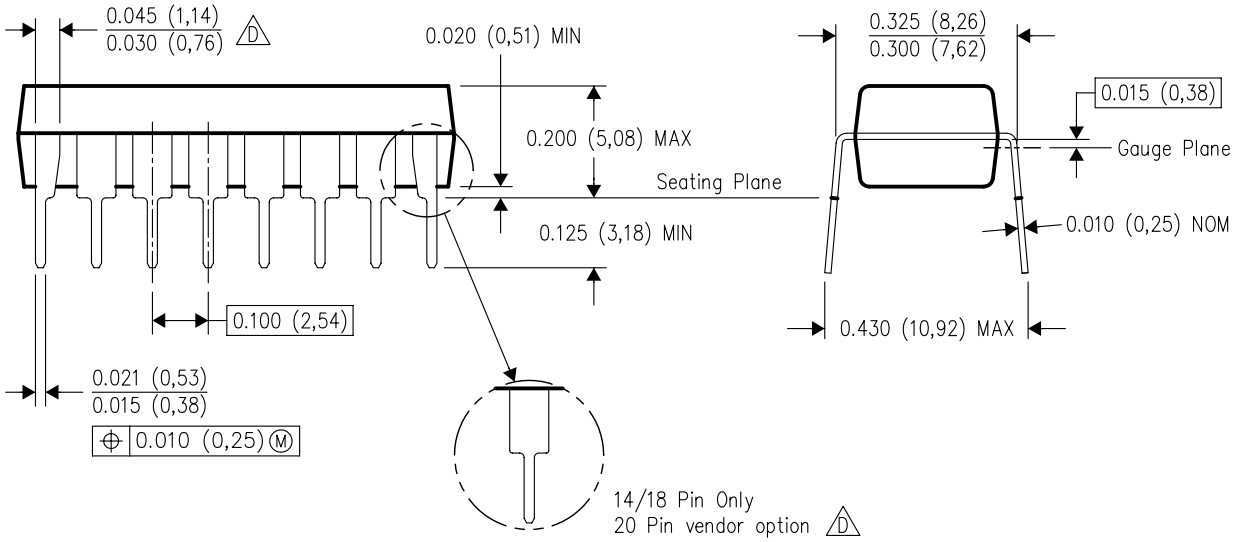
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

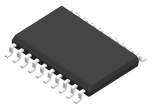


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

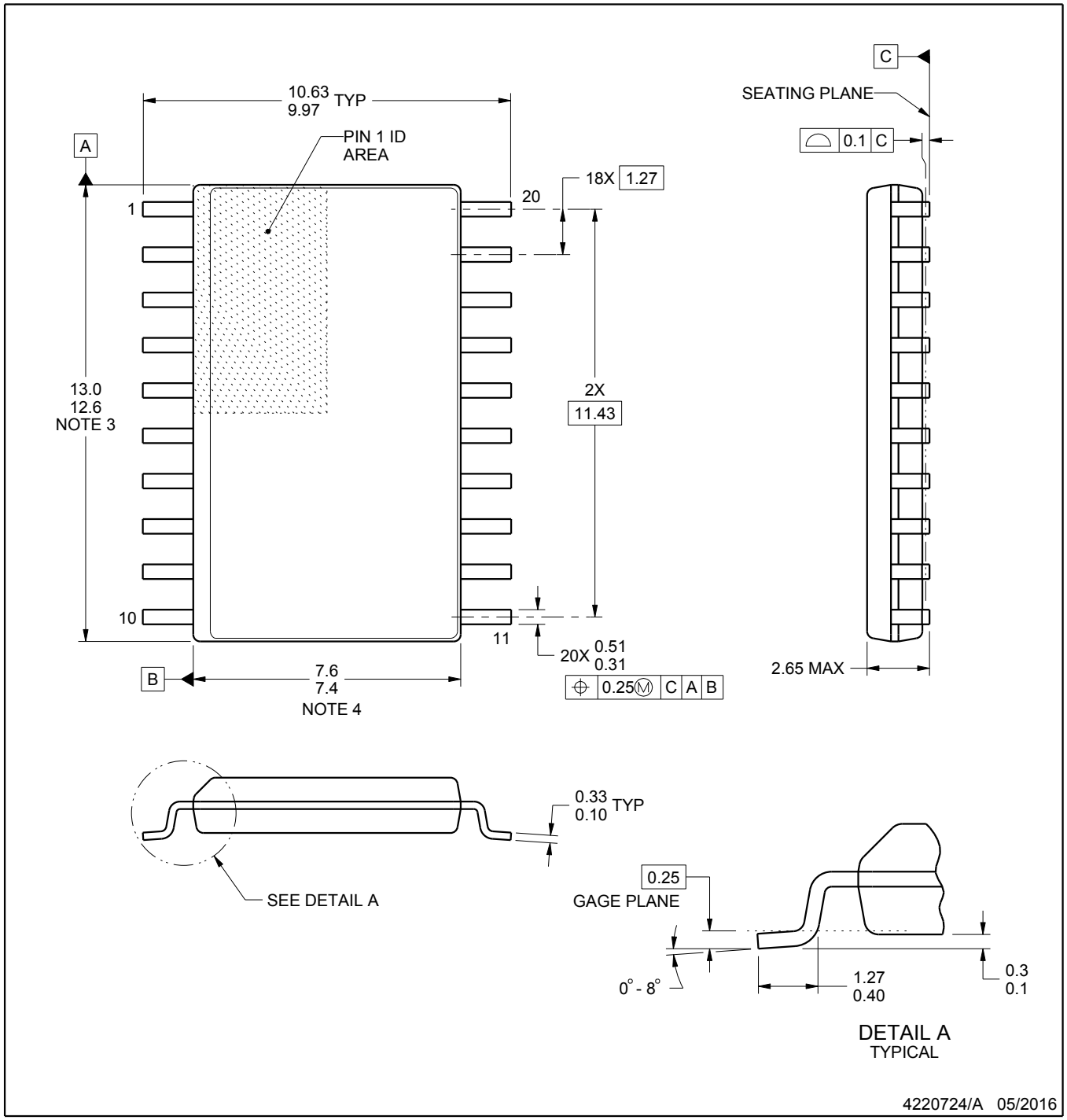


PACKAGE OUTLINE

DW0020A

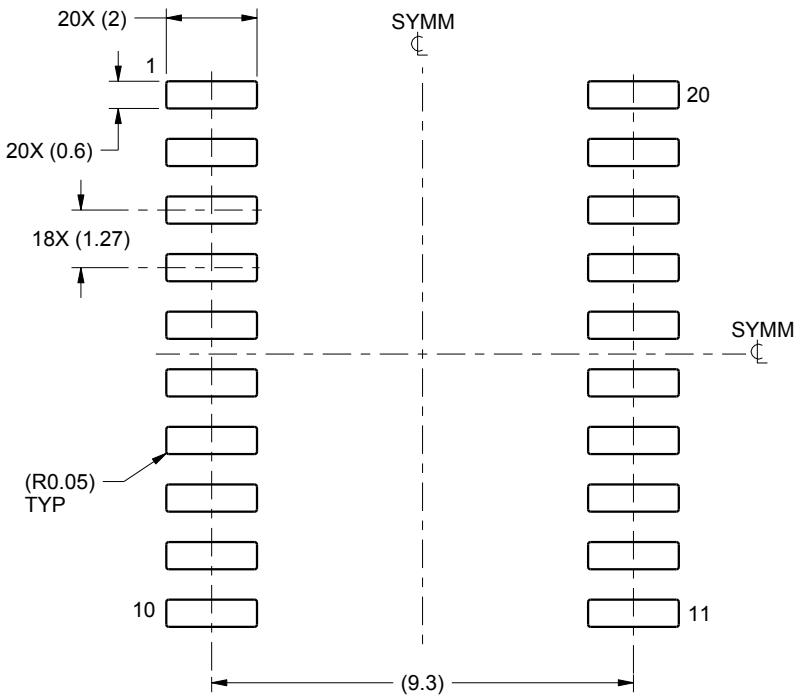
SOIC - 2.65 mm max height

SOIC

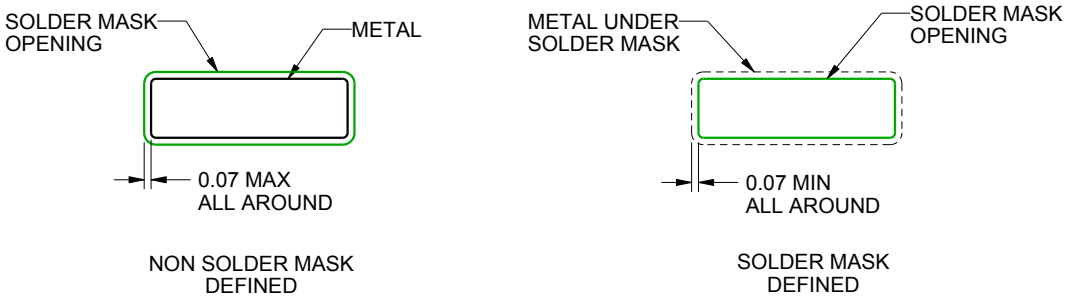


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

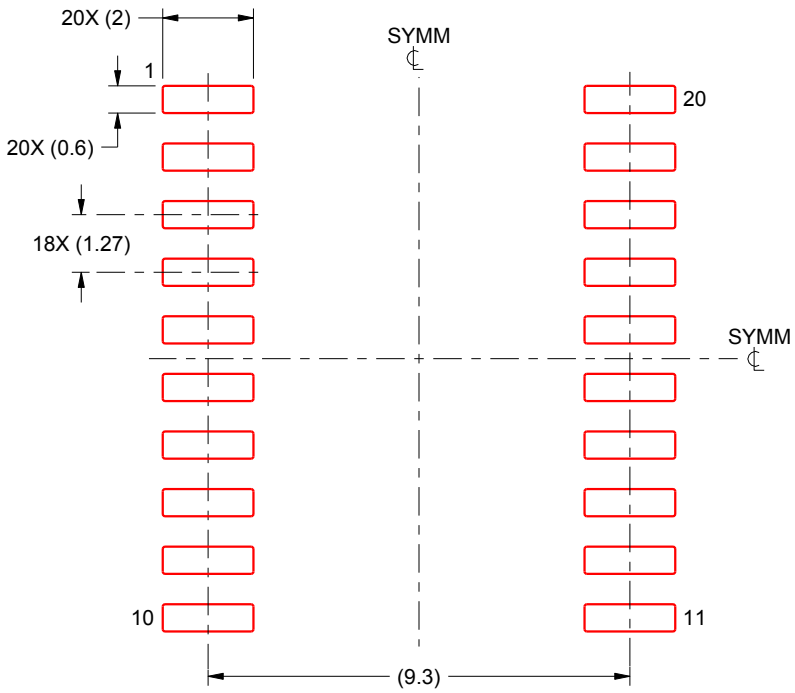


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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